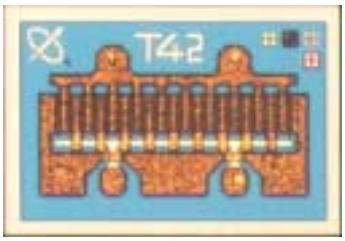
0.5W High Linearity and High Efficiency GaAs Power FETs

FEATURES

- 0.5W Typical Power at 12 GHz
- Linear Power Gain: G_L = 11 dB Typical at 12 GHz
- High Linearity: IP3 = 37 dBm Typical at 12 GHz
- High Power Added Efficiency: Nominal PAE of 40 % at 12 GHz
- Non-Via Hole Source for Single-Bias Application
- Suitable for High Reliability Application
- Breakdown Voltage: BV_{DGO} ≥ 13.5 V
- Lg = 0.25 μm, Wg = 1.2 mm
- Tight Vp ranges control
- High RF input power handling capability
- 100 % DC Tested

PHOTO ENLARGEMENT



DESCRIPTION

The TC1404N is a GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) which has high linearity and high Power Added Efficiency. The device is processed without via-holes for single-bias applications. The short gate length enables the device to be used in circuits up to 20GHz. All devices are 100% DC tested to assure consistent quality. Bond pads are gold plated for either thermo-compression or thermo-sonic wire bonding. Backside gold plating is compatible with standard AuSn die-attach. Typical applications include commercial and military high performance power amplifiers

ELECTRICAL SPECIFICATIONS (T_A=25 °C)

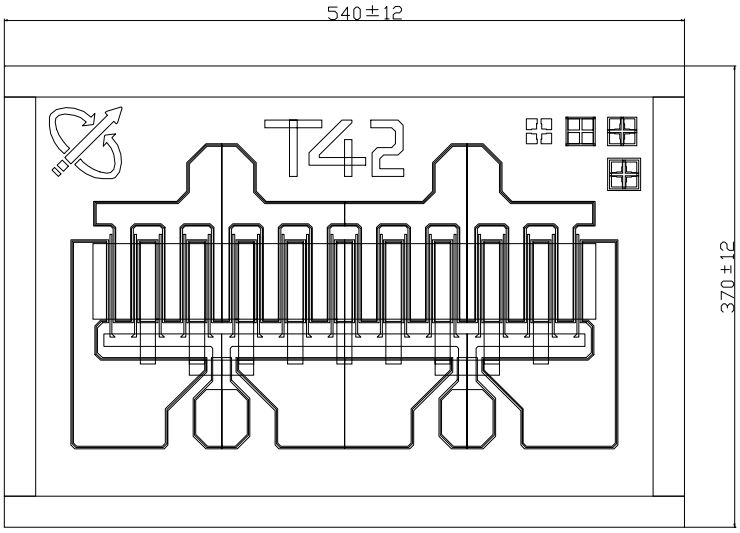
Symbol	Conditions	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point , f = 12GHz V_{DS} = 8 V, I_{DS} = 120 mA	26.5	27		dBm
G_L	Linear Power Gain, f = 12GHz V_{DS} = 8 V, I_{DS} = 120 mA		11		dB
IP3	Intercept Point of the 3rd-order Intermodulation, f = 12GHz V_{DS} =8V, I_{DS} = 120 mA, *P_{SCL} = 14 dBm		37		dBm
PAE	Power Added Efficiency at 1dB Compression Power, f = 12GHz		40		%
I_{DSS}	Saturated Drain-Source Current at V_{DS} = 2 V, V_{GS} = 0 V		360		mA
g_m	Transconductance at V_{DS} = 2 V, V_{GS} = 0 V		260		mS
V_P	Pinch-off Voltage at V_{DS} = 2 V, I_D = 2.4 mA		-1.7		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at I_{DGO} =0.6 mA	13.5	15		Volts
R_{th}	Thermal Resistance		30		°C/W

Note:
*** P_{SCL}: Output Power of Single Carrier Level.**

ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Symbol	Parameter	Rating
V_{DS}	Drain-Source Voltage	12 V
V_{GS}	Gate-Source Voltage	-5 V
I_{DS}	Drain Current	I_{DSS}
P_{in}	RF Input Power, CW	26 dBm
P_T	Continuous Dissipation	1.9 W
T_{CH}	Channel Temperature	175 °C
T_{STG}	Storage Temperature	- 65 °C to +175 °C

CHIP DIMENSIONS



Units : Micrometer

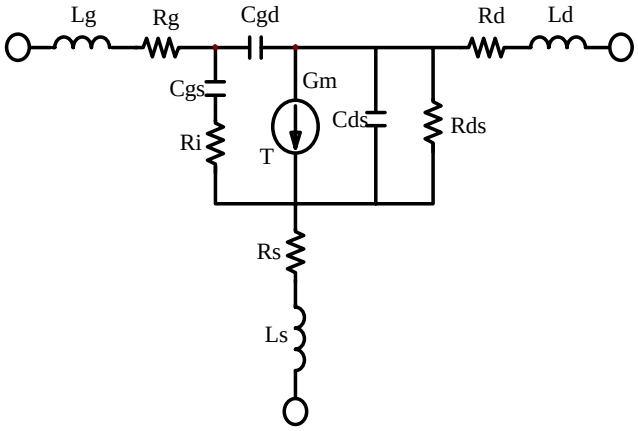
Chip Thickness : 76.2

Gate Pad : 45*45

Drain Pad : 55*55

SMALL SIGNAL MODEL, V_{DS} = 8 V, I_{DS} = 120 mA

SCHEMATI

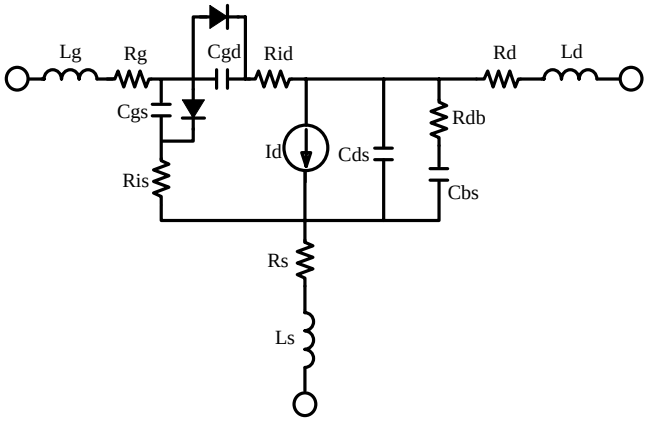


PARAMETERS

Lg	0.02 nH	**Rs**	0.8 Ohm
Rg	0.97 Ohm	**Ls**	0.005 nH
Cgs	2.652 pF	**Cds**	0.274 pF
Ri	1.246 Ohm	**Rds**	55.8 Ohm
Cgd	0.144 pF	**Rd**	0.65 Ohm
Gm	574.6 mS	**Ld**	0.02 nH
T	3.9 psec		

LARGE SIGNAL MODEL, V_{DS} = 8 V, I_{DS} = 120 mA

SCHEMATI



TOM2 MODEL PARAMETERS

VTO	-1.62 V	**VMAX**	0.5 V
ALPHA	14.13	**CGD**	0.144 pF
BETA	0.354	**CGS**	2.652 pF
GAMMA	0.0228	**CDS**	0.274 pF
DELTA	0.1565	**RIS**	2.005 Ohm
Q	0.88	**RID**	0.0001 Ohm
NG	0.1	**VBR**	13.5 V
ND	0.01	**RDB**	119.667 Ohm
TAU	3.9 ps	**CBS**	2.5 pF
RG	0.97 Ohm	**TNOM**	25 °C
RD	0.65 Ohm	**LS**	0.005 nH
RS	0.8 Ohm	**LG**	0.02 nH
IS	1E-11 mA	**LD**	0.02 nH
N	1	**AFAC**	1
VBI	1 V	**NFING**	1
VDELTA	0.2 V		

CHIP HANDLING

DIE ATTACHMENT: Conductive epoxy or eutectic die attach is recommended. Eutectic die attach can be accomplished with Au-Sn (80%Au-20%Sn) perform at stage temperature: 290°C ± 5°C; Handling Tool: Tweezers; Time: less than 1min.

WIRE BONDING: The recommended wire bond method is thermocompression bonding with 0.7 to 1.0 mil (0.018 to 0.025 mm) gold wire. Stage temperature: 220°C to 250°C; Bond Tip Temperature: 150°C; Bond Force: 20 to 30 gms depending on size of wire and Bond Tip Temperature.

HANDLING PRECAUTIONS: The user must operate in a clean, dry environment. Care should be exercised during handling avoid damage to the devices. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.