

55W Power Transistor

GaN HEMT on SiC

Description

The CHK9014-99F is a 55W Gallium Nitride High Electron Mobility Transistor.

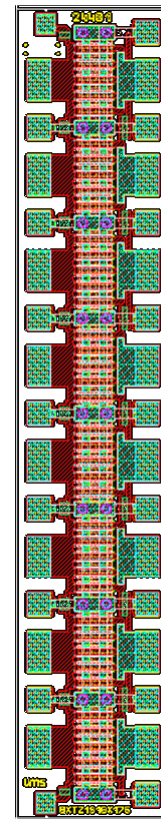
This product offers a general purpose and broadband solution for a variety of RF power applications such as radar and telecommunication.

The circuit is manufactured on a 0.25 μ m gate length GaN HEMT technology on SiC substrate.

It is proposed in a bare die form and requires an external matching circuitry.

Main Features

- Wide band capability up to 13GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: V_D up to 30V
- Chip size: 0.88x4.27x0.1mm
- RoHS N°2011/65
- REACh N°1907/2006



Main Electrical Characteristics

$T_{ref} = +25^{\circ}C$, Pulsed mode, Freq=12GHz, $V_{DS}=30V$, $I_{D,Q}=0.85A$

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		13		dB
P_{SAT}	Saturated Output Power		60		W
PAE	Max Power Added Efficiency		50		%
G_{PAE_MAX}	Associated Gain at Max PAE		8		dB

These values are deduced from elementary power cell performances.

Recommended Operating Ratings

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _{DS}	Drain to Source Voltage			30	V	
V _{GS}	Gate to Source Voltage		-3.3		V	V _{DS} =30V, I _{D,Q} =0.7A
V _{DG_peak}	Drain-Gate Voltage		80		V	DC+RF
V _{GS_peak}	Gate-Source Voltage	-20			V	DC+RF
I _{D,Q}	Quiescent Drain Current		0.7	1.6 ⁽¹⁾	A	V _{DS} =30V
I _{D,MAX}	Drain Current			3.6 ⁽¹⁾	A	V _{DS} =30V, compressed mode
I _{G,MAX}	Gate Current in forward mode		0	55	mA	DC or Compressed mode
T _{J,MAX}	Junction temperature			200	°C	(1)

(1) Power dissipation must be considered.

DC Characteristics

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _P	Pinch-Off Voltage	-4	-3.4	-2.8	V	V _D =10V, I _D = I _{DSS} /100
I _{D,SAT}	Saturated Drain Current		12.5		A	(1), V _D =10V, V _G =1V
I _{G,leak}	Gate Leakage Current	-2.8			mA	V _D =50V, V _G =-7V
V _{B DG}	Drain-Gate Break-down Voltage		120		V	V _G =-7V, I _D =20mA

(1) For information, limited by I_{D,MAX}, see on ROR & AMR.

RF Characteristics

T_{ref}= +25°C, Pulsed mode, Freq=12GHz, V_{DS}=30V, I_{D,Q}=0.7A

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G _{SS}	Small Signal Gain		13		dB	
P _{SAT}	Saturated Output Power		60		W	
P _{AE}	Max Power Added Efficiency		50		%	
G _{PAE_MAX}	Associated Gain at Max PAE		8		dB	

These values are deduced from elementary power cell performances.

Absolute Maximum Ratings

Tref = +25°C⁽¹⁾ ⁽²⁾ ⁽³⁾

Symbol	Parameter	Rating	Unit	Note
V _{DS_Q}	Drain-Source Biasing Voltage	55	V	
V _{GS_Q}	Gate-Source Biasing Voltage	-15, +2	V	(4), (5)
V _{DG_peak}	Drain-Gate Voltage (DC+RF)	120	V	
V _{GS_peak}	Gate-Source Voltage (DC+RF)	-25	V	
I _{G_MAX}	Maximum Gate Current	110	mA	
I _{G_MIN}	Minimum Gate Current	-7	mA	
I _{D_MAX}	Maximum Drain Current	See note		(4)
P _{IN}	Maximum Input Power	See note		(5)
T _J	Maximum Junction Temperature	230	°C	
T _{STG}	Storage Temperature	-55 to +150	°C	
T _{Case}	Case Operating Temperature	See note	°C	(4)

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

⁽³⁾ The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

⁽⁴⁾ Max junction temperature must be considered.

⁽⁵⁾ Linked to and limited by I_{g_max} & I_{g_min} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_{max}.

Biasing procedure

1. Bias power bar gate voltage at V_g close to V_{pinch-off} (Typically: V_{GS} ≈ -5V)
2. Apply V_{DS} bias voltage (Typically: V_{DS} = 30V)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.

A drain current control is recommended on the biasing network.

Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (T_j). This temperature is defined as the peak temperature in the channel area.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHK9014-99F is fabricated (GaN Power PHEMT 0.25 μ m).

The temperature T_b is defined as the chip back side temperature

The thermal resistance (R_{th}) is given for the full power bar, in "equivalent" CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

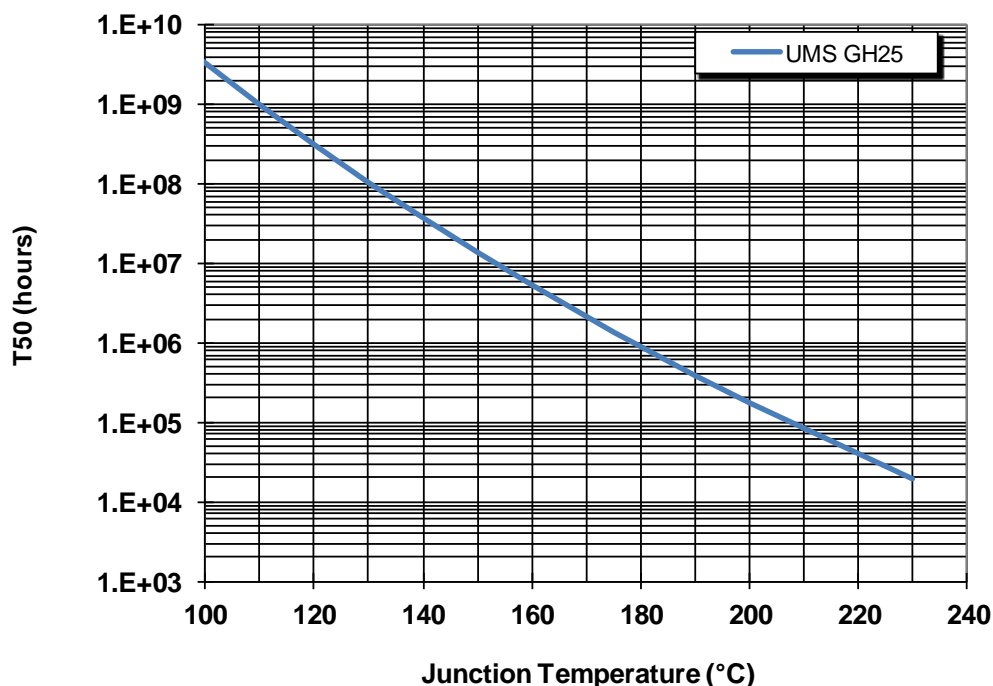
Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	R_{th}	Bare die characteristic $T_b=100^\circ\text{C}$	1.3	$^\circ\text{C}/\text{W}$
Junction Temperature	T_j	$P_{diss}=77\text{W}$ CW	200	$^\circ\text{C}$

The back side temperature (T_b) is considered uniform on all the surface

Typical Thermal Resistance	R_{th}	Bare die on carrier characteristic $T_c=75^\circ\text{C}$	2.6	$^\circ\text{C}/\text{W}$
Junction Temperature	T_j	$P_{diss}=48\text{W}$ CW	200	$^\circ\text{C}$

The reference temperature (T_c) is defined on the carrier back side. The power bar is mounted on carrier plate (20 μ m Au/Sn soldering + 1.4mm Cu/Mo/Cu).

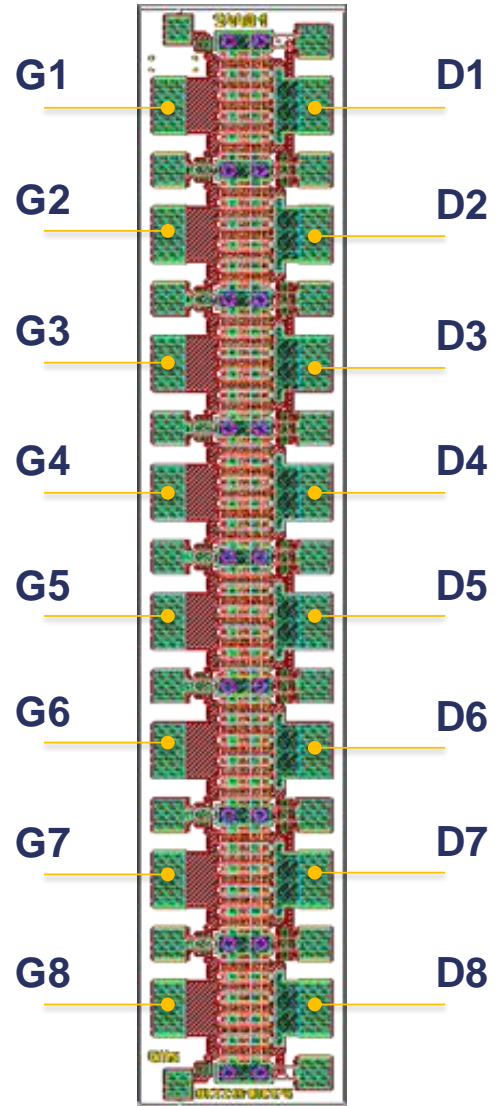
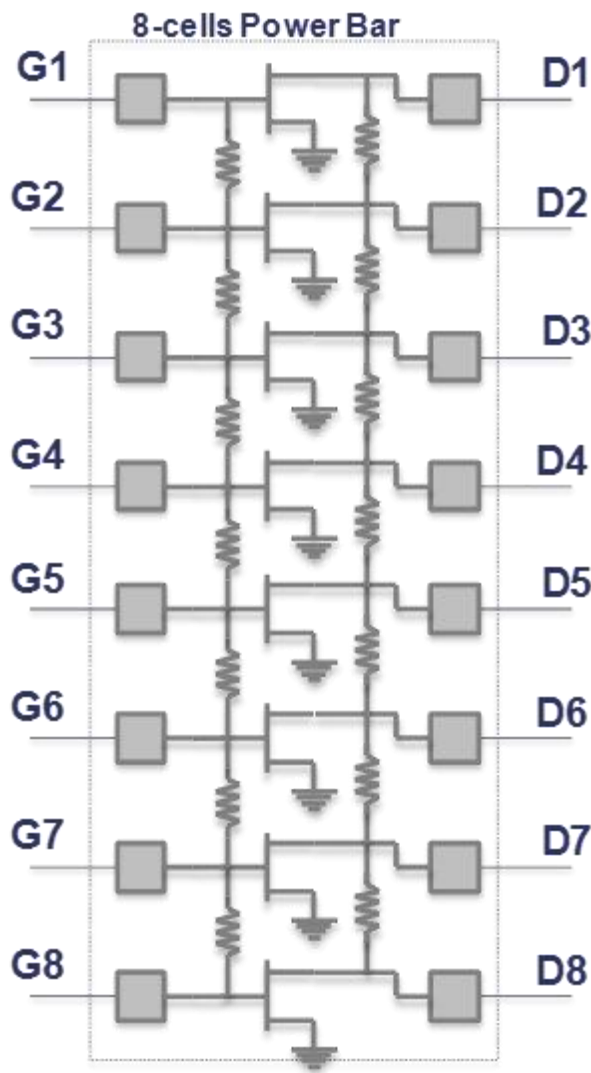
Median Life Time versus Junction Temperature



Power Bar Description

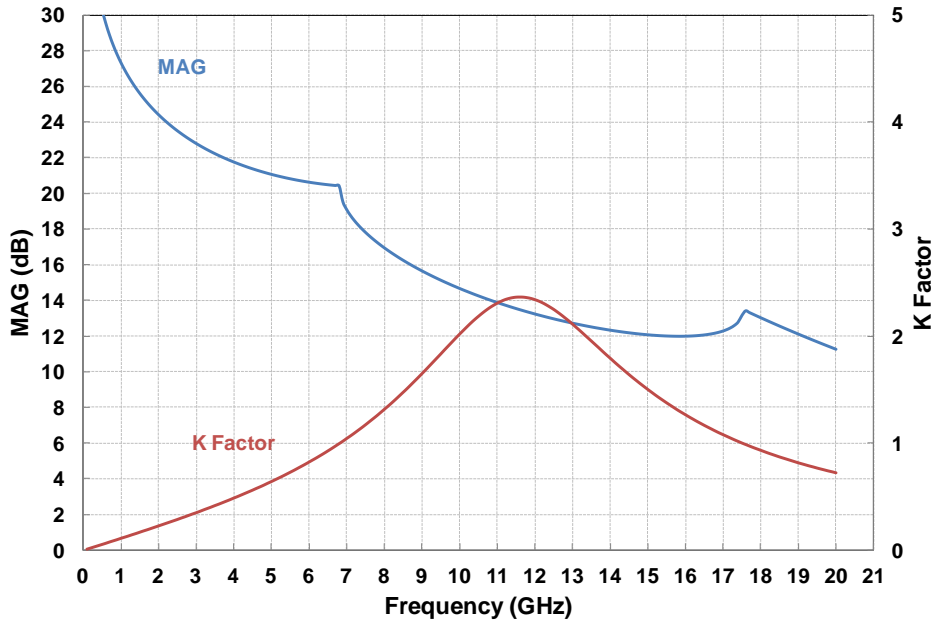
The device is composed of 8x7W elementary cells. These cells are connected together with a specific network providing a good trade-off between performance and stability (resistance between gates and drains as described on the schematic). The reference planes are on the center of the bonding pads.

A multiport non-linear model is available on request.



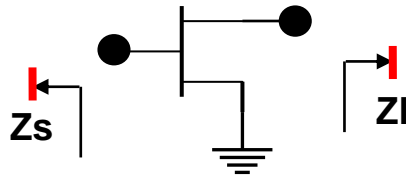
Elementary Cell Maximum Gain & Stability Characteristics

Tref = +25°C, V_{DS} = +30V, I_{D_Q} = 87mA, simulated results



Elementary Cell Load Pull Performances

Tref = +25°C, V_{DS} = +30V, I_{D_Q} = 87mA, simulated results



The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. Second harmonic of output load has been tuned.

These values are given in the bonding pads reference plane. .

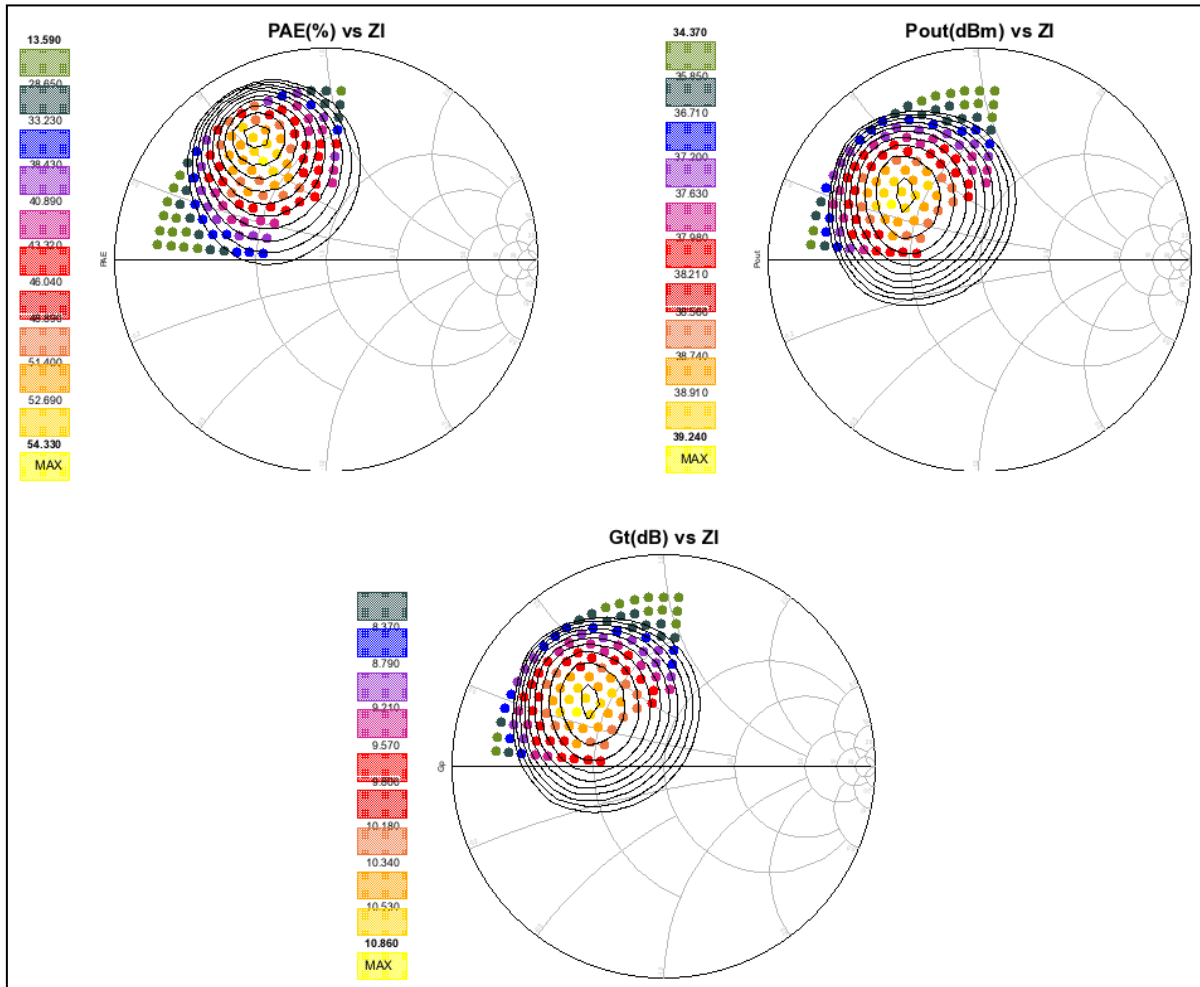
Frequency (GHz)	Zs	Zl	Gain (dB) @PAE _{max}	PAE _{max} (%)	Pout (W) @PAE _{max}	Pout _{max} (W)
3	7.3 + j7.5	42+ j39.5	13	72	7.7	9
6	4.3 + j7.6	16.6 + j30	11	72	7.7	9
9	3.4 + j3.2	8.2 + j19.2	9.7	57	6.9	7.9
12	1.58 - j0.8	4.7 + j12.75	9	53	6.3	7.9
13	1.34 - j1.62	4.1 + j11.2	8.7	52	5.8	7.8

Comparison Simulation/Measurement of Elementary Cell Load Pull Performances

Tref= +25°C, CW mode, Freq=6GHz, V_{DS}=30V, I_{D,Q}=87mA (50mA/mm)

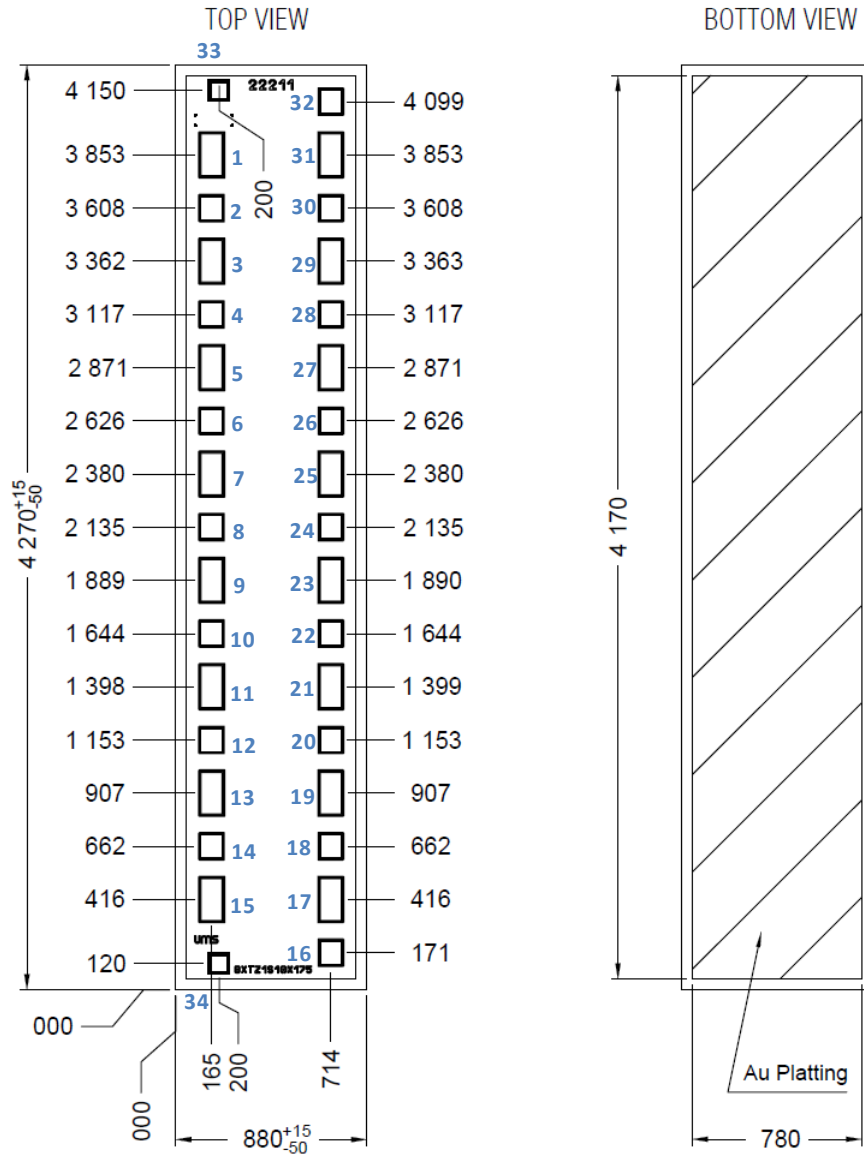
- ZloadH2=ZloadH3=50Ω
- Zsource matched for maximum gain
- CW mode applied for On wafer measurement
- Measurement are given in the transistor plan at 5dB of compression

PAE(%), Output Power (dBm) and transducer gain (dB) vs the load impedance



Measurements are represented by multicolour dots and model by black contours.

Mechanical data



Chip thickness: 100μm +/- 10 μm
All dimensions are in micrometers

All Gate and Drain pads must be connected, ground connection is optional (source is grounded through vias hole)

Reference	Pad number	Pad size
DC Gate pads	(1, 3, 5, 7, 9, 11, 13, 15)	207 x 114μm ²
DC Drain pads	(17, 19, 21, 23, 25, 27, 29, 31)	207 x 114μm ²
GND pads	(2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32)	121x112μm ²
DC Alternative Gate pads connected to resistors	(33 & 34)	90 x 90μm ²

Notes



Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at <http://www.ums-gaas.com> for general recommendations on chip handling.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at <http://www.ums-gaas.com> for general recommendations on GaN-on-SiC Transistor handling and assembly.

Ordering Information

Chip form:

CHK9014-99F/00

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