PRODUCT DATASHEET

CGY2141UH/C1

DC-46GHz High Gain Broadband Amplifier

DESCRIPTION

The CGY2141UH/C1 is a distributed very wide band 43 Gb/s Electro-Absorption Modulator (EAM) / Lithium Niobate modulator driver. This device is a key component for ultra high speed optical communication systems (OC-768/STM-256).
The CGY2141UH/C1 can also be used as a flexible, multi-purpose, very wide band gain block usable from DC to 46 GHz.

The CGY2141UH/C1 features single-ended input and output and operates with a +5.0V supply voltage via an external bias tee.

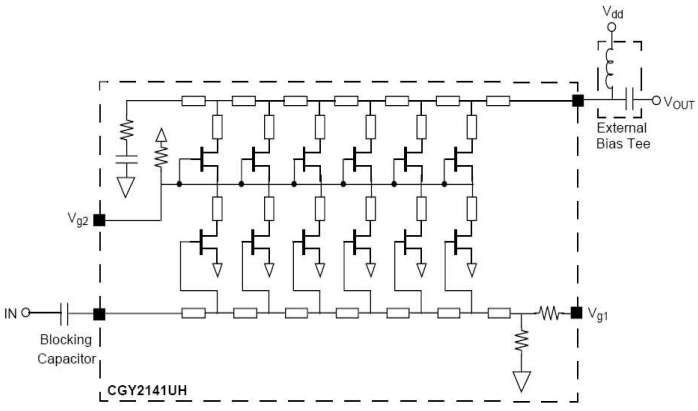
The MMIC is manufactured using OMMIC's qualified 0.13 µm PHEMT GaAs D01PH technology. The D01PH process is one of the European Space Agency (ESA) european preferred part list (EPPL) technologies.

APPLICATIONS

- 43 Gb/s OC-768 Driver amplifier for LiNbO3 Modulator or Electro-Absorption Modulator (EAM)
- Instrumentation, EW Systems
- General purpose amplifier

FEATURES

- Suitable for 43 Gb/s optical fibre links
- Wide frequency range : DC – 46 GHz
- 16 dB small signal gain
- 6.5 V_{pp} output voltage swing in a 50Ω load
- Power consumption (900 mW)
- P_{1dB} = 21 dBm at 15 GHz
- NF=2 dB at 15 GHz
- Chip size = 1270 x 1670 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Space and MIL-STD Available



Block Diagram of the CGY2141UH Broadband Amplifier

RoHS Compliant

LIMITING VALUES

Tamb = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DD}	Supply voltage		-0.5	+8	V
I_{DD}	Supply current			240	mA
V_{g1}	Gate supply voltage1		-7.0	7.0	V
V_{g2}	Gate supply voltage2		-0.5	5.0	V
T_{stg}	Storage temperature		-55	+150	° C
T_j	Junction temperature			+150	° C
T_{amb}	Ambient temperature		-10	+85	° C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient (T_a = 25 °C)	58	° C/W

DC CHARACTERISTICS

T_{amb} = 25 °C, V_{DD} = 5 V, R_L = 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		+4.75	+5.0	+5.25	V
I_{DD}	Supply current			180	200	mA
V_{g1}	Gate supply voltage1	See note 1	-4.5	0.0	4.5	V
I_{g1}	Gate supply current1			15.0		mA
V_{g2}	Gate supply voltage2		0.0	1.5	3.0	V
I_{g2}	Gate supply current2			2.0	3.0	mA

NOTE

1-V_{g1} determines the typical drain current. V_{g1} should be raised slowly from –4.5 V until the drain DC current reaches 180 mA.

AC CHARACTERISTICS

T_{amb} = 25 °C, V_{DD} = 5 V, V_{g2} = 1.5 V, I_{DD} = 180 mA, R_L = 50 Ω; The specifications mentioned below are measured on-wafer, using 50 Ω RF probes. Unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Rate	Serial Data rate	NRZ	43			Gb/s
Gain	Reference Gain	F = 3 GHz (see note 1)	15	16		dB
Gain ripple	See note 2	F = 100 MHz to 35 GHz	-0.6		+1.25	dB
		F = 35 GHz to F_C	-3		+1.25	dB
F_C	High frequency cut-off	$Gain_{3GHz}$ – 3dB	44	46		GHz
F_{C_low}	Low frequency cut-off	See note 3			50	KHz
T_G	Group delay	F = 3 GHz to 33 GHz		±8	±9	ps
		F = 33 GHz to 40 GHz		±10	±12	ps
V_{OUT}	Output swing voltage level	50Ω load, V_{in_pp} = 1.5 V		6.5		V
		50Ω load, V_{in_pp} = 0.5 V		3.0		V
t_R/t_F	Rise/Fall time	See note 4			10	ps
S11	Input return loss	F = 100 MHz to 22 GHz		-10.0	-9	dB
		F = 22 GHz to 35 GHz		-8.5	-7	dB
		F = 35 GHz to 45 GHz		-5.5	-4.5	dB
S22	Output return loss	F = 100 MHz to 40 GHz		-17	-11	dB
		F = 40 GHz to 45 GHz		-13	-10	dB
J	Jitter	See note 4			1.0	ps-rms
NF	Noise Figure	F = 5 GHz to 35 GHz		<4		dB
P1dB	Output P1dB	F = 1 GHz to 30 GHz		19		dBm
K	Microwave stability factor. T_{amb} = -10°C to +85°C	All passive source and loads	1.2			

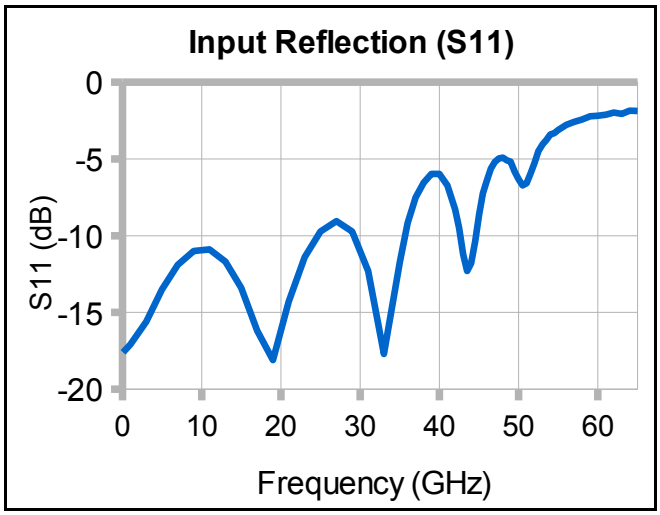
NOTE

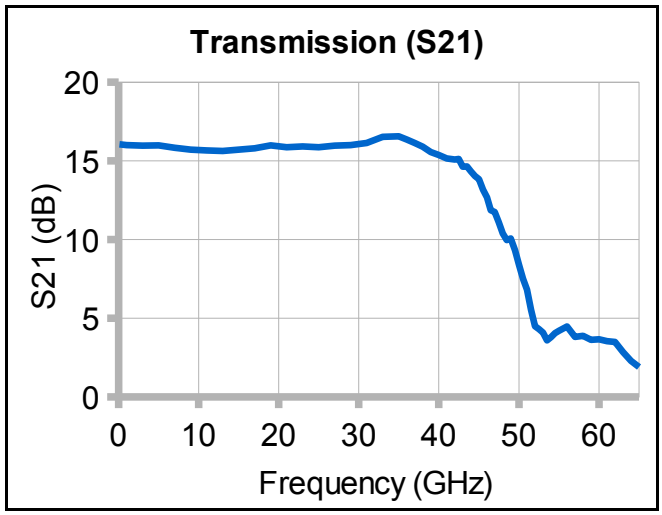
1-Measurement is guaranteed by correlation down to the lower frequency cut-off. 3 GHz is specified as a reference for convenience of measurement.
2-Low frequency gain ripple assumes the use of drain decoupling close to the chip, as proposed on the figure 1 and 2.
3-The input and output are DC coupled. The low frequency cut-off is set by the choice of the input blocking capacitor or by the output bias tee used for drain current supply voltage.
4-Measurement limited by the input reference signal, cable losses, probes and connectors.

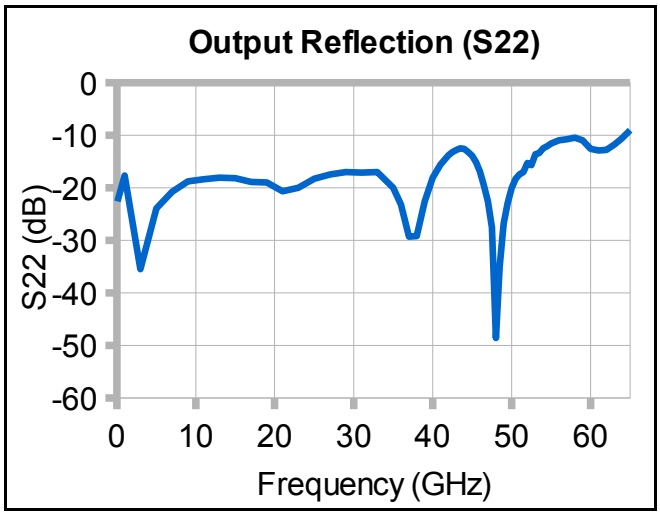
Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

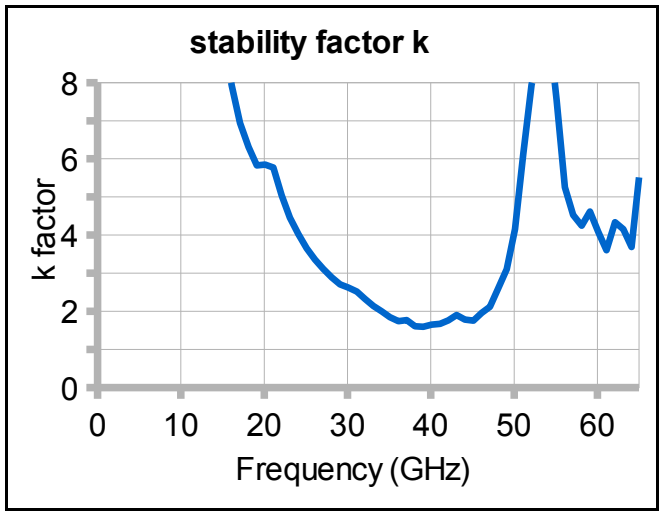
MEASURED PERFORMANCE

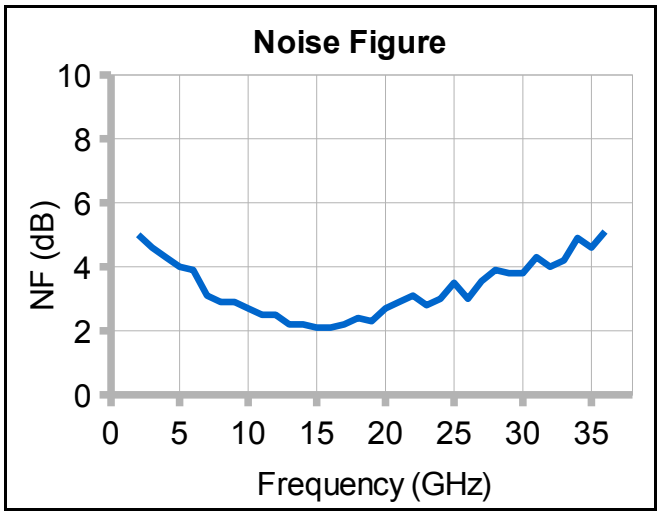
T_{amb} = 25 °C, V_{DD} = 5 V, V_{g2} = 1.5 V, I_{DD} = 180 mA, Vg1 = 0.0 V, Vg2 = 1.5 V, on wafer.

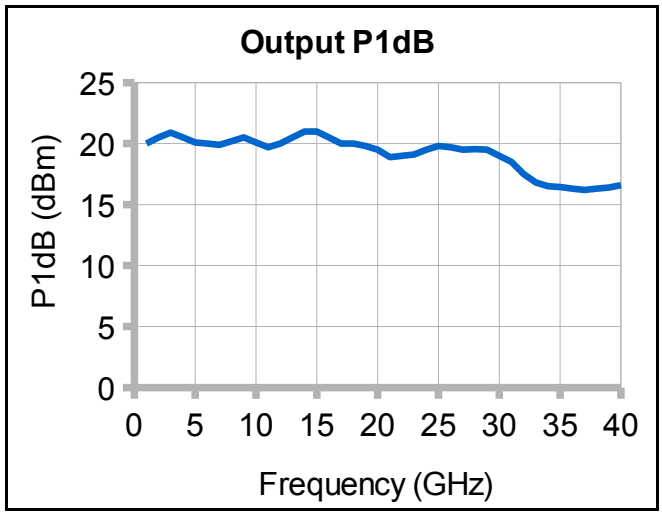












CGY2141UH/C1 TYPICAL SCATTERING PARAMETERS

T_{amb} = 25°C, Vg1 = 0.0 V, Vg2 = 1.5 V, Vdd = +5.0 V, Idd = 180 mA, R_L = 50 Ω.

Frequency (GHz)	Mag S11	Ang S11 (°)	Mag S21	Ang S21 (°)	Mag S12	Ang S12 (°)	Mag (S22)	Ang S22 (°)
0.1	0.132	-179	6.346	-178	0.0002	91.5	0.074	56.4
1	0.140	-172	6.317	160	0.0005	79.2	0.130	-66.8
3	0.166	-164	6.279	138	0.0016	67.7	0.017	43.2
5	0.211	-163	6.294	113	0.0028	49.5	0.064	29.9
7	0.254	-171	6.194	86.7	0.0039	28.6	0.091	16.3
9	0.282	178	6.109	61	0.0051	11.6	0.115	-1.29
11	0.285	165	6.068	35	0.0061	-10.5	0.120	-14.2
13	0.260	153	6.046	9.27	0.0072	-27.6	0.125	-27.1
15	0.214	144	6.109	-16.3	0.0082	-44.2	0.123	-40.5
17	0.155	143	6.168	-42.8	0.0112	-63.1	0.114	-43.5
19	0.125	172	6.298	-70.5	0.0133	-93.4	0.112	-55.4
21	0.193	-176	6.207	-98.3	0.0132	-110	0.092	-49
23	0.269	176	6.251	-125	0.0164	-124	0.1	-34.1
25	0.326	163	6.207	-153	0.0195	-151	0.122	-41.2
27	0.352	146	6.284	179	0.0224	-177	0.133	-45.2
29	0.326	127	6.317	151	0.0266	158	0.141	-52.5
31	0.243	114	6.406	121	0.0299	136	0.140	-60.9
33	0.130	134	6.709	89.6	0.0355	107	0.141	-71.3
35	0.260	166	6.728	56.3	0.0394	77.5	0.1	-88.8
36	0.348	158	6.571	38.3	0.0412	57.9	0.069	-97
37	0.421	149	6.416	21.6	0.0380	45.7	0.034	-74.6
38	0.471	137	6.232	5.13	0.0422	33.1	0.035	-12.6
39	0.502	125	6.001	-11.5	0.0432	12.7	0.074	6.85
40	0.502	112	5.873	-28.3	0.0427	1	0.125	1.17
41	0.461	100	5.720	-44.1	0.0457	-13.3	0.166	-10.8
42	0.385	90.7	5.675	-62	0.0462	-32.4	0.204	-22.7
42.5	0.335	88.6	5.704	-71.4	0.0479	-43	0.219	-30.3
43	0.275	92.2	5.391	-81.9	0.0468	-49.9	0.229	-38.8
43.5	0.243	104	5.400	-91.8	0.0507	-58.6	0.237	-48
44	0.257	117	5.198	-101	0.0525	-72.2	0.234	-58.1
44.5	0.302	125	5.033	-111	0.0537	-84.2	0.219	-68.6
45	0.371	126	4.914	-123	0.0531	-97	0.202	-77.9
45.5	0.435	123	4.560	-132	0.0479	-109	0.174	-88.4
46	0.478	118	4.304	-141	0.0484	-118	0.143	-100
46.5	0.524	113	3.917	-149	0.0442	-127	0.105	-108
47	0.550	108	3.866	-157	0.0442	-138	0.074	-115
47.5	0.565	101	3.588	-167	0.0452	-150	0.042	-119
48	0.568	95.6	3.309	-176	0.0412	-160	0.004	-84.9
48.5	0.557	90.3	3.150	178	0.0394	-169	0.018	48.3
49	0.551	86.4	3.189	171	0.0359	-174	0.046	33.3
49.5	0.512	83.3	2.923	157	0.0412	174	0.072	36.3
50	0.483	83.9	2.626	150	0.0367	161	0.1	27.4

APPLICATION INFORMATION

Typical application scheme

Two module layouts are proposed in figure 1 and 2. In figure 1, RF input and output accesses are built in microstrip transmission line. While in figure 2, coplanar transmission line are used and will give similar performance. All path lengths and physical sizes of the components should be minimized.

All RF input and output bonding inductances should be minimized to give the best performance of the driver module. Two gold wires are recommended with maximum separation between the wires. Overall wire length should be kept less than 0.4 mm to keep lead inductance to less than 0.2 nH. Wedge-Wedge bonding is highly recommended for this purpose. Degradation of gain and match will be evident at higher RF input/output inductance. Ribbon bonding technique can also be used.

All others bonding inductances (pads Vdd1, Vdd2, Vg1, Vg2) should be kept as short as possible.

In figure 1 and figure 2, C1, C2 (47 pF) and C3, C4 (100 nF) capacitors are used to improve the power supply rejection, while C5 (100 nF) is used for low frequency gain extension. C6 is a link capacitor used to isolate the amplifier from external circuitry. C6 (100 nF) will give a low frequency cut-off down to a few kHz.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn or silver conductive epoxy material can be used for die attachment.

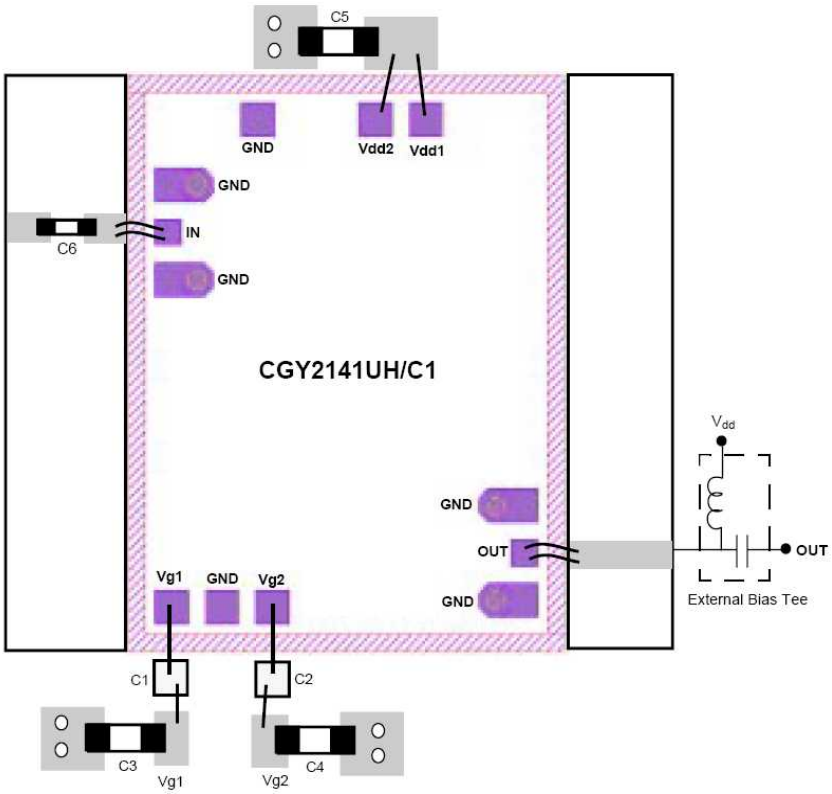


Figure 1: *CGY2141UH/C1 module layout : microstrip assembly*

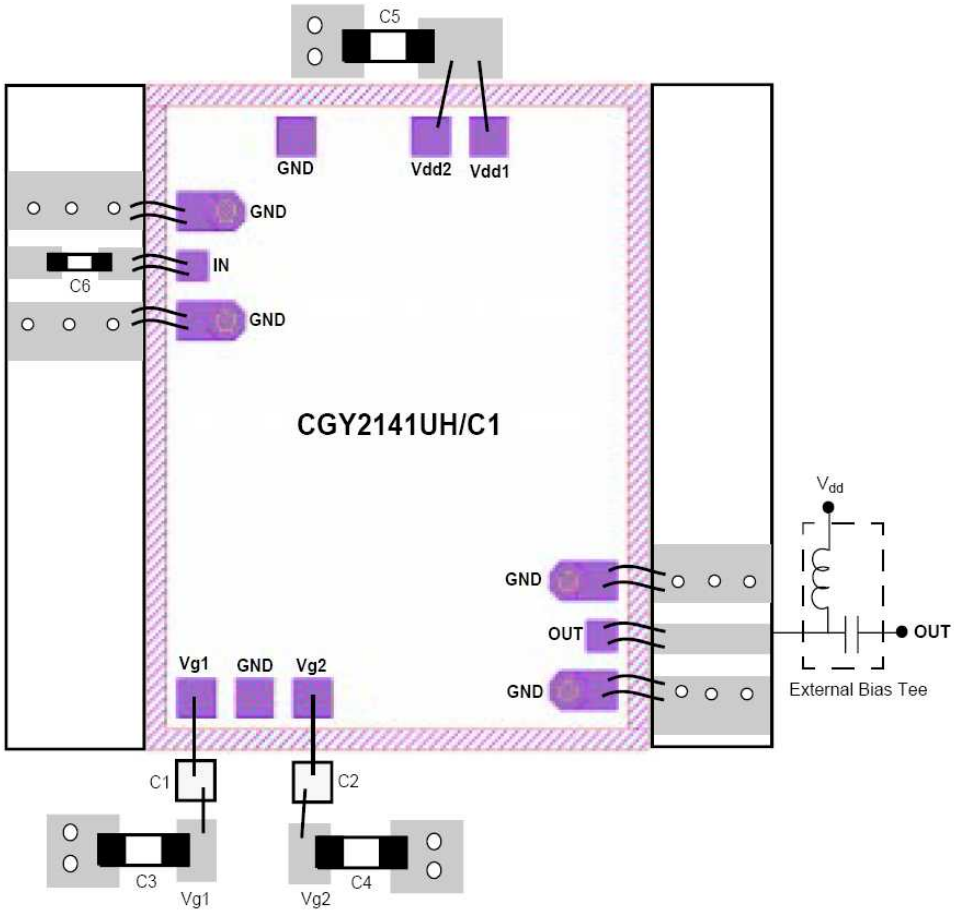


***Figure 2**: CGY2141UH/C1 module layout : coplanar assembly*

OPERATING AND HANDLING INSTRUCTIONS

The CGY2141UH/C1 is a very high performance GaAs device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

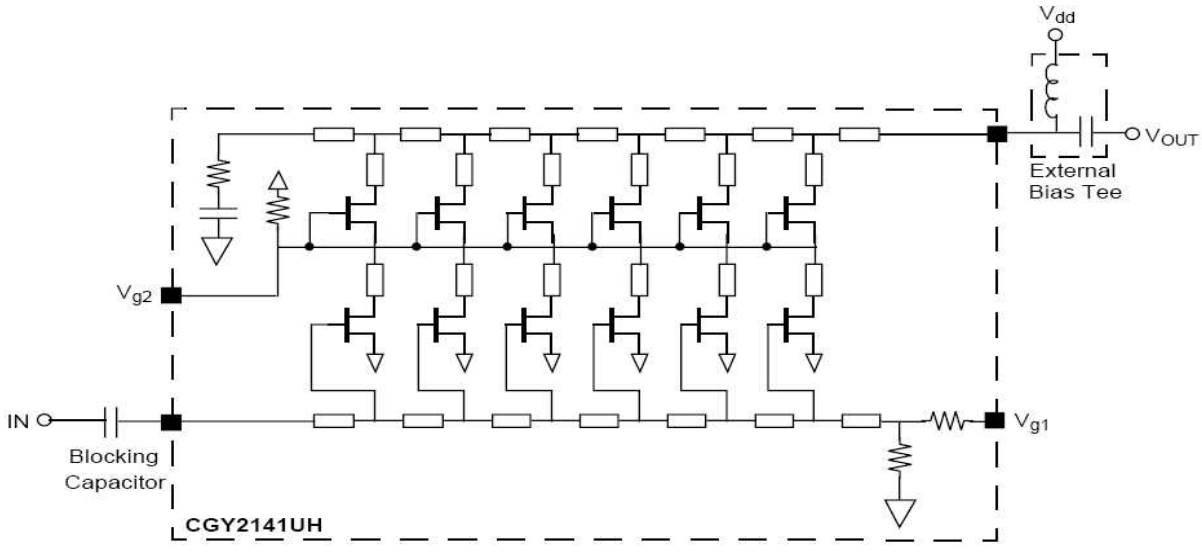
The following power supply sequence is recommended.

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting V_{g1} to –4.5 V and V_{g2} to 0.0 V.
c) Increase V_{dd} = 5.0 V while monitoring the drain current.
d) Increase V_{g2} to 1.5 V
e) Increase V_{g1} slowly from –4.5 V until the drain current reaches 180 mA.
f) Apply the RF input signal.

2- Mounting and ESD handling precautions

For high performance Integrated Circuits, such as the CGY2141UH/C1, care must be taken when mounting GaAs MMICs so as to correctly mount, bond and subsequently seal the packages and hence obtain the most reliable long-term operation. The temperature, duration, material and sealing techniques compatible with GaAs MMICs and the precautions to be taken are described in OMMIC's document "OMCI-MV/001/PG", entitled, "Precautions for III-V users".

BLOCK DIAGRAM AND PAD CONFIGURATION



Block Diagram of the CGY2141UH/C1

PAD POSITION

SYMBOL	PAD	COORDINATES (1)		DESCRIPTION
		Y	X	
GND	1	1365	115	Connected to ground with on-chip via hole
IN	2	1225	115	RF input, used to connect V_{DD} via bias Tee
GND	3	1085	115	Connected to ground with on-chip via hole
Vg1	4	115	115	Gate supply voltage 1, must be decoupled to ground using external capacitor(s)
GND	5	115	265	Connected to ground with on-chip via holes
Vg2	6	115	415	Gate supply voltage 2, must be decoupled to ground using external capacitor(s)
GND	7	135	1155	Connected to ground with on-chip via hole
OUT	8	275	1155	RF output
GND	9	415	1155	Connected to ground with on-chip via hole
Vdd2	10	1555	875	Drain low frequency extension pad 1, must be decoupled to ground using external capacitor(s)
Vdd1	11	1555	735	Drain low frequency extension pad 2, must be decoupled to ground using external capacitor(s)
GND	12	1555	375	Connected to ground with on-chip via hole

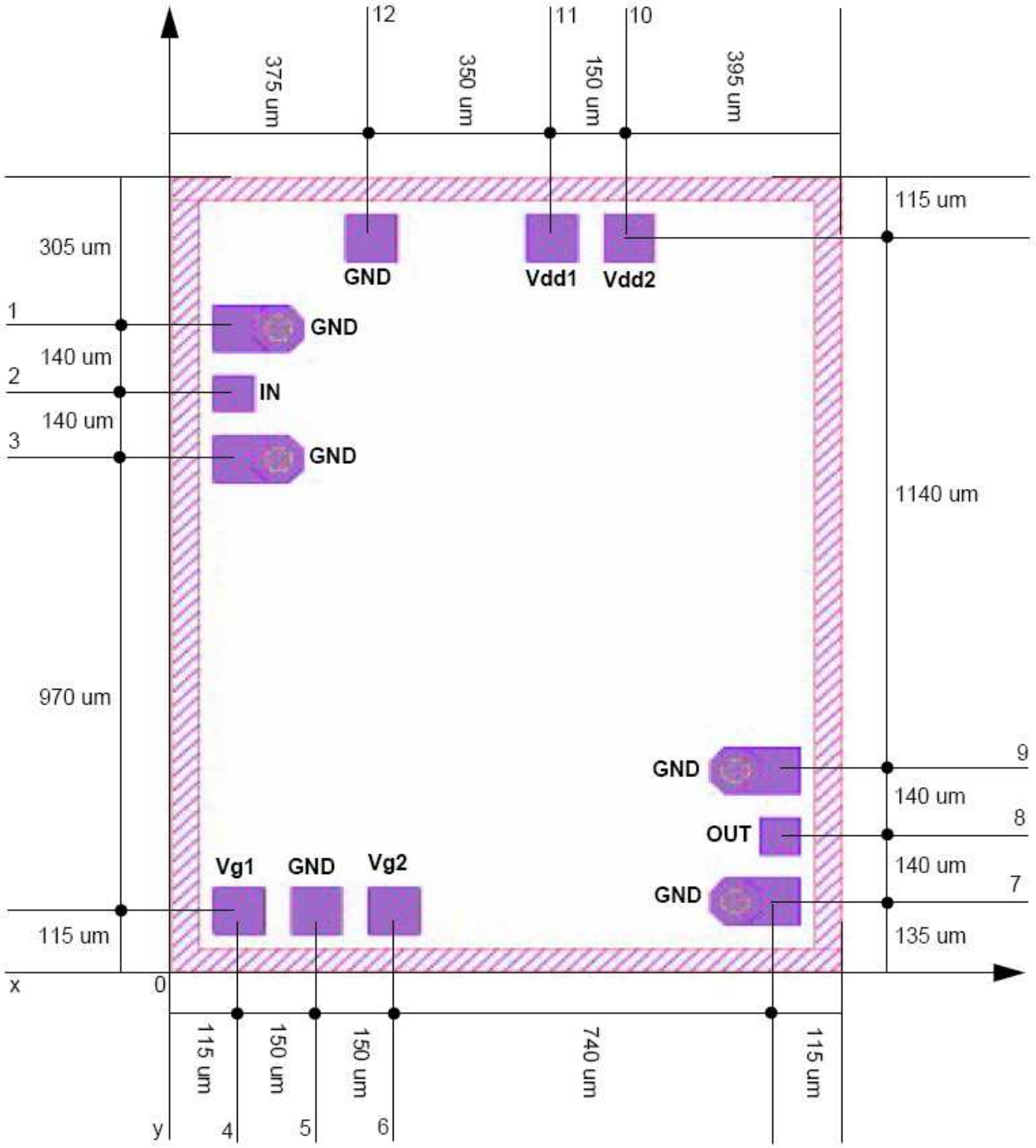
NOTE

1-All x and y coordinates in µm represent the position of the centre of the pad with respect to the lower left corner of the chip layout (see the bonding pattern).

MECHANICAL INFORMATION

PARAMETER		VALUE
Size		1670 x 1270 µm (Tolerance : +/- 15 µm)
Thickness		100 µm
Backside material		TiAu
Passivation		PECVD deposited Si_3N_4
Bonding pad dimensions	GND, Vdd1, Vdd2, Vg1, Vg2	100 x 100 µm
	IN, OUT	90 x 90 µm

BONDING PADS



CGY2141UH/C1 bonding pattern

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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ORDERING INFORMATION

Generic type	Package type	Version	Description
CGY2141UH	Bare Die	C1	InGaAs Semi-conductor die. External dimensions : 1670 x 1270 µm (Tolerance : ±15 µm). Die thickness: 0.1 mm. Backside material: TiAu

RoHS Compliant

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OMMIC
2, chemin du Moulin – BP. 11 – 94453
Limeil-Brévannes France
Information@ommic