PRELIMINARY DATASHEET

CGY2132UH

1W 37-41 GHz High Power Amplifier

DESCRIPTION

The CGY2132UH is a PHEMT GaAs Power Amplifier with output power of 30dBm (1W) and more than 20dB of gain covering frequencies from 37 to 41 GHz.

The CGY2132UH is a 3 stage dual line-up architecture with lange couplers for power combining and excellent input and output matching.

The 1dB Compression point is 28.5 dBm with excellent linearity delivering OIP3 at 37 dBm. DC power supply is 4.5V and PAE 14%.

The CGY2132UH is manufactured using the D01PH GaAs PHEMT power process from OMMIC. This process has a 130nm gate length with a Ft 110Ghz and a Fmax of 180GHz.

The D01PH process used to manufacture the MMIC has been evaluated by ESA and is present in the EPPL (European Preferred Part List). This very reliable process is suitable to manufacture power amplifiers dedicated to flight models in aerospace applications as well as power amplifier for terrestrial applications.

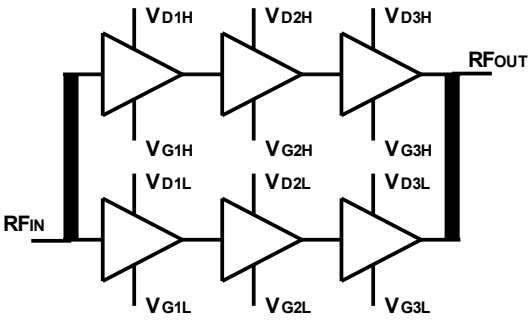
APPLICATIONS

- High performance GaAs High Power Amplifier
- Earth-to-space or point-to-point radiolinks
- Backhaul networks
- Telecommunications

FEATURES

- Usable frequency range from 37 to 41 GHz
- Psat > 1W (+ 30dBm)
- P1dB ~ 28.5 dBm
- Gain ~ 20 dB
- 50 Ohms input and output matched
- Input and Output Return Loss better than -10dB
- Uses a highly reliable PHEMT MMIC process
- Delivered as 100 % on-wafer RF tested dies
- Samples and evaluation Boards Available
- Die size is 3.86 x 2.88 mm

The MMIC is available in the die form, OMMIC can deliver packaged version of the component.



CGY2132UH High Power Amplifier Block Diagram

RoHS Compliant

MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1H}, V_{G2H}, V_{G3H}, V_{G1L}, V_{G2L}, V_{G3L}	Gate voltage		- 2.5	0	V
V_{D1H}, V_{D2H}, V_{D3H}, V_{D1L}, V_{D2L}, V_{D3L}	Drain voltage		0	+ 6	V
I_{D1H}, I_{D1L}	Drain Current			200	mA
I_{D2H}, I_{D2L}				400	
I_{D3H}, I_{D3L}				600	
$I_{GNH,L}$ (all gates)	Gate Current		- 1	+ 1	mA
P_{IN}	Input power			+ 10	dBm
T_{amb}	Ambient temperature		- 40	+ 85	° C
T_j	Junction temperature			+ 175	° C
T_{stg}	Storage temperature		- 55	+ 85	° C

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j\ -\ amb)}$	Thermal resistance from junction to ambient (DC at T_{amb} max)	TBD	° C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RF_{in}	Input frequency		37		41	GHz
Performances on Reference Board at f_i = 39 GHz						
$V_{D1H,\ D2H,\ D3H}$ $V_{D1L,\ D2L,\ D3L}$	Supply voltage			+ 4,5		V
I_{DD}	Total supply current @Psat	All gates at V_G = -0,2V		1450		mA
G	Gain	All gates at V_G = -0,2V		20		dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point	All gates at V_G = -0,2V		+ 28.5		dBm
Psat	Saturated power	All gates at V_G = -0,2V	,	+ 30		dBm
PAE	Power Added Efficiency			14		%
OIP3	Output third order intercept point	I_{D3L} = I_{D3U} = 280 mA		+ 37		dBm
IMD3	2 Carriers 14 dB below P1dB			- 44		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT} / RF_{IN}		- 40		dB
S_{11}	Input reflection coefficient	50 Ohms		- 14		dB
S_{22}	Output reflection coefficient	50 Ohms		- 14		dB
P_{OFF}	Leakage when HPA off All gates = -2,5V	RF_{IN} = + 10dBm		- 30		dBm

(*) Measurement reference planes are the INPUT and OUTPUT coaxial connectors.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

On-Wafer measurements is the standard way of performing device testing but have inherently poor thermal conditions. Tests are performed under full biasing conditions and CW operation which combined with poor thermal conditions give a lower gain and P1dB compared to the MMIC's real performances with a good thermal heatsink..

S-PARAMETERS (SMITH CHARTS)

Conditions : $V_{D1H, D1L}$ = $V_{D2H, D2L}$ = $V_{D3H, D3L}$ = 4.5V, $V_{G1H, G1L}$ = $V_{G2H, G2L}$ = $V_{G3H, G3L}$ = -0.2V, ($I_{DQ1H, DQ1L}$ = 100mA, $I_{DQ2H, DQ2L}$ = 200mA, $I_{DQ3H, DQ3L}$ = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)

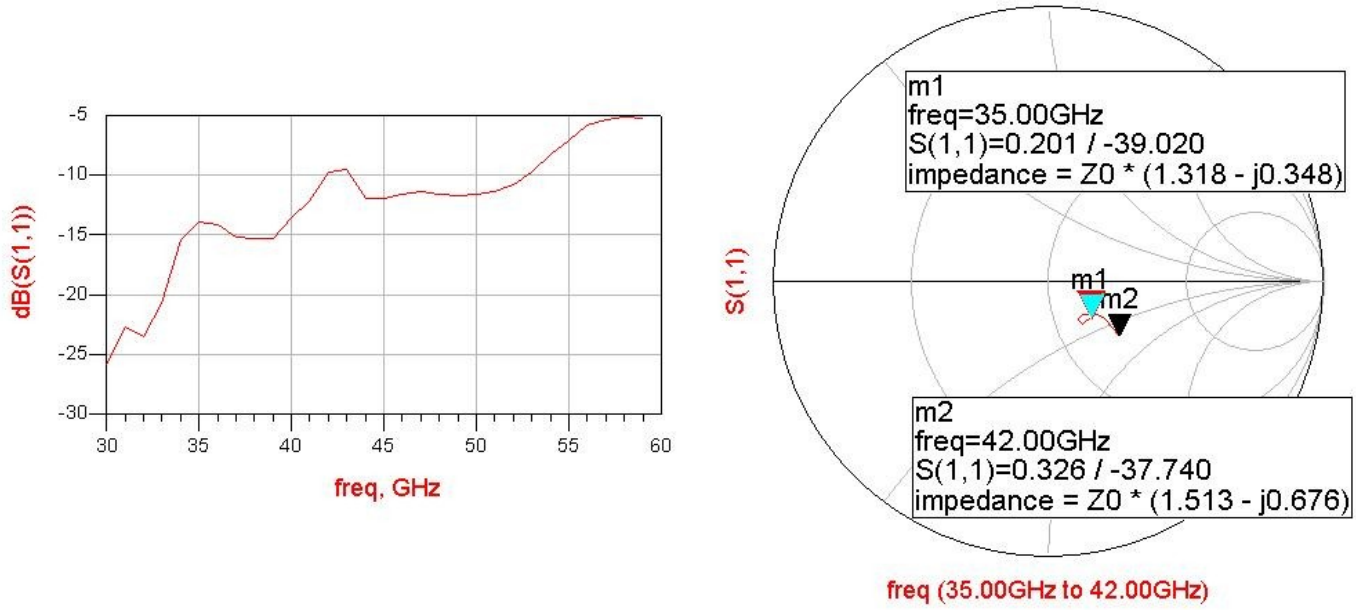


Figure 1: S11 On-Wafer measurements

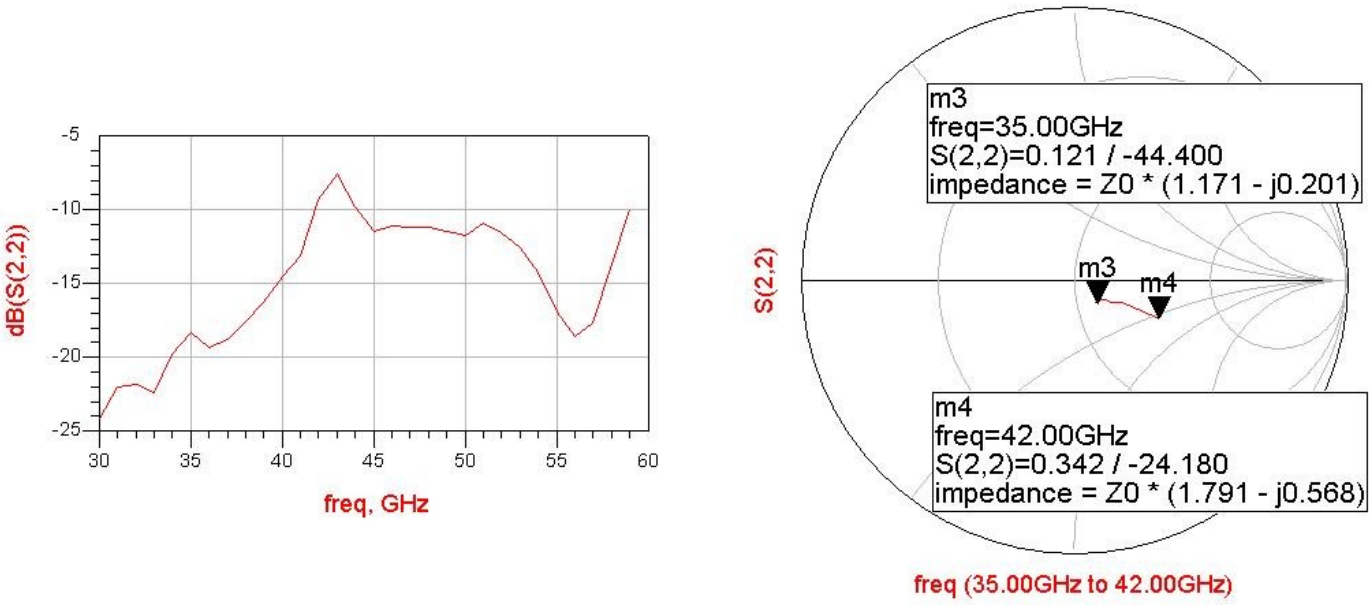


Figure 2: S22 On-Wafer measurements

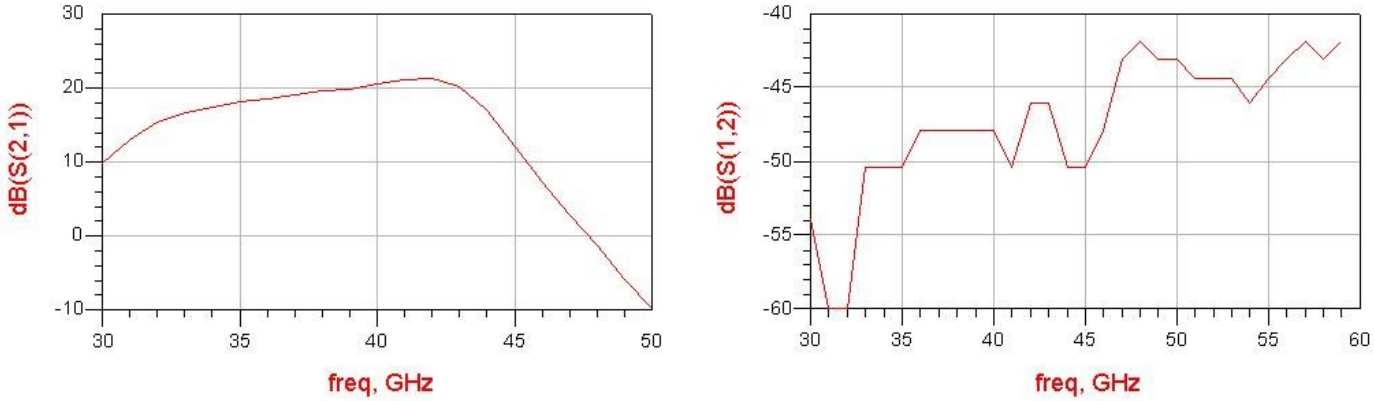


Figure 3: Gain and reverse isolation On-Wafer measurements

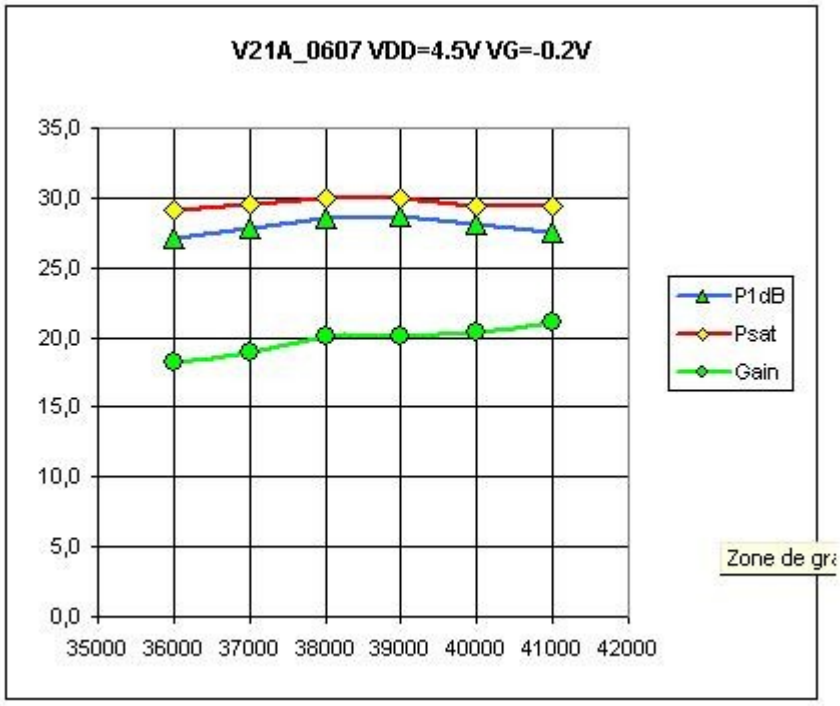
S PARAMETERS (TABLE)

Conditions : $V_{D1H, D1L} = V_{D2H, D2L} = V_{D3H, D3L} = 4.5V$, $V_{G1H, G1L} = V_{G2H, G2L} = V_{G3H, G3L} = -0.2V$, ($I_{DQ1H, DQ1L}$ = 100mA, $I_{DQ2H, DQ2L}$ = 200mA, $I_{DQ3H, DQ3L}$ = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)

GHz	|S11|	S11 Phase	|S21|	S21 Phase	|S12|	S12 Phase	|S22|	S22 Phase
30	0.051	-7.2	3.121	-160.3	0.002	-147.7	0.062	-36.9
31	0.073	-25.7	4.411	160.2	0.001	116.5	0.079	-34.2
32	0.067	-30.9	5.868	113.6	0.001	-13.8	0.081	-43.1
33	0.092	-3.6	6.839	64.4	0.003	-64.0	0.076	-35.6
34	0.169	-22.0	7.430	17.9	0.003	-116.0	0.102	-33.5
35	0.201	-39.0	8.072	-28.8	0.003	-156.3	0.121	-44.4
36	0.197	-51.7	8.414	-73.2	0.004	160.6	0.108	-45.6
37	0.175	-52.0	8.943	-116.2	0.004	103.0	0.115	-37.4
38	0.171	-51.2	9.638	-164.1	0.004	69.5	0.132	-30.1
39	0.171	-43.5	9.863	149.0	0.004	15.5	0.153	-30.7
40	0.210	-33.6	10.703	100.6	0.004	-31.1	0.188	-24.4
41	0.245	-33.3	11.376	47.4	0.003	-55.4	0.219	-24.5
42	0.326	-37.7	11.668	-12.1	0.005	-97.0	0.342	-24.2
43	0.334	-60.1	10.174	-80.5	0.005	-145.3	0.416	-53.5
44	0.252	-62.3	7.071	-148.2	0.003	160.4	0.324	-66.2
45	0.254	-53.8	4.050	153.8	0.003	179.3	0.268	-64.1
46	0.264	-52.4	2.289	108.5	0.004	-169.9	0.278	-62.2
47	0.271	-53.6	1.394	67.1	0.007	144.7	0.277	-61.2
48	0.262	-53.9	0.857	30.3	0.008	105.5	0.275	-64.7
49	0.261	-53.4	0.512	-7.5	0.007	83.9	0.266	-62.2
50	0.262	-51.3	0.324	-42.7	0.007	57.9	0.258	-64.2
51	0.271	-49.3	0.212	-72.4	0.006	45.1	0.284	-64.9
52	0.290	-42.1	0.113	-106.6	0.006	27.1	0.263	-70.9
53	0.328	-41.5	0.085	-109.2	0.006	15.7	0.234	-75.5
54	0.387	-45.8	0.097	175.0	0.005	35.1	0.193	-70.1
55	0.444	-49.2	0.027	-161.7	0.006	20.7	0.143	-60.3
56	0.513	-58.2	0.055	111.3	0.007	-0.5	0.117	-38.8
57	0.541	-72.3	0.062	-63.5	0.008	-8.8	0.131	-11.0
58	0.558	-83.0	0.050	57.5	0.007	-19.5	0.207	7.4
59	0.547	-98.4	0.027	-106.3	0.008	-23.9	0.316	7.098

1DB COMPRESSION POINT, SATURATED POWER AND GAIN

Conditions : $V_{D1H, D1L}$ = $V_{D2H, D2L}$ = $V_{D3H, D3L}$ = 4.5V, $V_{G1H, G1L}$ = $V_{G2H, G2L}$ = $V_{G3H, G3L}$ = -0.2V, ($I_{DQ1H, DQ1L}$ = 100mA, $I_{DQ2H, DQ2L}$ = 200mA, $I_{DQ3H, DQ3L}$ = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)



APPLICATION SCHEMATIC

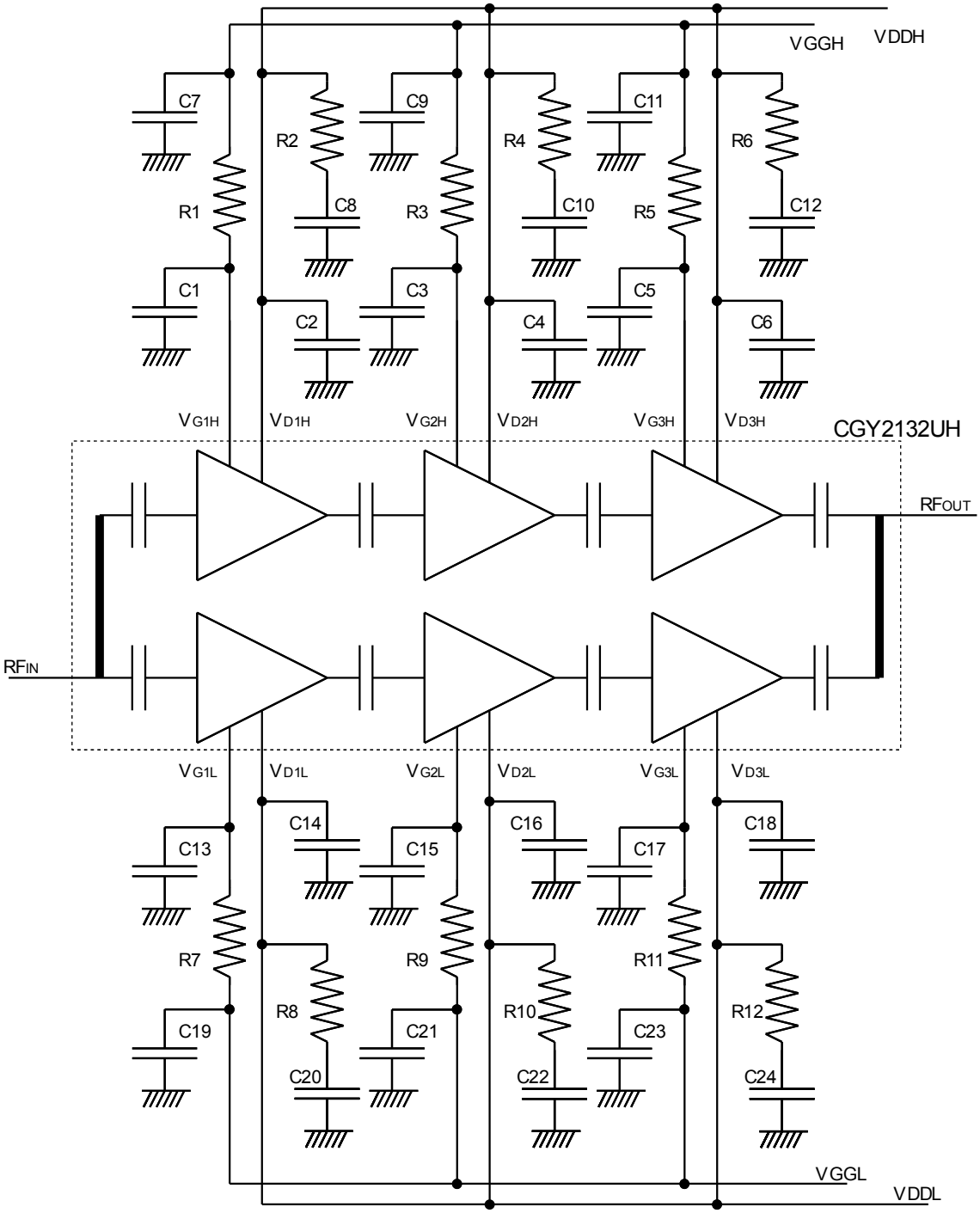


Figure 4: APPLICATION SCHEMATICS

Component NAME	Value	Type	Comment
C1 to C6 C13 to C18	47p	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die, bonding as short as possible
R2,R4,R6 R8,R10,R12	39	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-0739RL

R1,R3,R5 R7,R9,R11	100	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-07100RL
C7 to C12 C19 to C24	100n	SMD 0603 Capacitor	MURATA GRM188R71H104KA93D

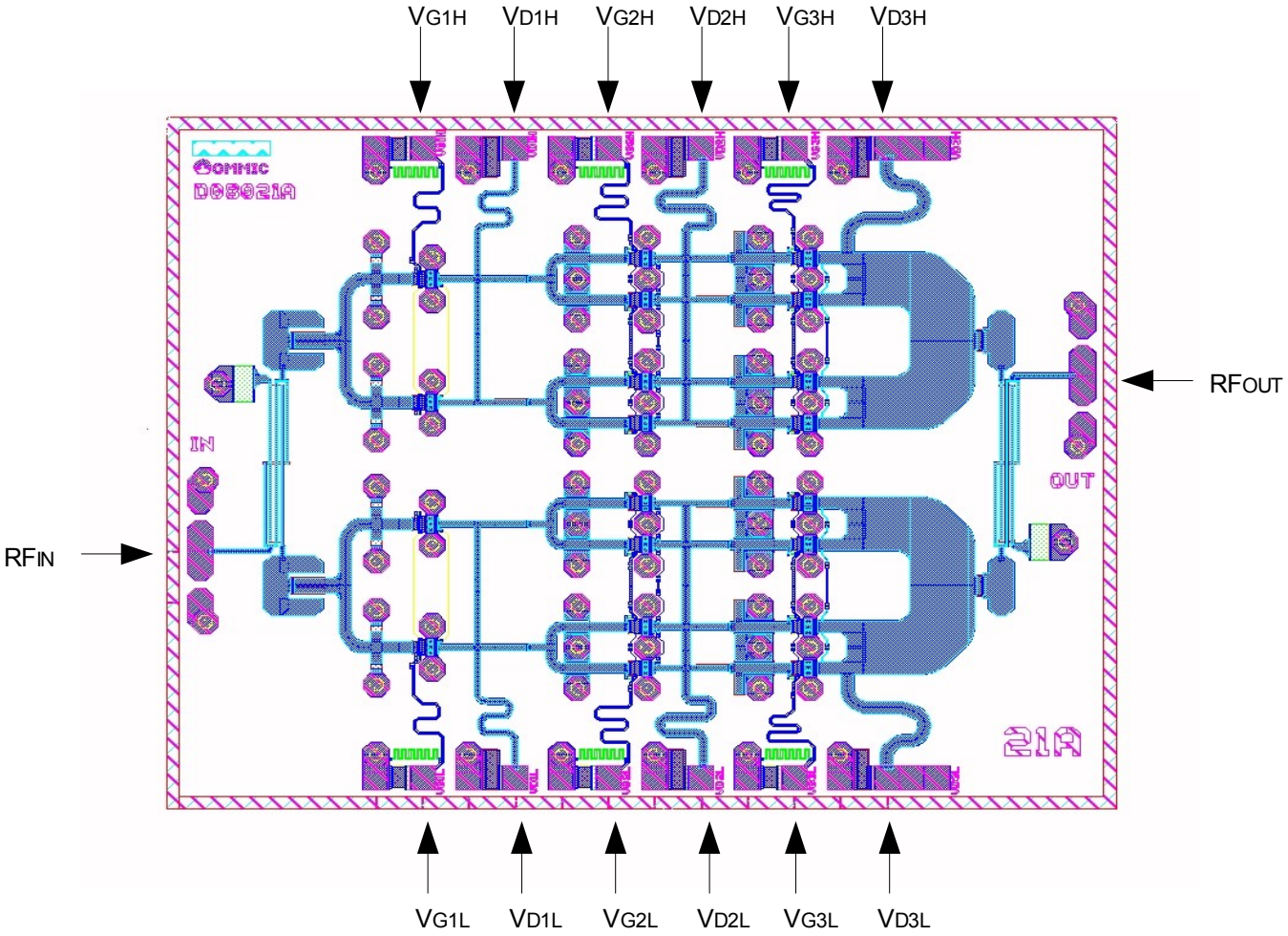
Due to the highly symmetrical design of the component and the requirements of the power combiner, it is recommended to keep V_{G1L} equal to V_{G1H}, V_{G2L} equal to V_{G2H} and V_{G3L} equal to V_{G3H}, for the same reason, it is recommended to keep V_{D1L} equal the V_{D1H}, V_{D2L} equal the V_{D2H} and V_{D3L} equal the V_{D3H}.

In order to save DC power consumption and improve PAE each gate can be individually driven at a different bias voltage. In this case, when using the targeted RF signal (modulated carrier), the distortion is monitored while adjusting V_{G1L}, V_{G2L}, V_{G3L}, V_{G1H}, V_{G2H} and V_{G3H}. The global strategy is to introduce all the distortion allowed by the targeted standard in the last stage of the amplifier by adjusting V_{G3L}, V_{G3H} while V_{G1L}, V_{G1H} and V_{G2L}, V_{G2H} are positioned in such a way that I_{D2L}, I_{D2H} and I_{D1L}, I_{D1H} are kept at the minimum value corresponding to a neglectable contribution to the global distortion.

An additional amount of DC power supply can be saved in fine tuning the drain voltages V_{D1L},V_{D2L}, V_{D3L}, V_{D1H}, V_{D2H} and V_{D3H} while following the same procedure and the same strategy as described above.

In order to validate each stage of the amplifier, with respect to the DC, it is recommended to set V_{GNL} or V_{GNH} to -2.5V, then to set first the corresponding drain voltage V_{DNL} or V_{DNH} to +1V and check that the corresponding I_{DNL} or I_{DNH} drain current stay a a very low level, after that verification, V_{DNL} or V_{DNH} can be set to 4.5V. When V_{GNL} or V_{GNH} is changed from -2.5 to -0.3V, the corresponding drain current I_{DNL} or I_{DNH} increases slowly in a controlled manner to reach the typical targeted value.

DIE LAYOUT AND PIN CONFIGURATION



It is hightly recommended to place a 47pF RF decoupling chip capacitor C1-C6 and C13-C18 at each DC terminal with as short as possible bonding wires. Additionnaly for power up, prior to applying drain voltage, gates voltages should be preset to -1,5 V. After applying the drain voltage, transistors should be activited (gate positionned in the -0.3V to 0V range) from the third stage to the first. On shut down, reverse order operation should be performed.

PINOUT

Symbol	Pad	Description
RF_{OUT}	OUT	RF output
RF_{IN}	IN	RF input
V_{D1H}	VD1H	First stage Drain Upper Line-up
V_{D2H}	VD2H	Second stage Drain Upper Line-up
V_{D3H}	VD3H	Third stage Drain Upper Line-up

V_{G1H}	VG1H	First stage Gate Upper Line-up
V_{G2H}	VG2H	Second stage Gate Upper Line-up
V_{G3H}	VG3H	Third stage Gate Upper Line-up
V_{D1L}	VD1L	First stage Drain Lower Line-up
V_{D2L}	VD2L	Second stage Drain Lower Line-up
V_{D3L}	VD3L	Third stage Drain Lower Line-up
V_{G1L}	VG1L	First stage Gate Lower Line-up
V_{G2L}	VG2L	Second stage Gate Lower Line-up
V_{G3L}	VG3L	Third stage Gate Lower Line-up
GND	BACKSIDE	Ground

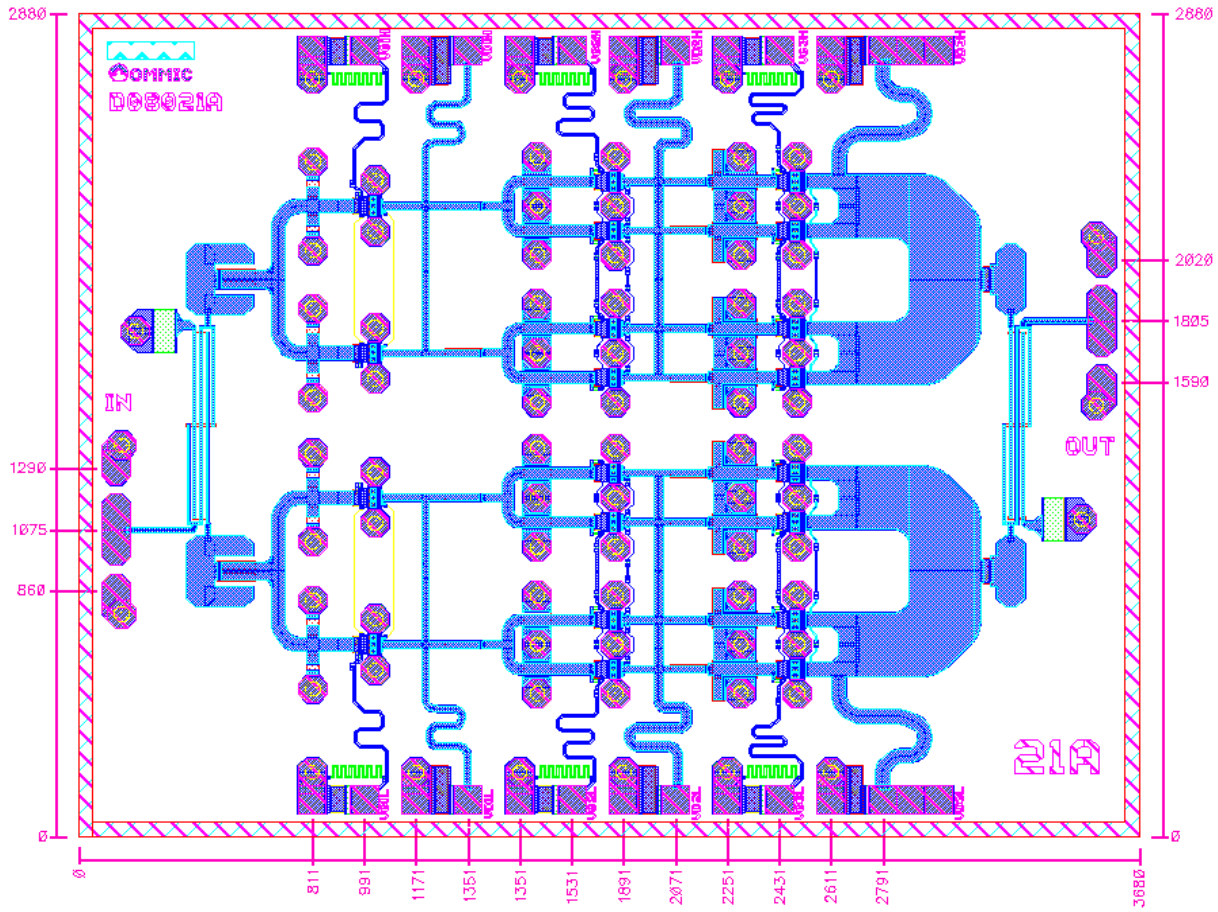
Note :

In order to ensure good RF performances and stability It is key to connected to the ground the pad available on the backside of the die.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on wafer tested	18	-	3.86 x 2.88 x 0.1

BONDING PAD COORDINATES



SOLDERING

During soldering process, to avoid permanent damages or impact on reliability, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400°C

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
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ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2132	UH	C1	-	On-Wafer measured Die

RoHS Compliant

Document History :
Version 1.0, Last Update 26/07/2010
Version 1.1, Demo Board Update 14/09/2011

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