

## 17.0- 23.6GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

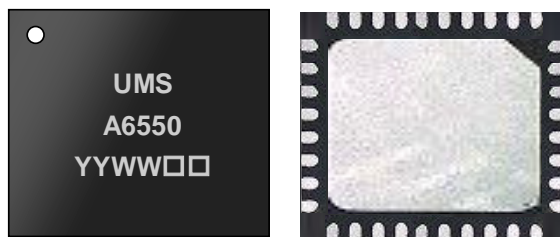
### Description

The CHA6550-QXG is a three stage monolithic GaAs high power circuit producing 2.5 Watt output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included.

It is designed for Point To Point Radio and K band.

The circuit is manufactured with a pHEMT process, 0.15µm gate length.

It is supplied in RoHS compliant SMD package.

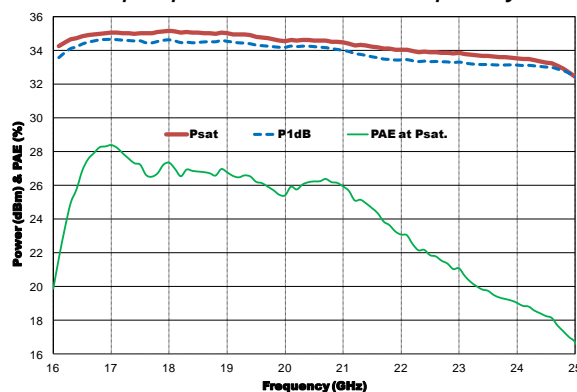


36 lead 6x5 mm QFN package

### Main Features

- Broadband performances: 17.0- 23.6GHz
- 34dBm saturated power
- 41dBm OIP3
- 22dB gain
- DC bias: Vd = 6.0Volt @ Id = 1.3A
- QFN 6x5
- MSL3

Output power & PAE vs frequency



### Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		23.6	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		34		dBm
OIP3	Output IP3		41		dBm

### Electrical Characteristics

T<sub>amb.</sub> = +25°C, V<sub>d</sub> = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17.0		23.6	GHz
Gain	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power		34		dBm
OIP3	Output IP3		41		dBm
PAE	PAE at saturation		20		%
CG	Gain control range		15		dB
R <sub>lin</sub>	Input Return Loss		20		dB
R <sub>lout</sub>	Output Return Loss		20		dB
NF	Noise figure at nominal gain		5		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
V <sub>detect</sub>	Voltage detection V <sub>REF</sub> - V <sub>DET</sub> up to Psat		10 to 1500		mV
V <sub>g</sub>	DC gate Voltage		-0.65		V
I <sub>dq</sub>	Total drain current		1.3		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>amb.</sub> = +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	DC Drain bias voltage without RF	8	V
I <sub>d</sub>	Drain bias quiescent current	1600	mA
V <sub>g</sub>	Gate bias voltage	-2 to 0	V
P <sub>in</sub>	Maximum Input Power	+15	dBm
T <sub>a</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

**Typical Bias Conditions**T<sub>amb.</sub> = +25°C

Symbol	Pad N°	Parameter	Values	Unit
V <sub>d1</sub>	7, 20	DC Drain voltage 1 <sup>st</sup> stage	6.0	V
V <sub>d2</sub>	5, 22	DC Drain voltage 2 <sup>nd</sup> stage	6.0	V
V <sub>d3</sub>	3, 24	DC Drain voltage 3 <sup>rd</sup> stage	6.0	V
V <sub>g1</sub>	8, 19	DC Gate voltage 1 <sup>st</sup> stage	-0.65	V
V <sub>g2</sub>	6, 21	DC Gate voltage 2 <sup>nd</sup> stage	-0.65	V
V <sub>g3</sub>	4, 23	DC Gate voltage 3 <sup>rd</sup> stage	-0.65	V

### Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

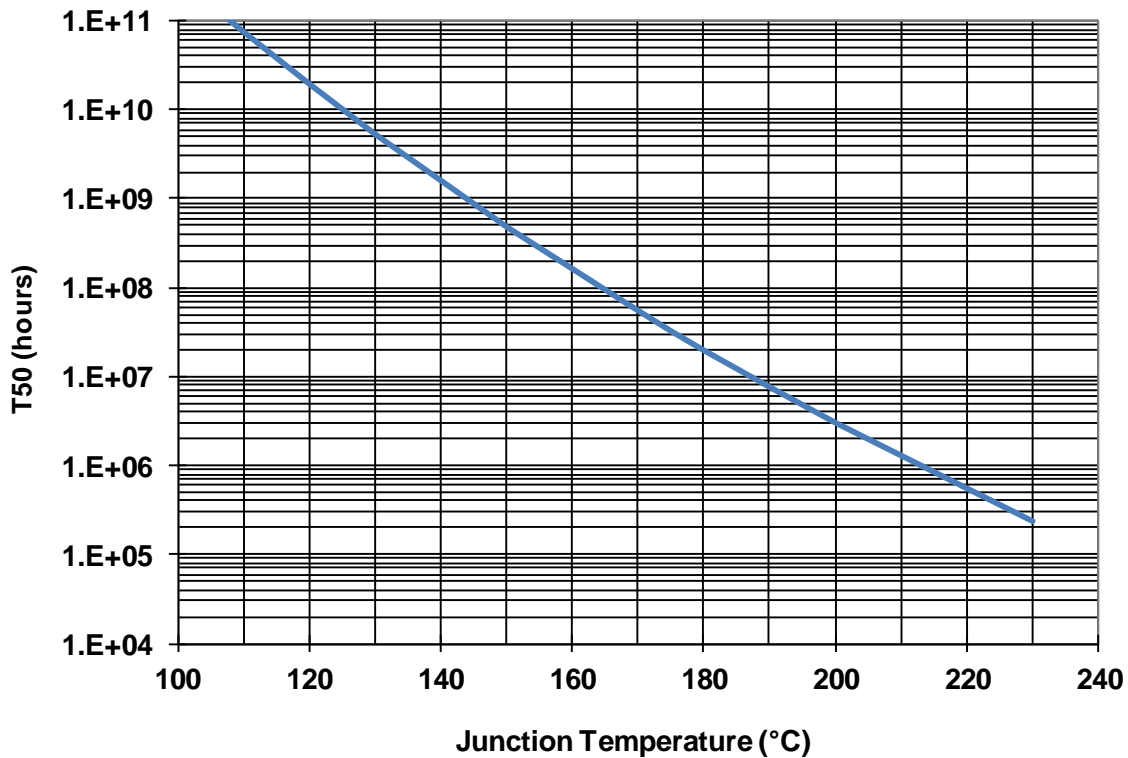
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R <sub>TH</sub> (°C/W)	T50 (hours)
R <sub>TH</sub> <sup>(1)</sup> Thermal Resistance ( Junction to Case)	Vd= 6V Id= 1300mA Pdis= 7.8W	176	11.8	3.0E+07

<sup>(1)</sup> Assuming 85°C Tcase



### Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

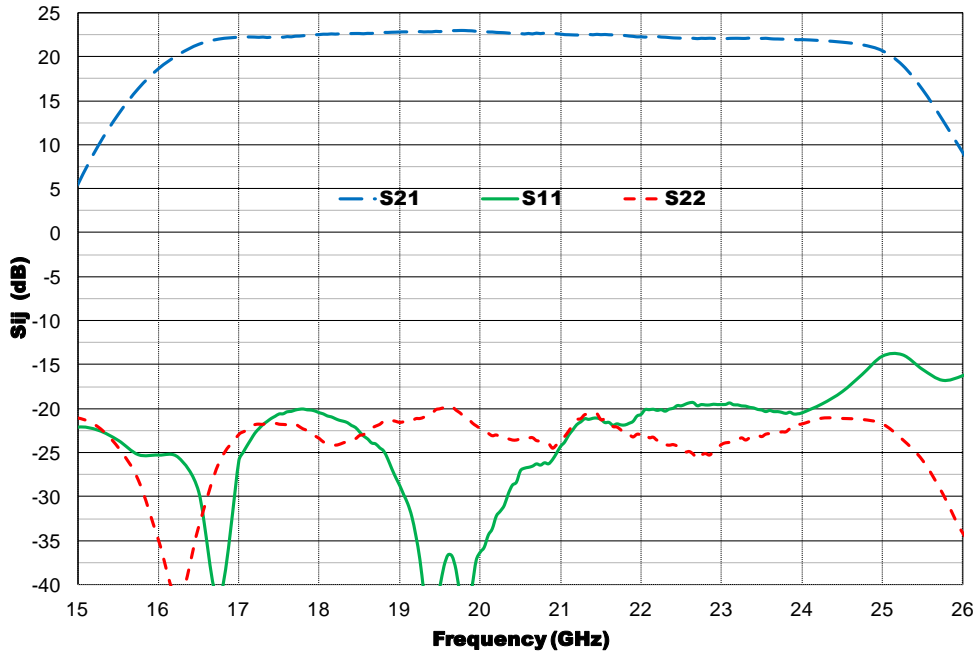
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.304	160.0	-75.785	56.3	-79.553	42.2	-0.230	160.1
2	-0.308	139.7	-75.948	95.0	-75.108	64.0	-0.297	140.0
3	-0.373	119.6	-74.489	16.3	-70.767	26.1	-0.337	119.7
4	-0.437	98.8	-67.950	-4.5	-60.913	0.2	-0.504	98.2
5	-0.519	77.2	-69.162	2.1	-51.149	-84.0	-0.881	77.1
6	-1.027	53.3	-67.392	-25.7	-43.160	154.2	-1.408	55.0
7	-1.811	31.0	-66.872	-41.0	-41.768	36.9	-2.137	34.6
8	-3.271	9.7	-71.237	-78.2	-43.570	-51.0	-2.732	15.1
9	-4.415	-4.9	-74.198	-7.4	-47.323	-113.2	-3.164	-6.8
10	-4.469	-24.6	-65.652	-75.8	-51.087	174.1	-3.625	-31.0
11	-4.964	-53.1	-59.691	-122.6	-56.368	179.1	-4.184	-62.8
12	-6.599	-89.5	-56.495	176.1	-53.701	-156.4	-6.385	-103.6
13	-10.907	-138.7	-56.329	129.2	-49.926	157.3	-12.416	-153.3
14	-25.889	140.3	-54.755	80.3	-19.183	38.3	-37.002	-153.0
15	-22.132	-58.9	-51.362	59.4	5.521	-117.0	-21.083	-116.7
16	-25.304	-78.8	-52.723	32.6	18.654	60.3	-34.920	125.1
17	-25.917	-1.5	-50.015	-5.2	22.240	-108.6	-22.946	48.6
18	-20.489	-74.4	-49.873	-17.9	22.532	119.4	-23.407	-16.9
19	-28.776	-144.8	-51.342	-65.9	22.826	-0.3	-21.584	-18.2
20	-36.351	26.2	-63.966	-94.6	22.913	-115.6	-22.250	-46.8
21	-24.307	19.1	-66.161	-172.2	22.591	133.0	-23.766	-27.1
22	-20.676	-11.7	-56.109	37.0	22.281	21.4	-22.953	-54.1
23	-19.544	-35.0	-46.516	15.8	22.074	-93.3	-24.079	-41.9
24	-20.505	-34.9	-42.581	-18.4	21.959	140.3	-21.761	-54.9
25	-14.051	-40.4	-44.388	-66.6	20.693	-12.5	-21.745	-99.3
26	-16.264	-60.3	-42.833	-62.7	9.106	-175.0	-34.140	-121.1
27	-12.747	-79.5	-40.784	-83.9	-4.465	78.3	-24.001	-67.6
28	-12.841	-111.9	-40.876	-115.4	-16.299	-13.5	-18.580	-119.0
29	-16.677	-131.7	-41.691	-136.5	-26.375	-99.6	-17.218	-170.1
30	-18.642	-88.1	-40.329	-136.7	-34.027	-159.5	-18.410	153.1
31	-10.219	-92.7	-38.587	-150.0	-40.761	-167.0	-17.735	132.2
32	-5.916	-125.3	-39.354	172.7	-41.480	179.0	-15.277	86.5
33	-3.783	-159.2	-41.653	175.0	-40.586	179.8	-12.637	9.4
34	-2.725	169.0	-38.114	157.2	-37.970	156.2	-8.151	-75.3
35	-2.159	140.5	-38.466	121.2	-38.327	121.6	-4.343	-140.1
36	-1.799	114.0	-44.726	108.3	-44.009	102.0	-2.336	172.4
37	-1.456	88.6	-46.802	116.7	-46.033	123.9	-1.248	134.0
38	-1.556	62.3	-45.451	151.0	-45.377	153.8	-0.907	101.1
39	-2.232	36.6	-39.931	138.1	-40.309	135.5	-1.128	71.5
40	-4.809	14.8	-37.979	111.2	-38.528	114.6	-2.077	44.4

## Typical Board Measurements

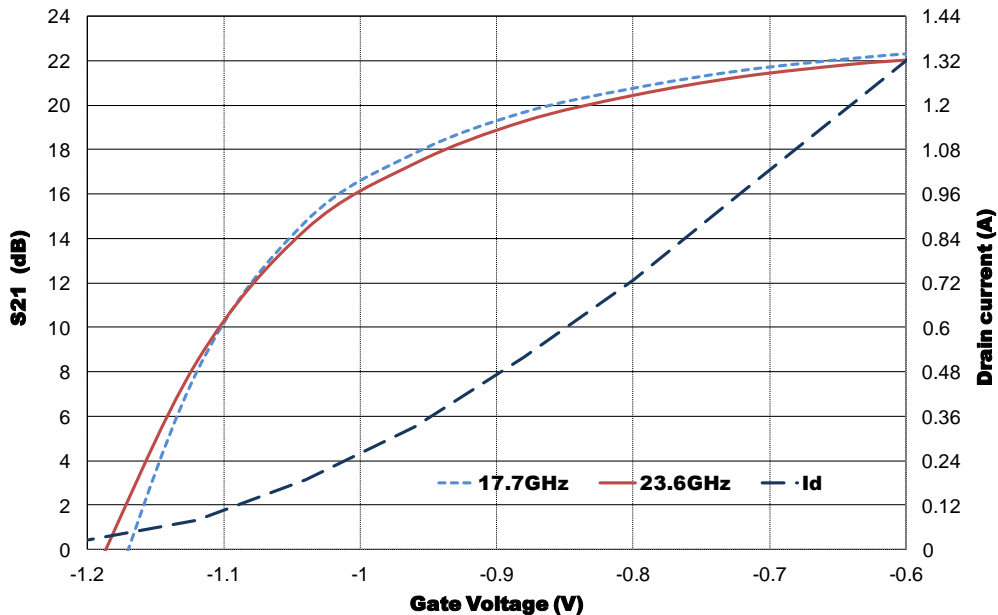
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Measurement performed in the access plans of the QFN, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board"

**Gain & Return Loss versus Frequency**

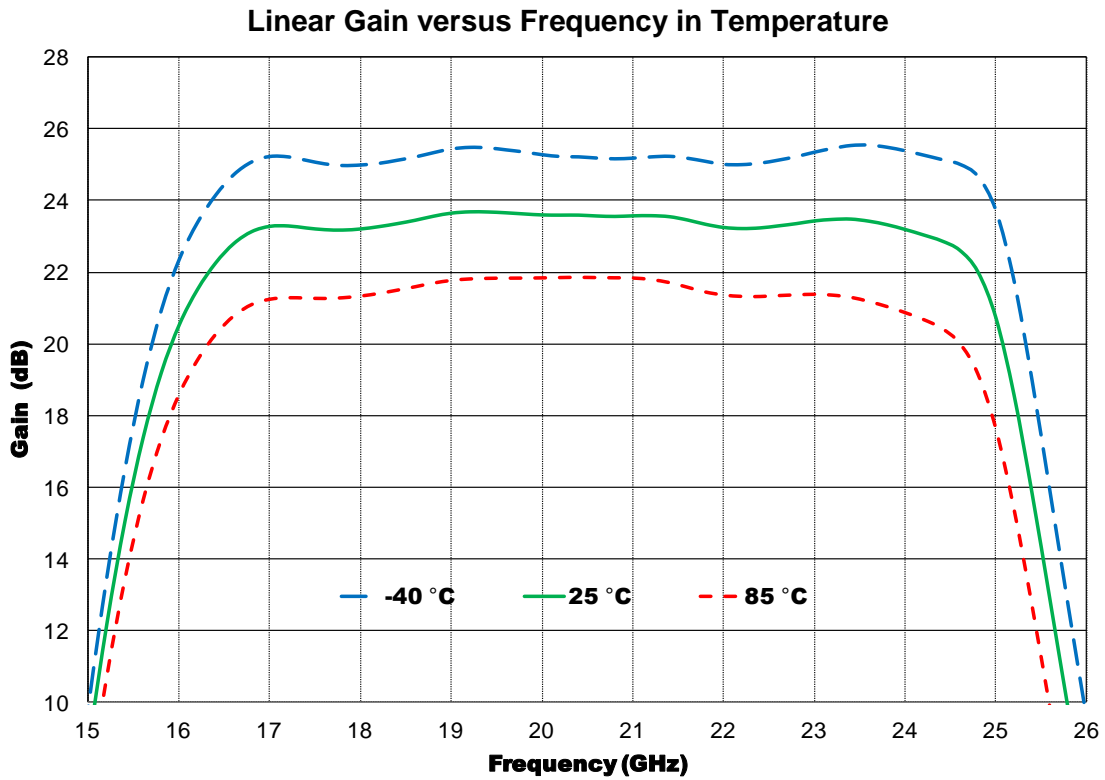
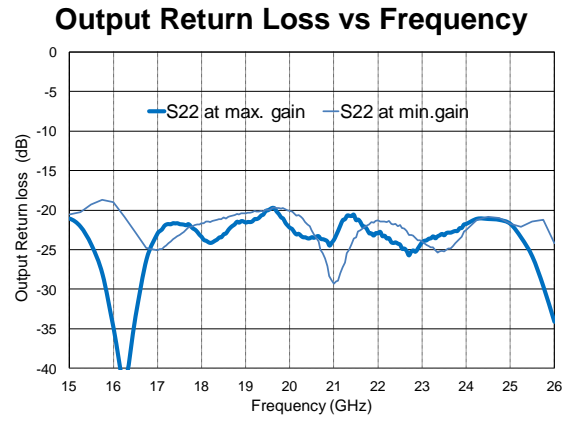
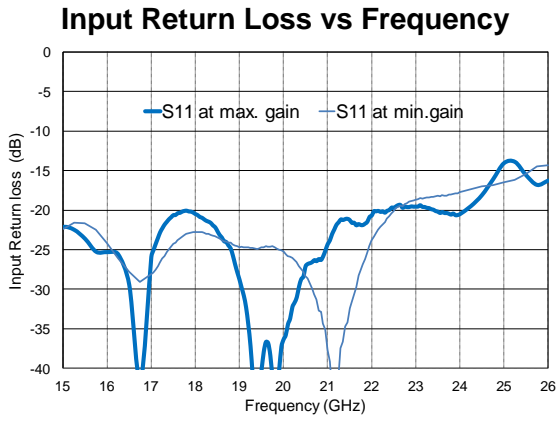


**Gain control & current versus Gate Voltage**



Typical Board Measurements

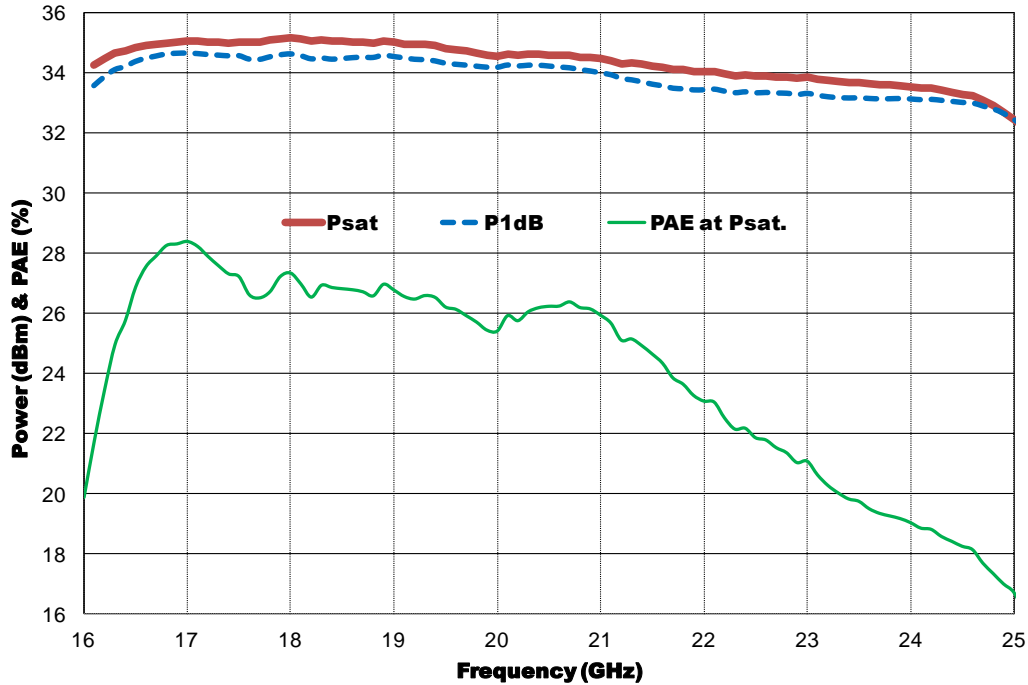
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



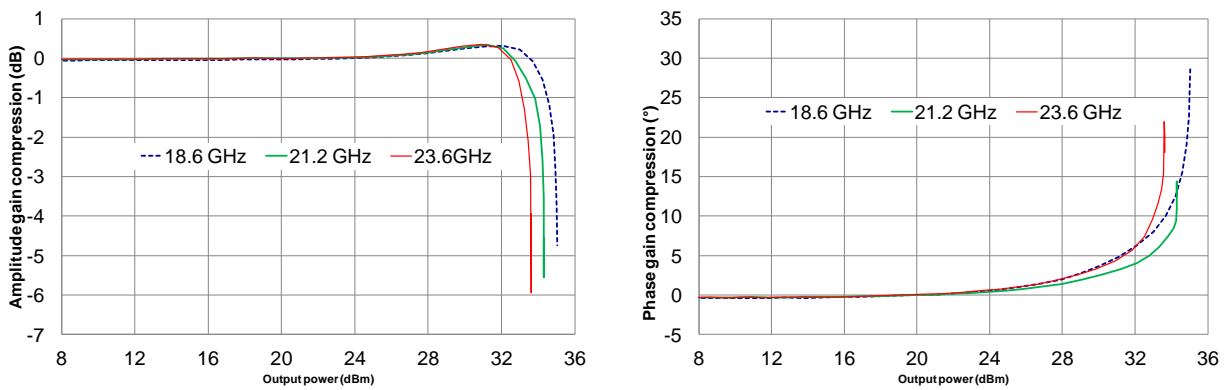
## Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

### Output power & PAE versus Frequency



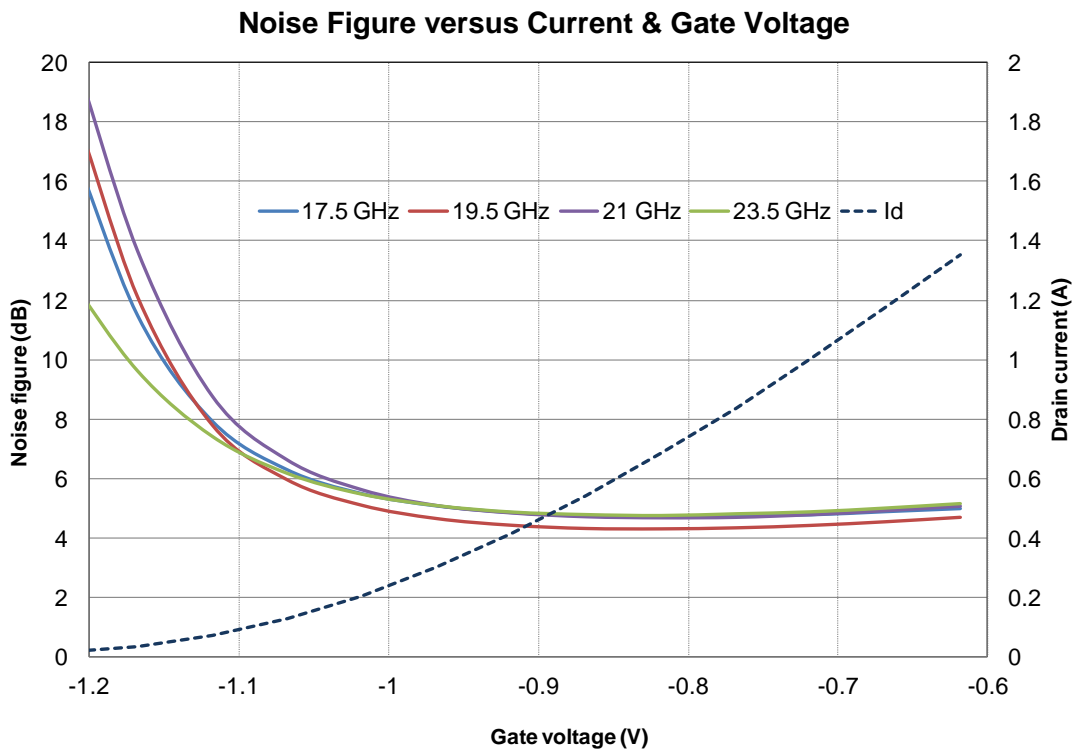
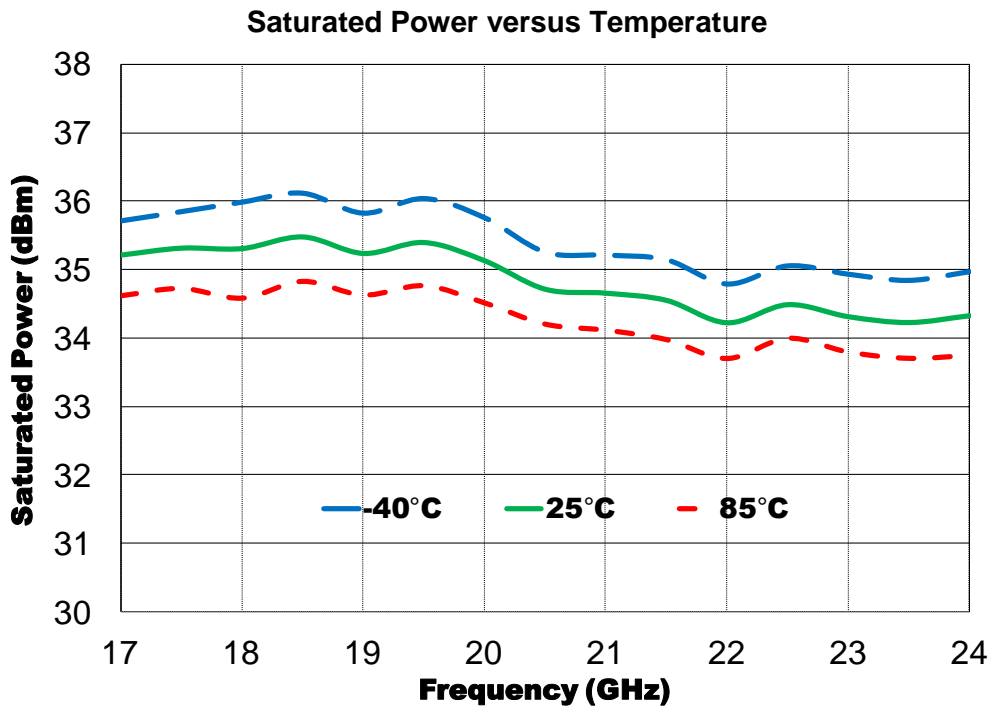
### Amplitude & Phase variation versus Output Power





Typical Board Measurements

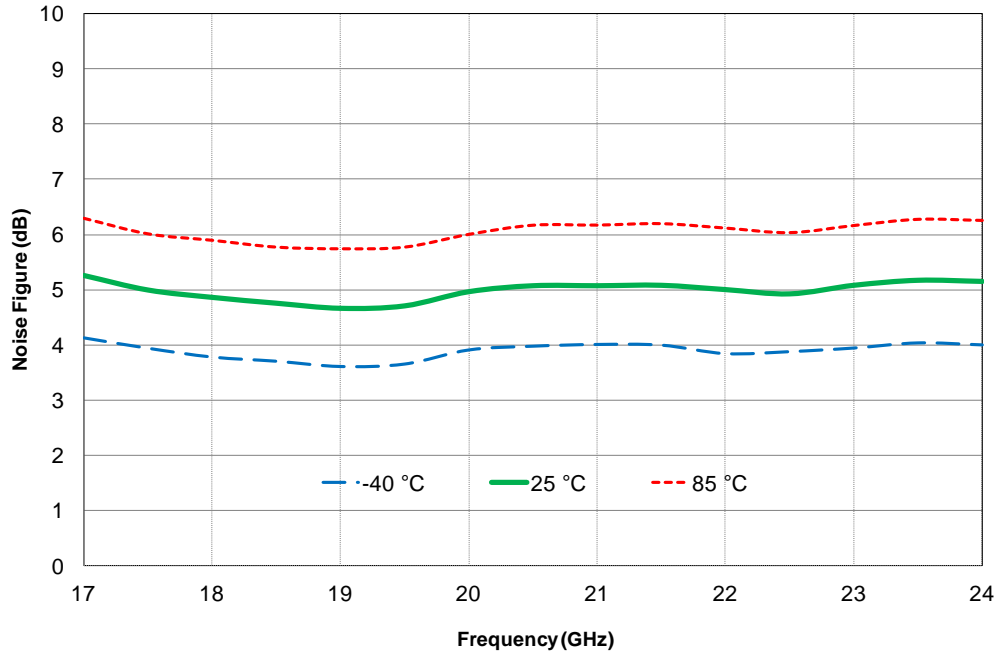
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



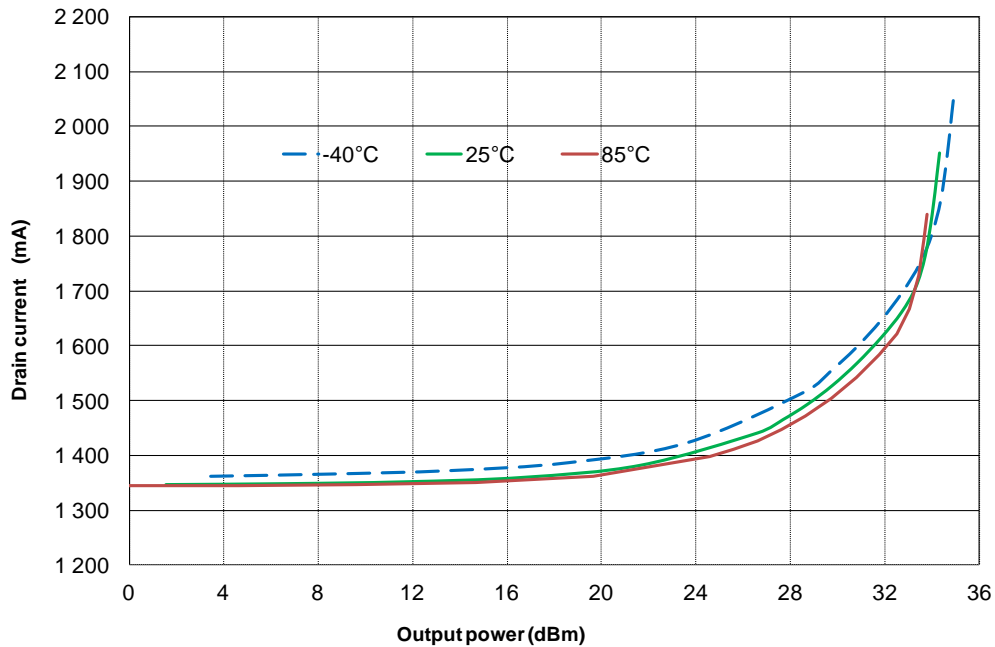
## Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

### Noise figure versus Temperature



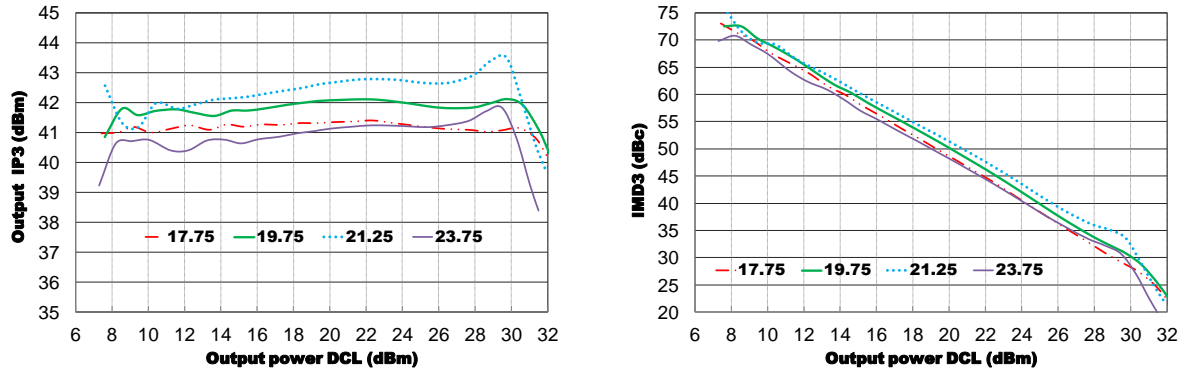
### Drain current versus Output Power



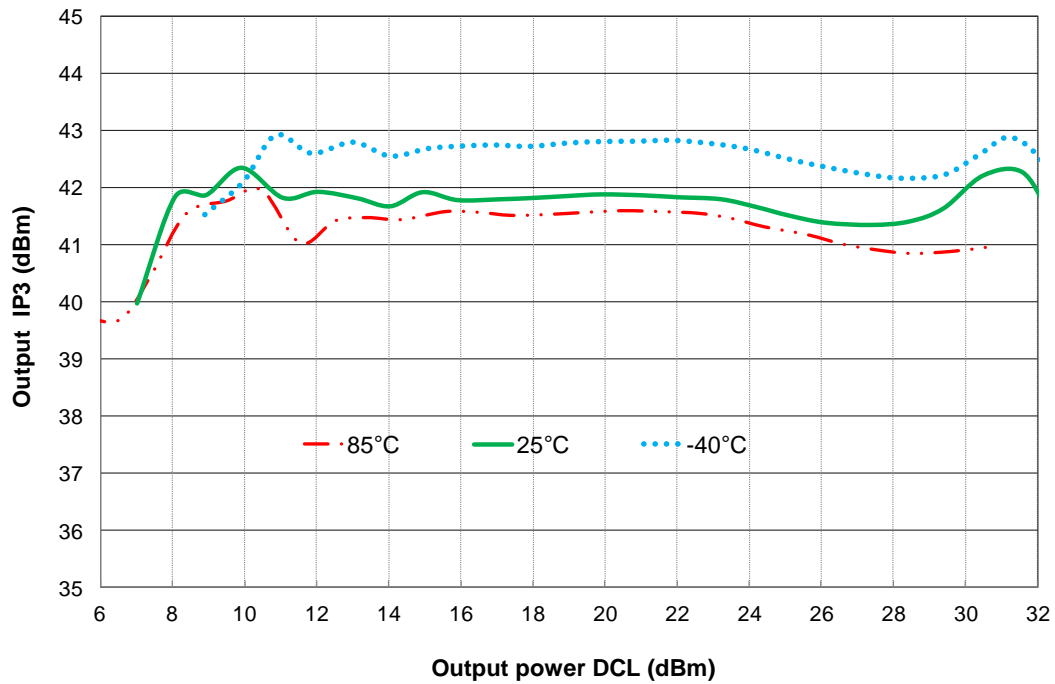
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Output IP3 & IMD3 versus Output Power

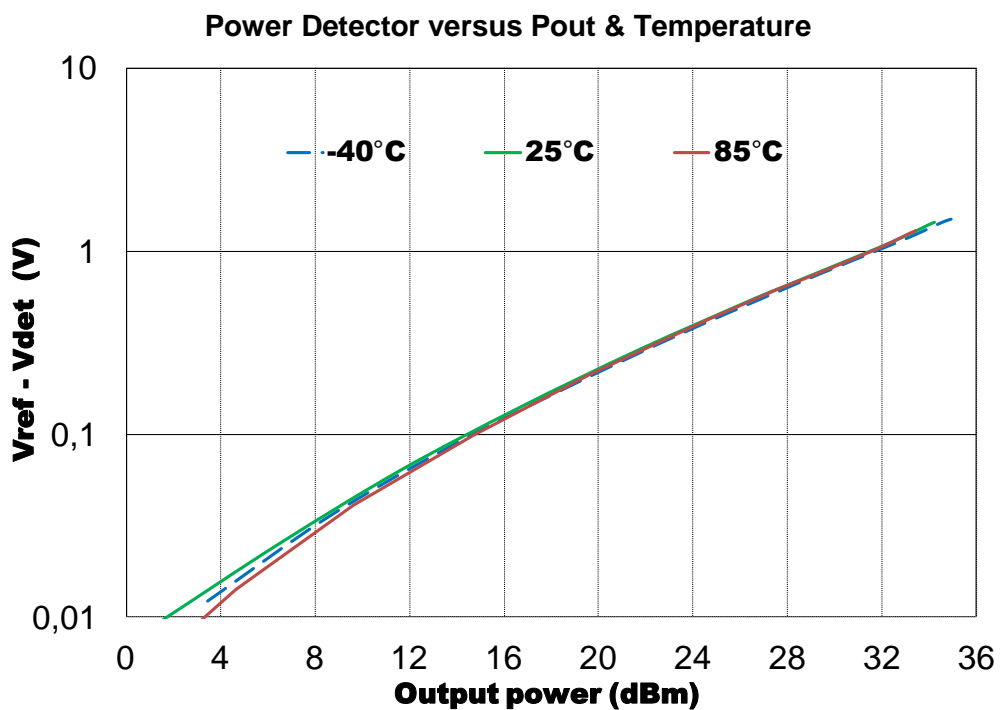
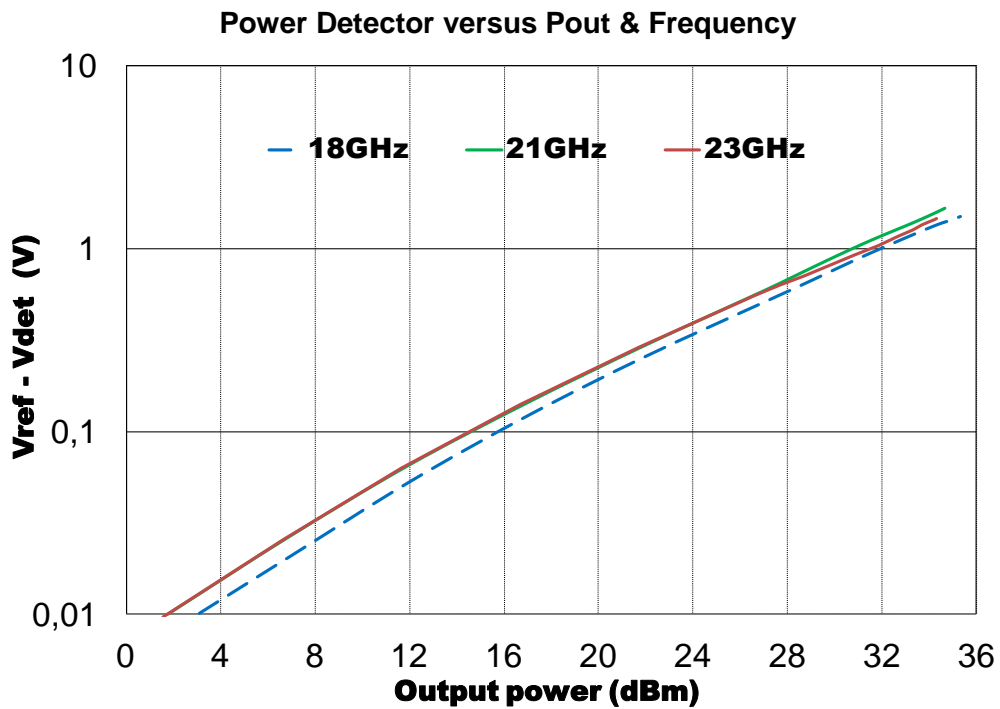


Output IP3 with temperature at 17.75GHz

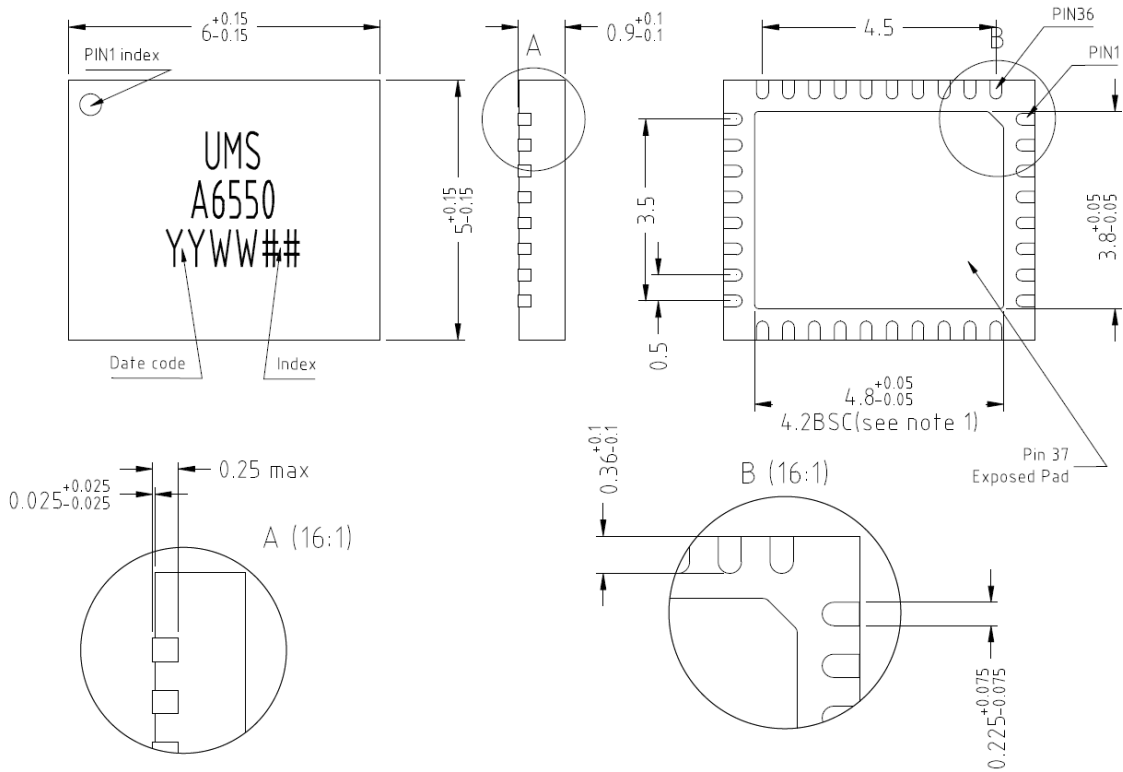


## Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



**Package outline <sup>(1)</sup>**



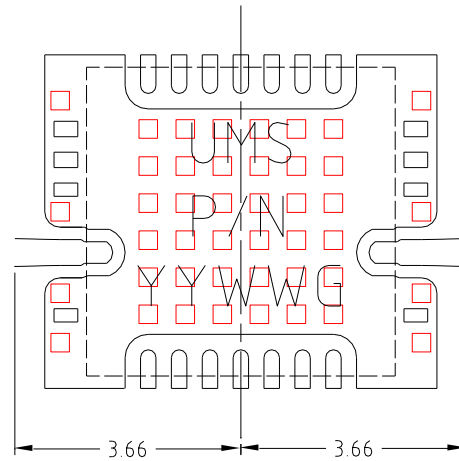
Matte tin, Lead Free (Green)	1- NC	13- RF in	25- NC
Units : mm	2- DET	14- Gnd <sup>(2)</sup>	26- NC
From the standard : JEDEC MO-220 (VGGD)	3- Vd3	15- NC	27- Gnd <sup>(2)</sup>
	4- Vg3	16- NC	28- NC
37- GND	5- Vd2	17- NC	29- Gnd <sup>(2)</sup>
	6- Vg2	18- NC	30- RF out
	7- Vd1	19- Vg1	31- NC
	8- Vg1	20- Vd1	32- NC
	9- NC	21- Vg2	33- NC
	10- NC	22- Vd2	34- NC
	11- NC	23- Vg3	35- REF
	12- NC	24- Vd3	36- NC

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

## Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



## ESD sensitivity

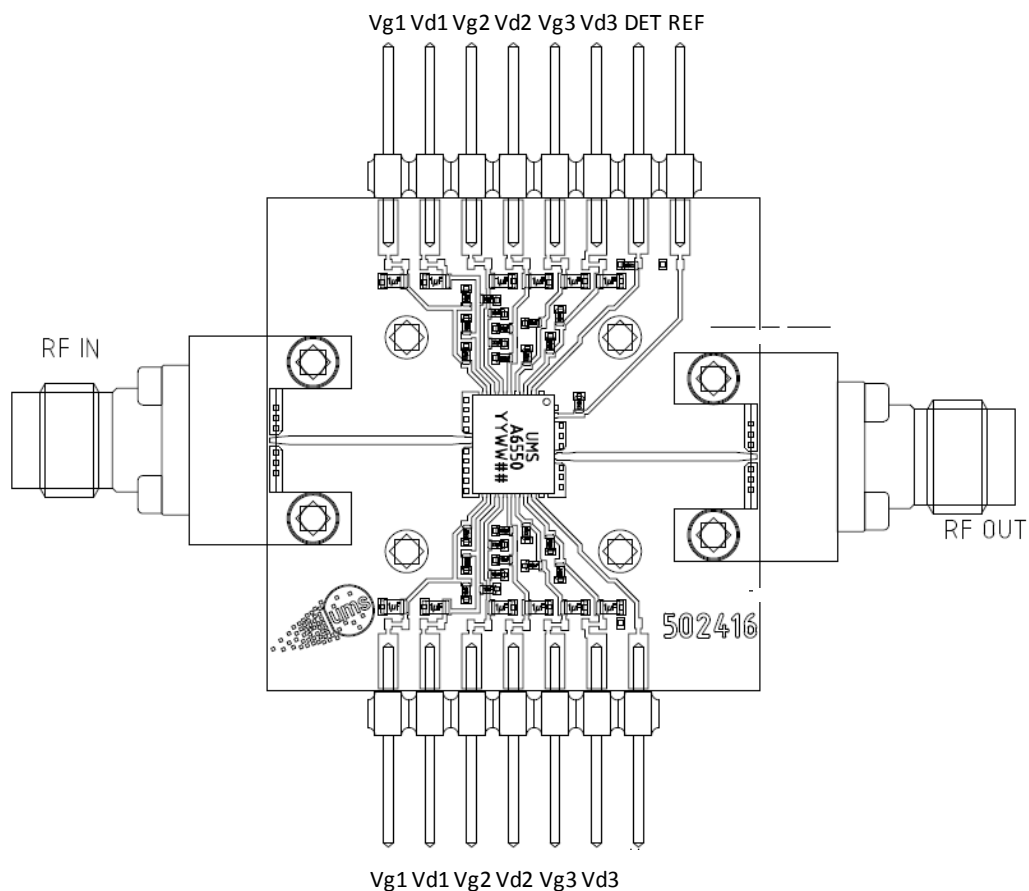
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

## Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

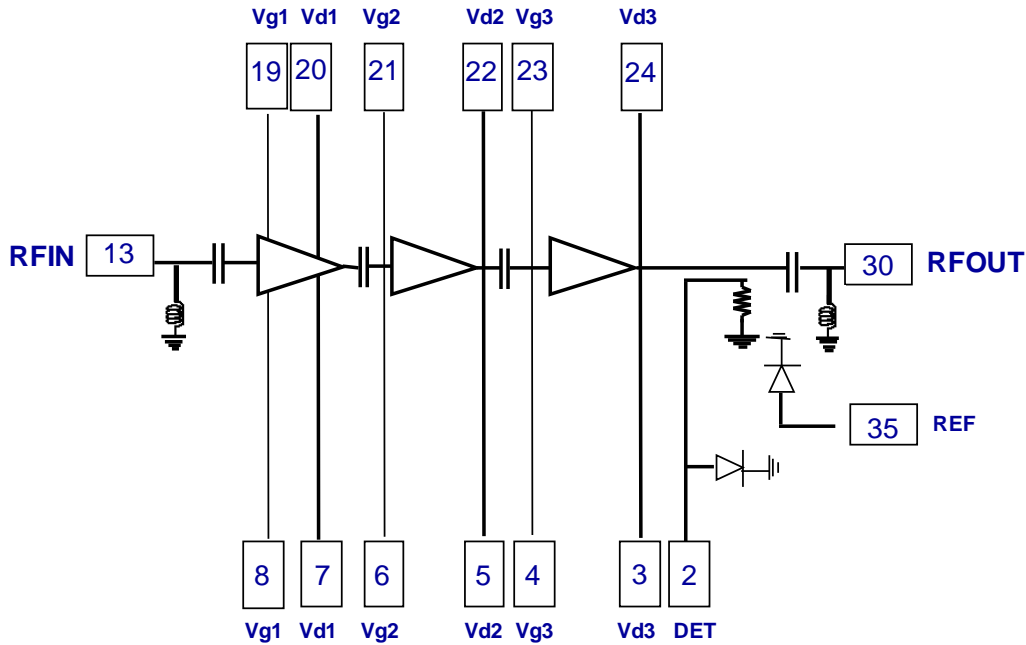
## Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 22pF  $\pm 5\%$ , 10nF  $\pm 10\%$  and 1 $\mu$ F  $\pm 10\%$  are recommended for the gate accesses.
- Decoupling capacitors of 100pF  $\pm 5\%$ , 10nF  $\pm 10\%$  and 1 $\mu$ F  $\pm 10\%$  are recommended for the drain accesses.
- A 10K $\Omega$  resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



### Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



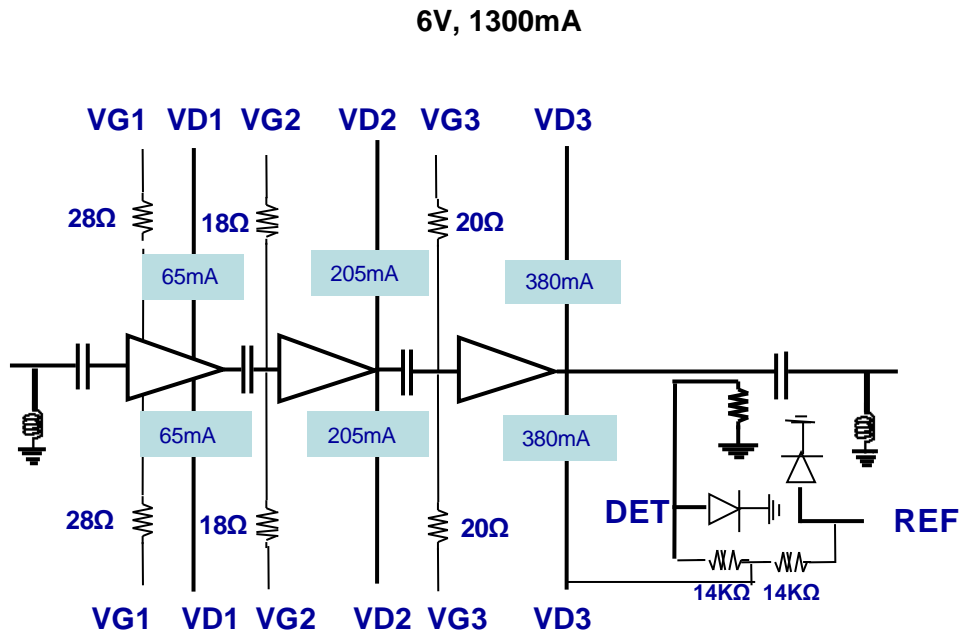
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (See paragraph “Evaluation mother board”) on the PC board, as close as possible to the package.

A 10K $\Omega$  resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads



**DC Schematic**



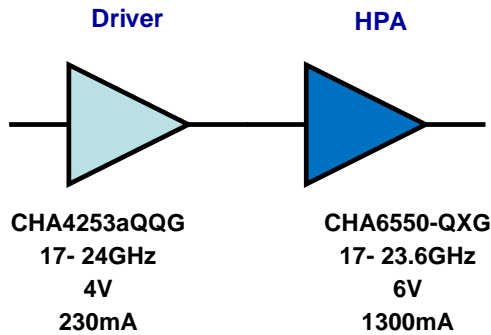
**Recommended UMS Power chain**

The CHA6550-QXG is recommended with the CHA4253aQQG as driver.

Total Gain: 45dB

Gain control: 30dB with the two amplifiers.

For more information about the CHA4253aQQG, see our web site [www.ums-gaas.com](http://www.ums-gaas.com)



## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 6x5 package:

CHA6550-QXG/XY

Stick: XY = 20

Tape & reel: XY = 21

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