

## 5.8-16GHz Low Noise Amplifier

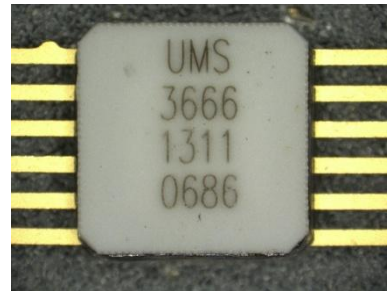
### GaAs Monolithic Microwave IC in SMD package

#### Description

The CHA3666-SNA is a two-stage self biased wide band monolithic low noise amplifier.

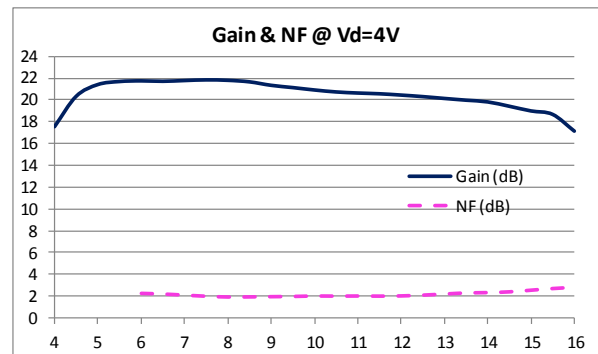
The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in lead-free, hermetic package compatible with space application.



#### Main Features

- Broadband performance 5.8-16GHz
- 2.8dB maximum noise figure
- 24dBm 3<sup>rd</sup> order intercept point
- 16dBm power at 1dB compression
- 20dB gain
- Low DC power consumption
- 12L-Glass/metal hermetic package



#### Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure		2.1	2.8	dB
G	Small signal Gain	16	20		dB
IP3	3rd order intercept point		24		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

## Electrical Characteristics

Tamb.= +25°C, Vd = +4.0V<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5.8		16	GHz
G	Small signal Gain	16	20		dB
ΔG	Gain flatness		±1		dB
NF	Noise figure		2.1	2.8	dB
IS11I	Input return loss		2.3:1	3:1	
IS22I	Output return loss		1.9:1	2.5:1	
IP3	3rd order intercept point		24		dBm
P1dB	Output power at 1dB gain comp	14.5	16		dBm
Vd	Drain bias voltage		4		V
Id	Drain bias current	60	80	100	mA

<sup>(1)</sup> These values are representative of on board measurements as defined on the drawing 96446 (see below).

## Absolute Maximum Ratings <sup>(1)</sup>

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Pin	RF input power	10	dBm
Top	Operating temperature range <sup>(2)</sup>	-40 to +85	°C
Tj	Junction temperature <sup>(3)</sup>	175	°C
Tstg	Storage temperature range	-55 to +125	°C
Tstg	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation on this device above any one of these parameters may cause permanent damage.

<sup>(2)</sup> Top = Package Ground Paddle back side temperature

<sup>(3)</sup> Thermal Resistance channel to ground paddle = 214°C/W for T<sub>ground paddle</sub> = +85°C

**Typical Package Sij parameters**

For low current configuration in 96446 board - in connector plane  
Temp = +25°C, Vd= +4V, typical Id=80mA

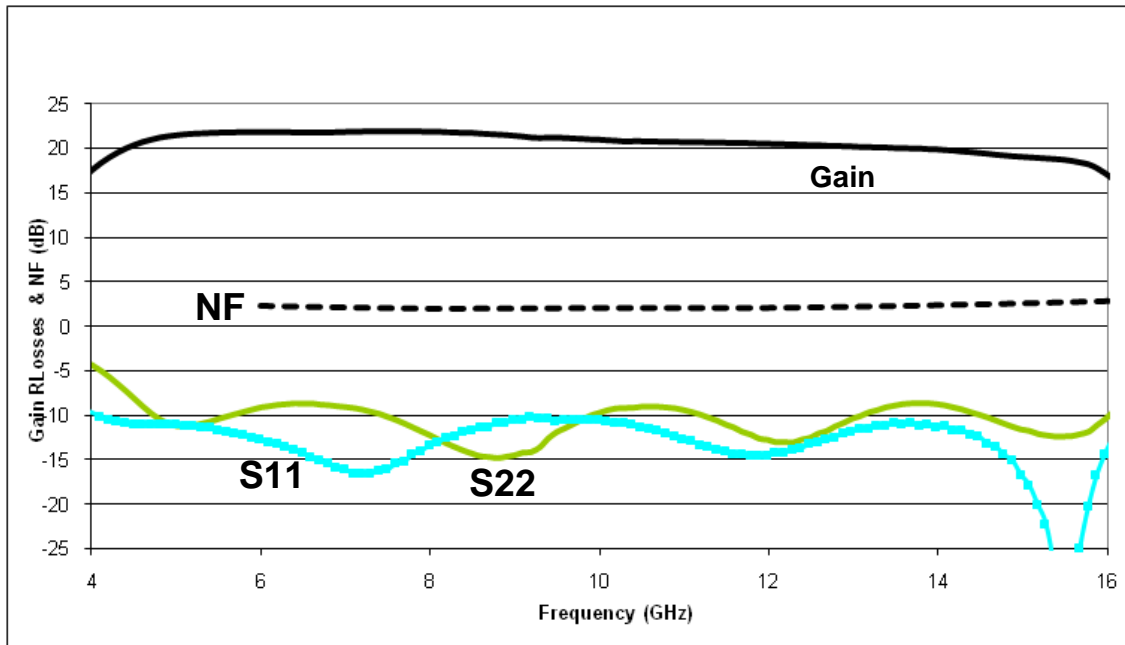
F(GHz)	dBS11	PhS11(°)	dBS21	PhS21(°)	dBS12	PhS12(°)	dBS22	PhS22(°)	NF(dB)
0.1	-0.02	-12.36	-60.38	139.48	-64.76	-124.85	-0.03	-12.38	
1.0	-0.20	-120.14	-51.96	106.43	-66.83	84.74	-0.34	-120.02	
1.5	-0.39	-177.23	-48.22	-127.20	-75.55	124.32	-0.77	-176.02	
2.0	-0.64	123.96	-24.00	167.40	-68.76	-7.25	-1.69	130.69	
2.5	-0.98	57.81	-14.91	110.27	-59.27	-25.95	-1.37	74.27	
3.0	-1.57	-21.16	2.92	44.44	-57.06	-110.13	-2.84	-3.77	
3.5	-2.43	-110.87	12.31	-67.44	-66.93	153.56	-6.78	-71.82	
4.0	-4.34	154.20	17.54	-172.21	-59.56	-102.75	-9.70	-124.50	
4.5	-8.12	54.55	20.34	89.22	-48.72	172.09	-11.01	-165.12	
5.0	-11.16	-52.92	21.42	-1.47	-44.68	96.06	-11.04	153.87	
5.5	-10.35	-138.28	21.70	-83.26	-43.11	23.69	-11.58	110.50	
6.0	-9.06	161.41	21.76	-159.03	-41.87	-42.92	-12.71	65.18	2.263
6.5	-8.66	111.23	21.72	129.68	-41.28	-105.13	-14.26	11.83	
7.0	-9.03	65.00	21.79	61.19	-40.42	-164.80	-16.11	-62.21	
7.5	-10.14	17.00	21.85	-6.81	-39.54	131.57	-16.10	-149.55	
8.0	-12.21	-34.04	21.81	-73.75	-39.48	67.94	-13.34	133.51	1.929
8.5	-14.28	-97.49	21.67	-139.41	-39.49	7.97	-11.71	74.57	
9.0	-14.46	-177.11	21.35	155.94	-39.32	-51.71	-10.50	25.06	
9.5	-11.85	115.71	21.14	93.78	-38.14	-111.12	-10.61	-21.62	
10.0	-9.69	55.02	20.92	31.53	-38.25	-168.04	-10.53	-64.86	2.016
10.5	-9.00	2.05	20.74	-29.49	-37.65	133.49	-11.26	-109.97	
11.0	-9.36	-50.93	20.64	-90.59	-37.24	78.04	-12.62	-160.01	
11.5	-10.99	-107.09	20.57	-151.94	-36.71	19.74	-14.09	145.24	
12.0	-12.72	-174.74	20.45	146.68	-36.63	-39.71	-14.50	86.87	2.026
12.5	-12.50	110.72	20.31	85.40	-36.74	-98.01	-13.20	31.84	
13.0	-10.35	48.31	20.14	24.29	-36.68	-153.72	-11.87	-17.92	
13.5	-8.87	-4.04	19.98	-36.89	-36.98	149.45	-10.88	-63.55	
14.0	-8.70	-47.93	19.82	-98.74	-36.97	93.10	-11.28	-108.47	2.33
14.5	-9.89	-87.63	19.42	-160.87	-36.83	36.08	-12.37	-154.57	
15.0	-11.55	-117.88	18.99	138.15	-36.64	-19.54	-16.65	149.97	
15.5	-12.35	-149.85	18.67	75.82	-35.86	-77.12	-35.87	84.18	
16.0	-10.37	165.68	17.13	10.79	-34.33	-150.29	-14.27	-163.03	2.809
16.5	-7.75	69.16	16.68	-24.68	-43.15	114.42	-10.90	82.97	
17.0	-9.93	3.68	18.88	-98.63	-43.49	134.87	-15.99	65.62	
17.5	-9.39	-43.54	17.96	-166.15	-38.62	98.95	-11.57	36.49	
18.0	-8.11	-93.30	17.52	132.71	-34.16	37.05	-8.63	-13.07	3.607
18.5	-9.91	-155.23	17.16	68.45	-31.76	-32.73	-8.10	-70.38	
19.0	-12.43	127.43	16.80	3.23	-31.36	-105.37	-11.09	-126.69	
19.5	-11.75	15.00	15.77	-67.74	-32.93	-168.03	-15.17	-179.57	
20.0	-9.90	-67.91	13.59	-133.13	-31.81	140.77	-15.84	102.41	

## Typical on wafer Measurements

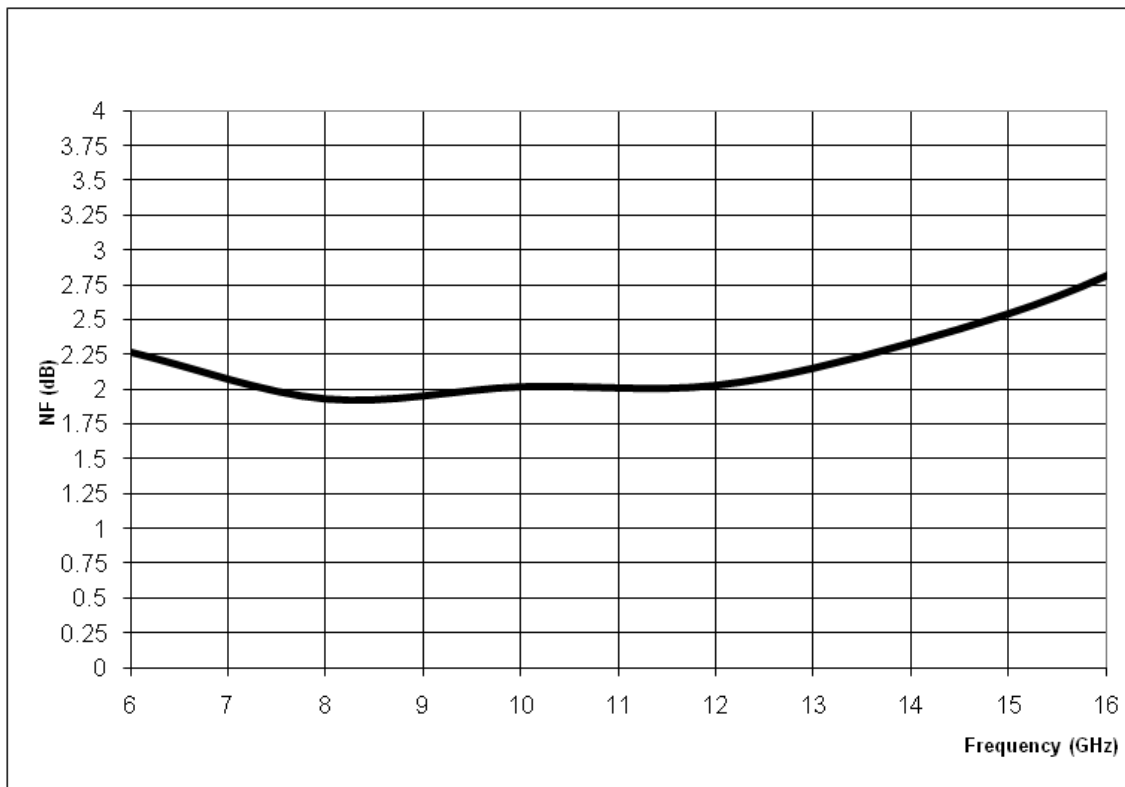
Temp = +25°C, Vd=4V (Id=80mA)

Measurements in the connector planes, using the proposed land pattern & board 96446.

**Gain Losses & NF @Vd=4V**



**NF@Vd=4V (Test board losses included)**

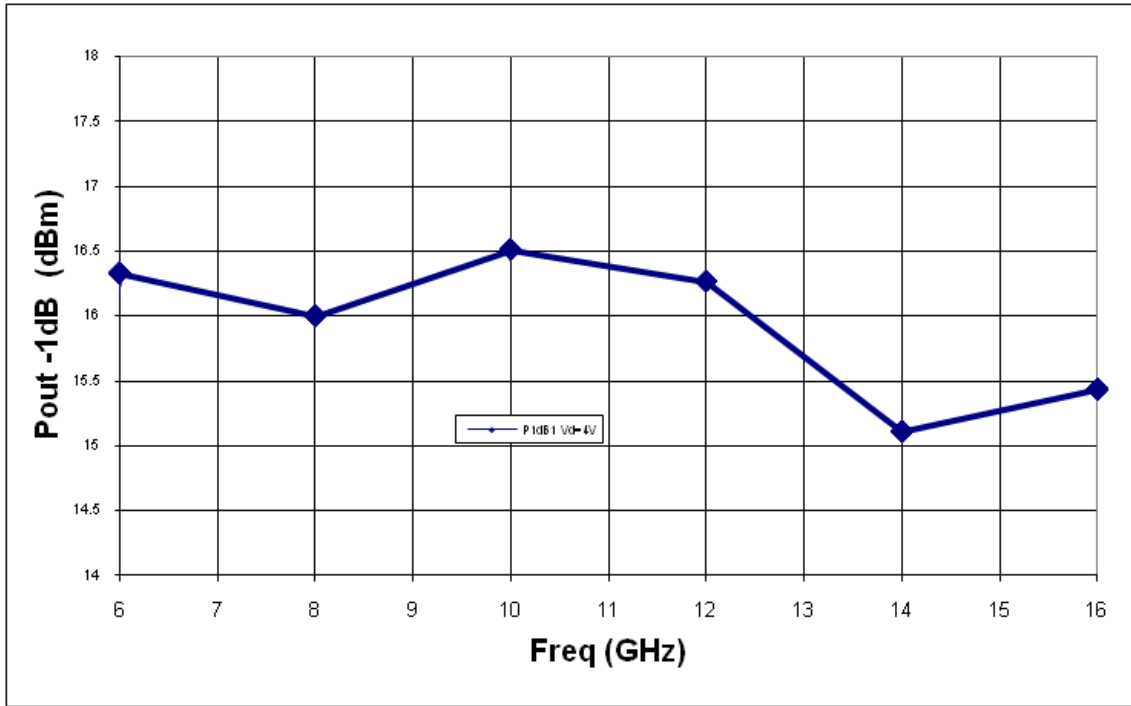


**Typical on wafer Measurements**

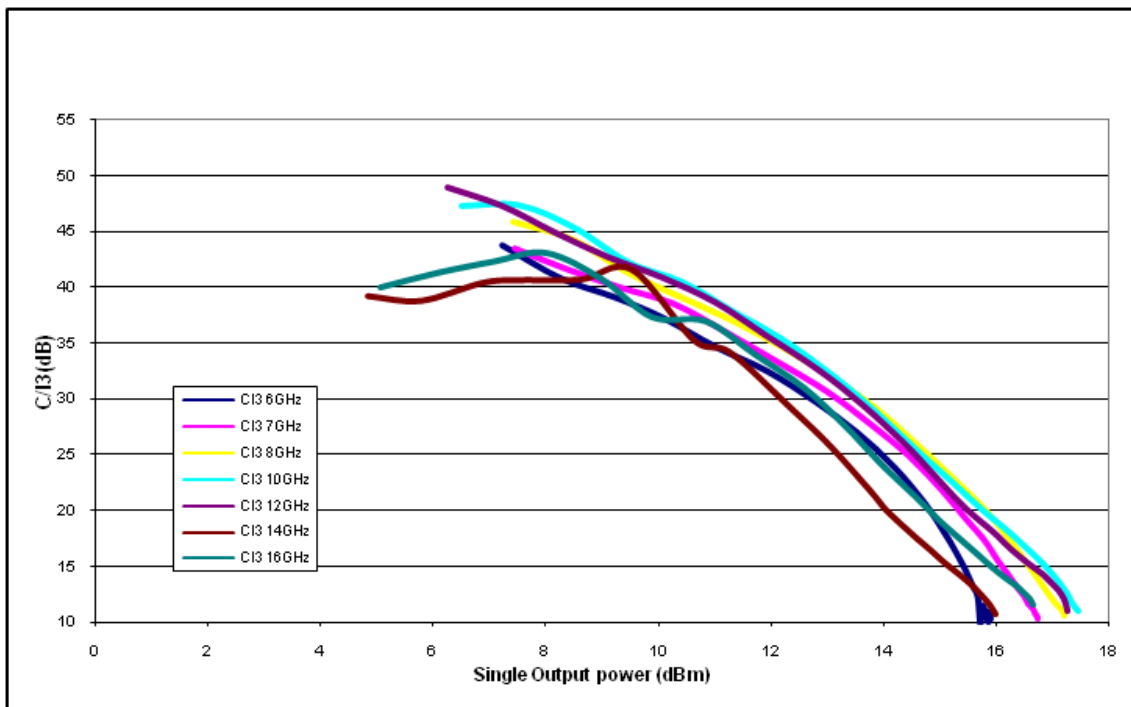
Temp = +25°C, Vd=4V (Id=80mA)

Measurements in the connector planes, using the proposed land pattern & board 96446.

**Output power at 1dB compression versus frequency**



**C/I3 versus output power**

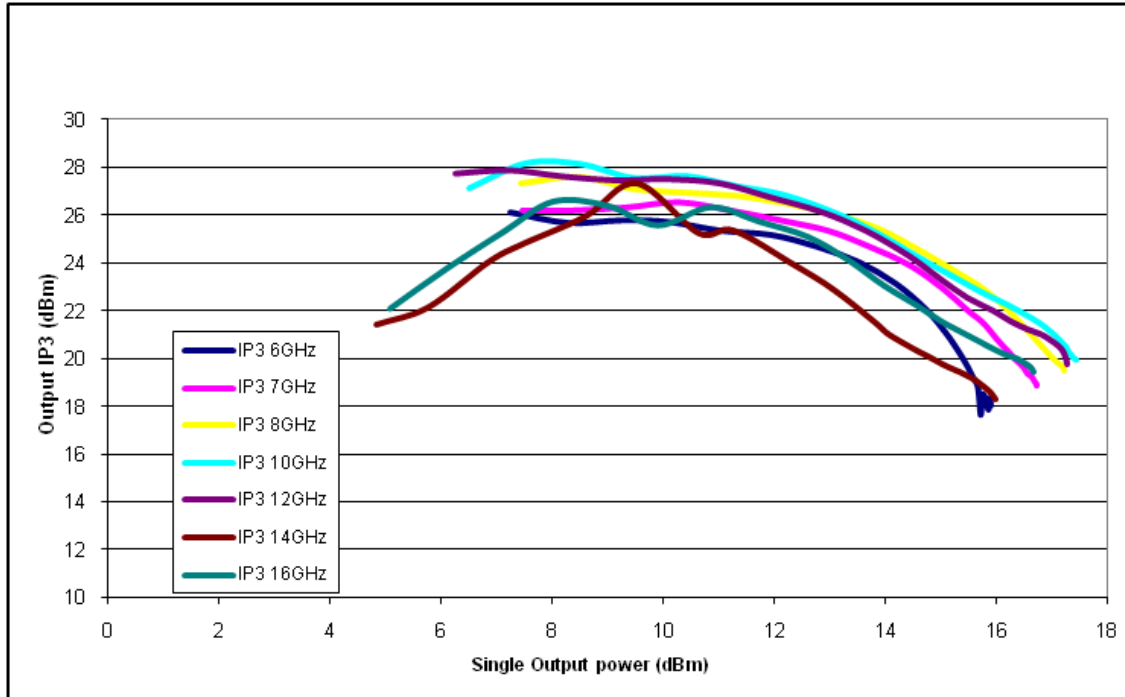


### Typical on wafer Measurements

Temp = +25°C, Vd=4V (Id=80mA)

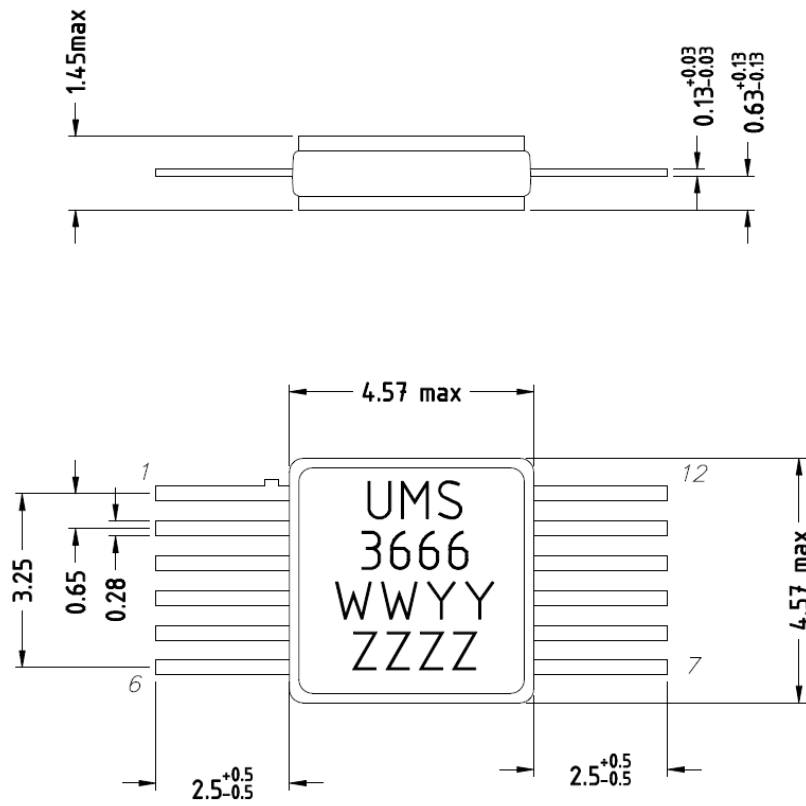
Measurements in the connector planes, using the proposed land pattern & board 96446.

Output IP3 versus output power



Package outline <sup>(1)</sup>

Units : mm

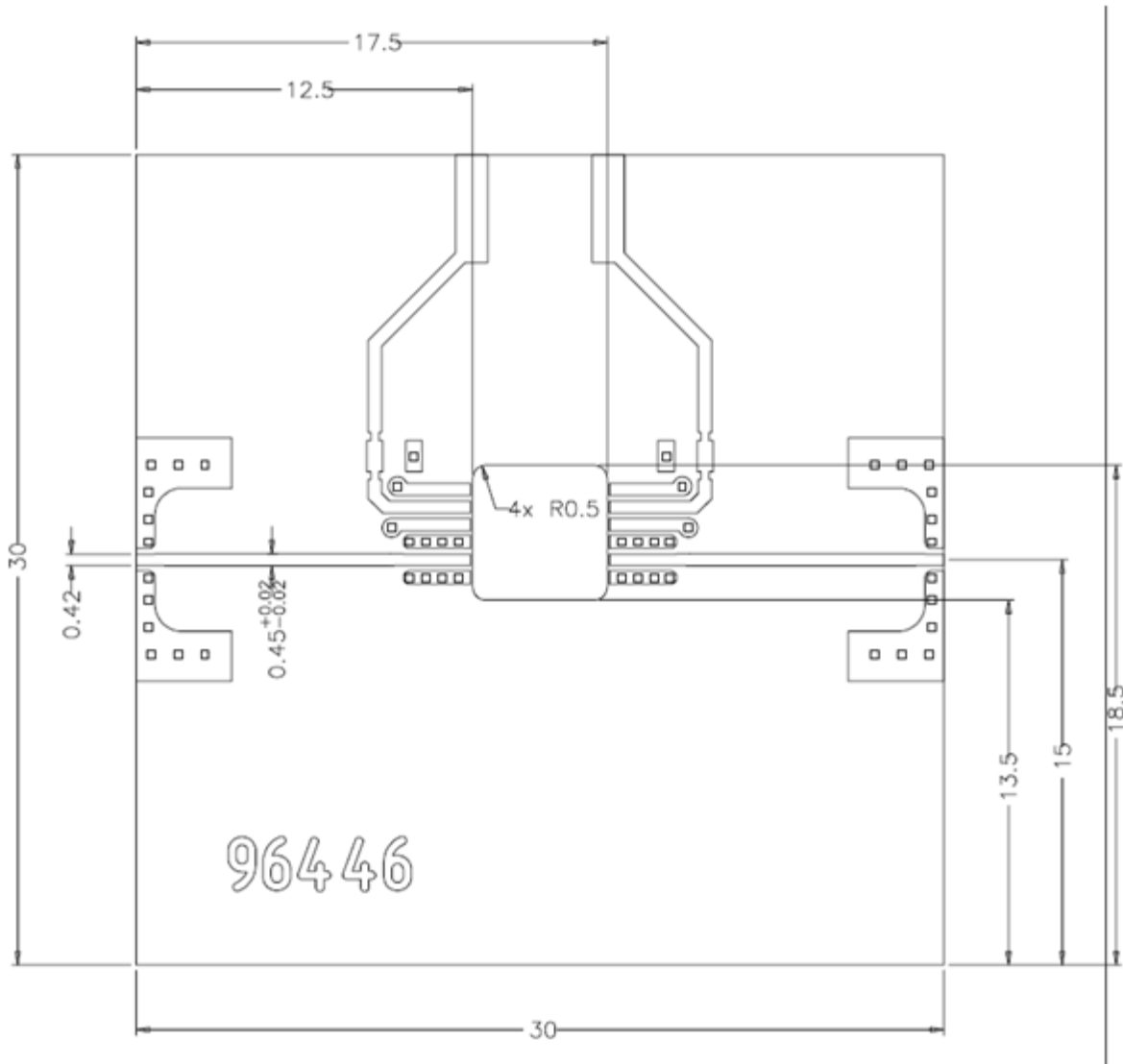


1-	Gnd	5-	RFin	9-	Gnd
2-	VD1-VD2	6-	Gnd	10-	Gnd
3-	Gnd	7-	Gnd	11-	VD1-VD2
4-	Gnd	8-	RFout	12-	Gnd

<sup>(1)</sup> Pin 2 and 11 are equivalent.

### Proposed Evaluation board "96446".

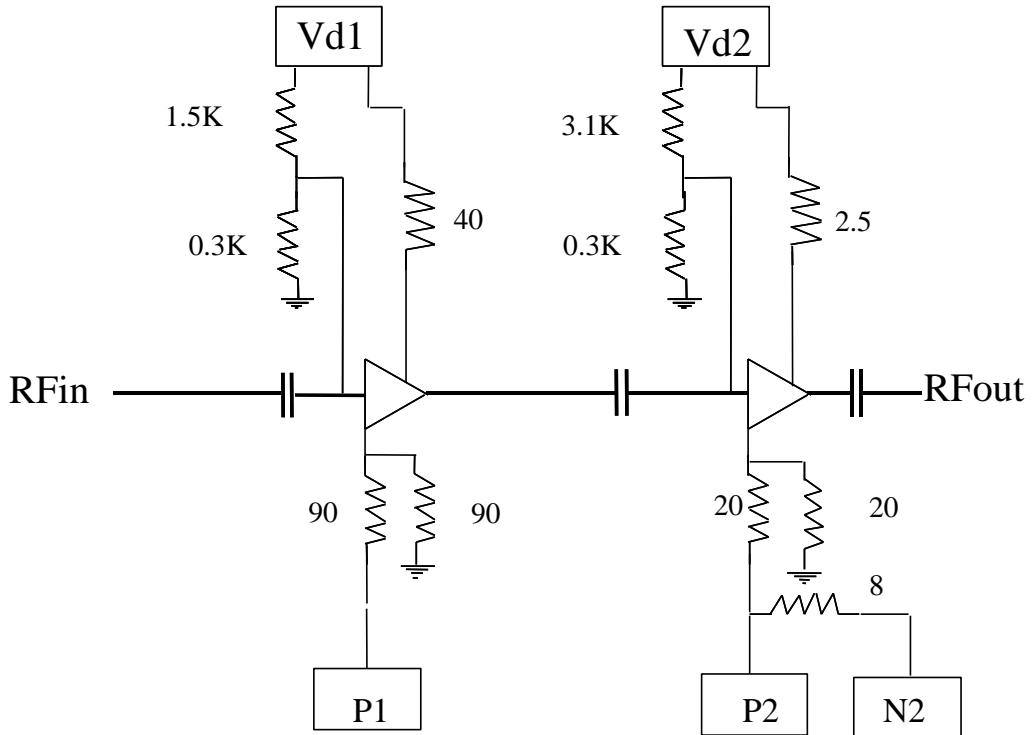
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Two biasing side options (pin 2 and 11)
- Decoupling capacitors of 10nF  $\pm 10\%$  are recommended for DC accesses.
- Recommended for the implementation of this product on a module board.





**DC Schematic**

This chip is self-biased, and flexibility is provided by the access to number of leads. The internal DC electrical schematic is given in order to use these leads in a safe way.



Standard biasing:

Low Noise and low consumption:

Vd = 4V  
Idd = 80mA & Pout-1dB = 16dBm Typical.

### Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

### Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

Glass/Metal 12L hermetic package:                      CHA3666-SNA/XY  
Tray: XY = 23

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