17-24GHz Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

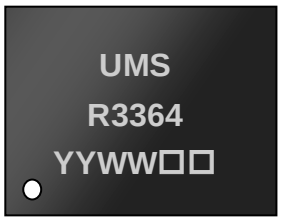
Description

The CHR3364-QEG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO chain with buffers associated to a time two multiplier, and a RF low noise amplifier including gain control.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

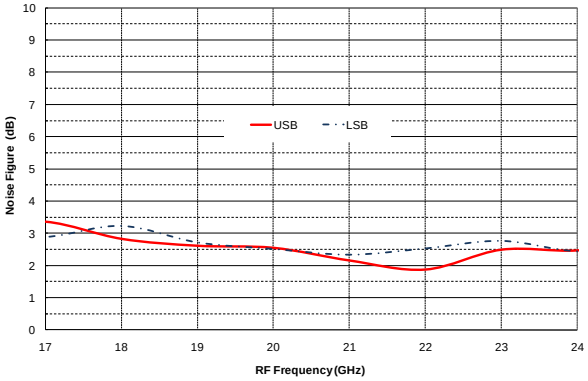
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 17-24GHz
- 11dB Conversion gain
- 17dBc Image Rejection
- 1dBm Input IP3
- 2.7dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=320mA
- 24L-QFN4x5
- MSL1

Noise figure



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17.0		24.0	GHz
F_{LO}	LO frequency range	6.5		14.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
C_G	Conversion gain		11.0		dB

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Electrical Characteristics

Tamb.= +25°C, VD = VDL = 4.0V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17		24	GHz
F_{LO}	LO frequency range	6.5		14	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
C_G	Conversion Gain		11		dB
NF	Noise Figure for IF>0.1GHz		2.7		dB
Im_rej	Image rejection (1)		17		dBc
P_{LO}	LO Input power		0		dBm
IIP3	Input IP3		1		dBm
2LO/RF	2LO leakage at RF port		-40		dBc
VD, VDL	DC drain voltage		4.0		V
ID	Drain current on VD pin for LO buffer		245		mA
IDL	Drain current on VDL pin for LNA		75		mA
VGL	LNA DC gate voltage (2)		-0.5		V
VGM	Mixer DC gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

(1) An external combiner 90° is required on I / Q.
(2) Typical VGL value for IDL = 75mA
See in paragraph " biasing option" other possibility to optimise differently the performances

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD, VDL	Drain bias voltage	5	V
ID+IDL	Drain bias current	430	mA
VGL	LNA Gate bias voltage	-2 to +0.4	V
VGM	Mixer Gate bias voltage	-2 to +0.4	V
P_{RF}	Maximum peak RF input power overdrive (2)	+10	dBm
P_{LO}	Maximum peak LO input power overdrive (2)	+10	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

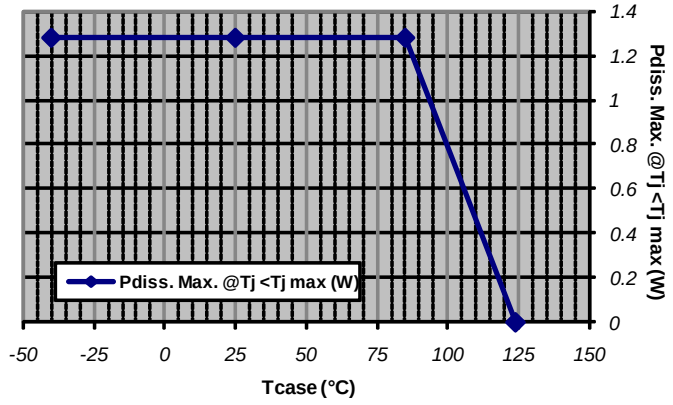
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

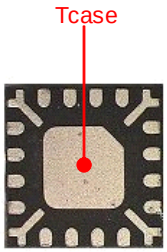
DEVICE THERMAL SPECIFICATION : CHR3364-QEG			
Recommended max. junction temperature (Tj max)		:	124 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power (Pdiss. Max.)		:	1.3 W
=> Pdiss. Max. derating above Tcase(1)=	85 °C	:	33 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<30 °C/W
Minimum Tcase operating temperature(3)		:	-40 °C
Maximum Tcase operating temperature(3)		:	85 °C
Minimum storage temperature		:	-55 °C
Maximum storage temperature		:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.0

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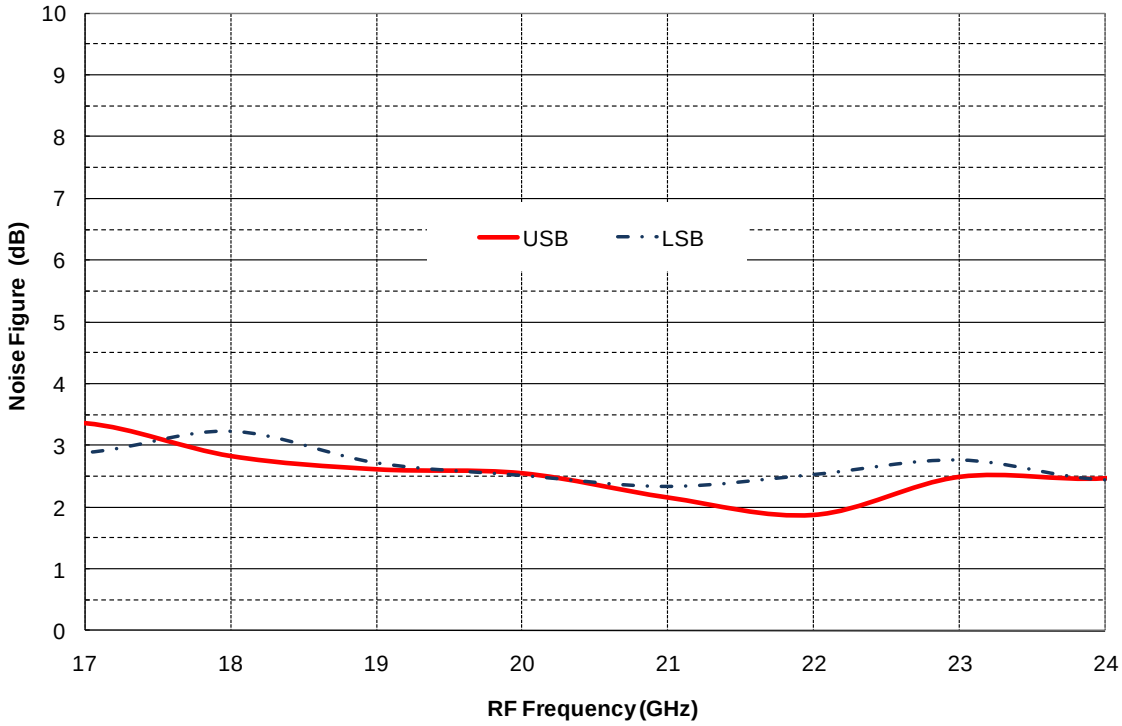
Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

The values shown on the following pages are representative of on-board measurements where results are given on package access planes.

Noise Figure in Supradyne and Infradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO} \pm F_{IF}$, F_{IF} = 2.0GHz



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Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

Conversion Gain in Supradyne and Infradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO} \pm F_{IF}$, F_{IF} = 3.5GHz

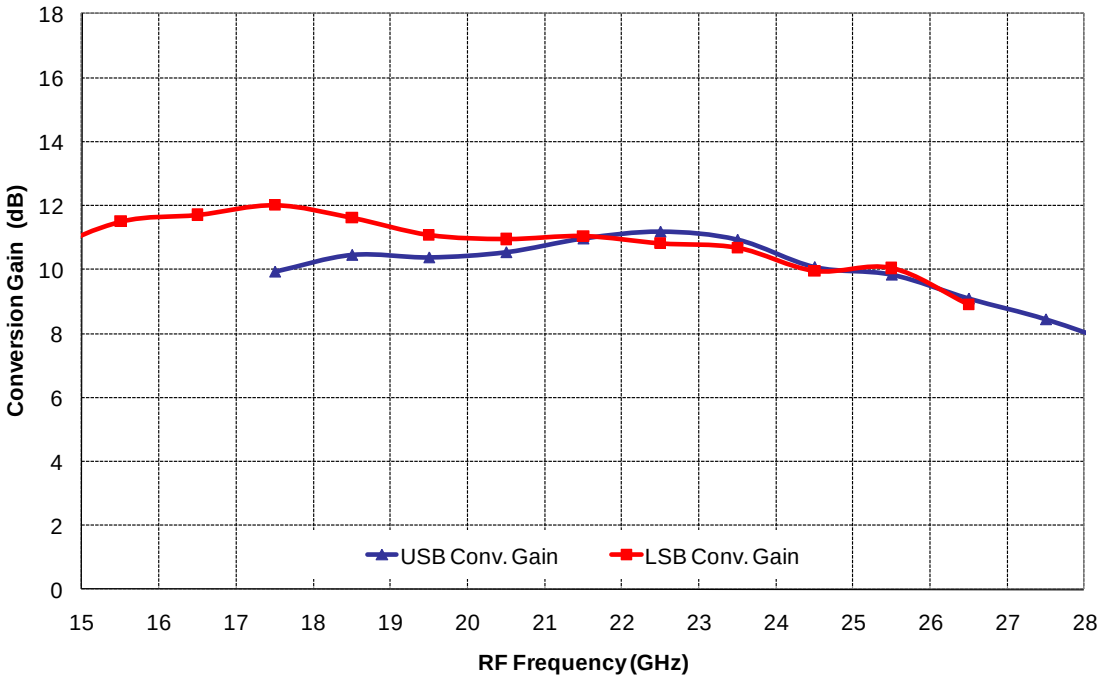
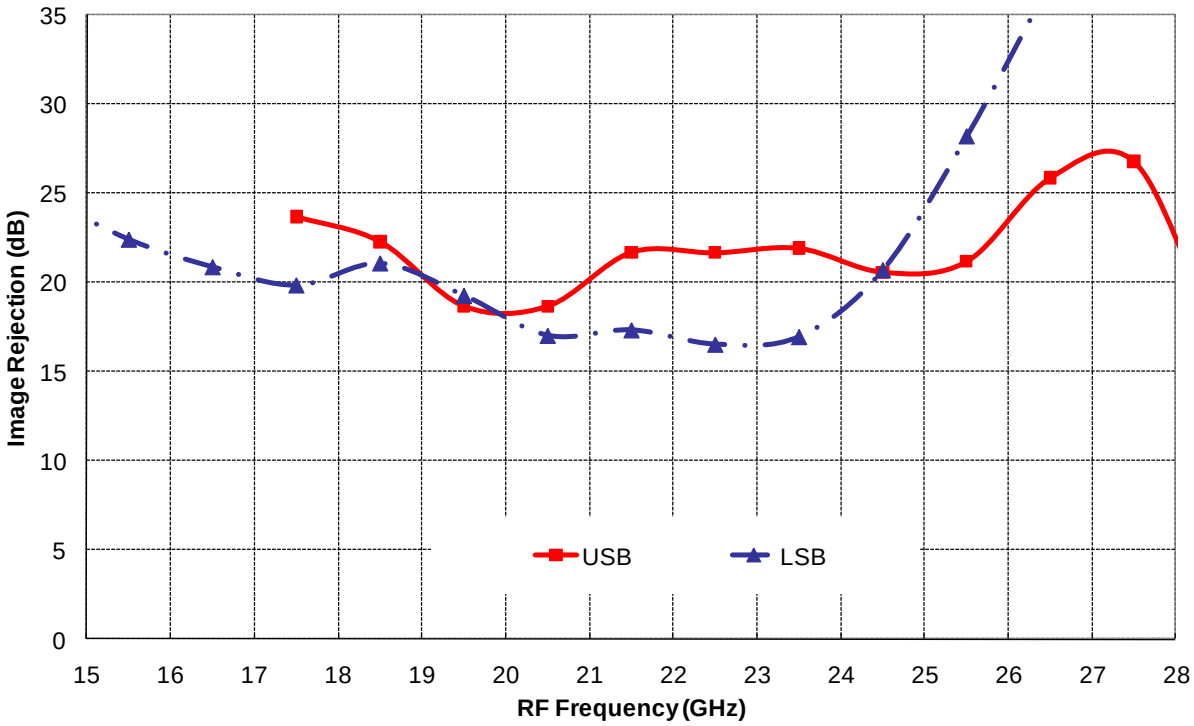


Image Rejection versus RF Frequency

$F_{RF} = 2xF_{LO} \pm F_{IF}$, F_{IF} = 3.5GHz



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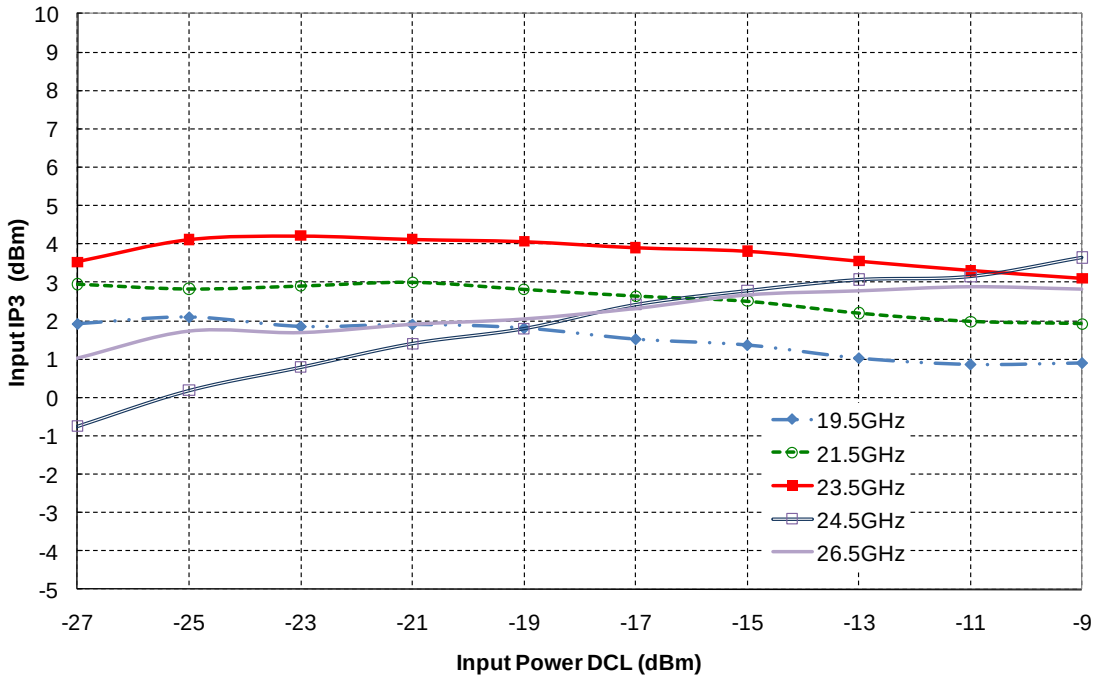
Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

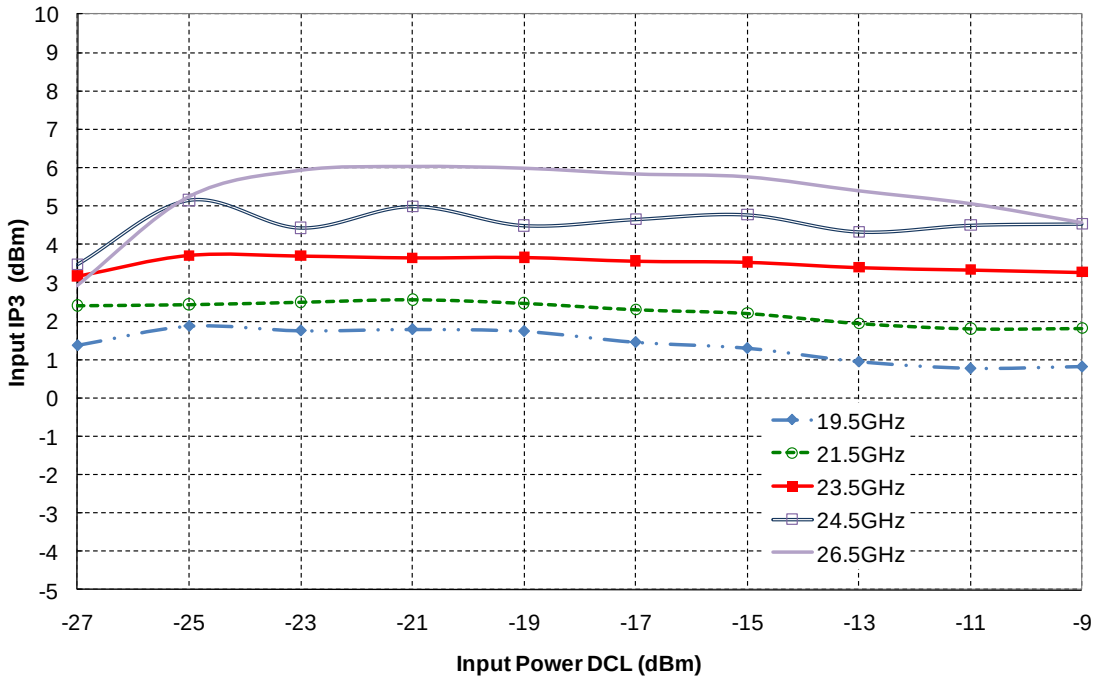
Input IP3 in Supradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}+F_{IF}$, F_{IF} = 3.5GHz



Input IP3 in Infradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}-F_{IF}$, F_{IF} = 3.5GHz



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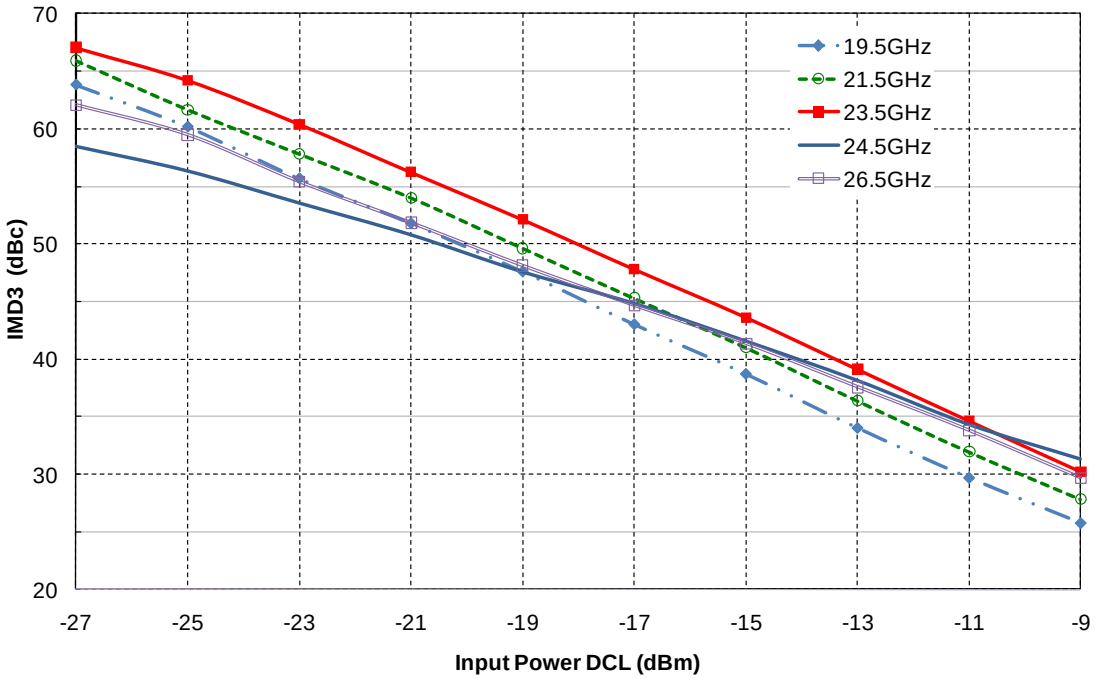
Typical Board Measurements

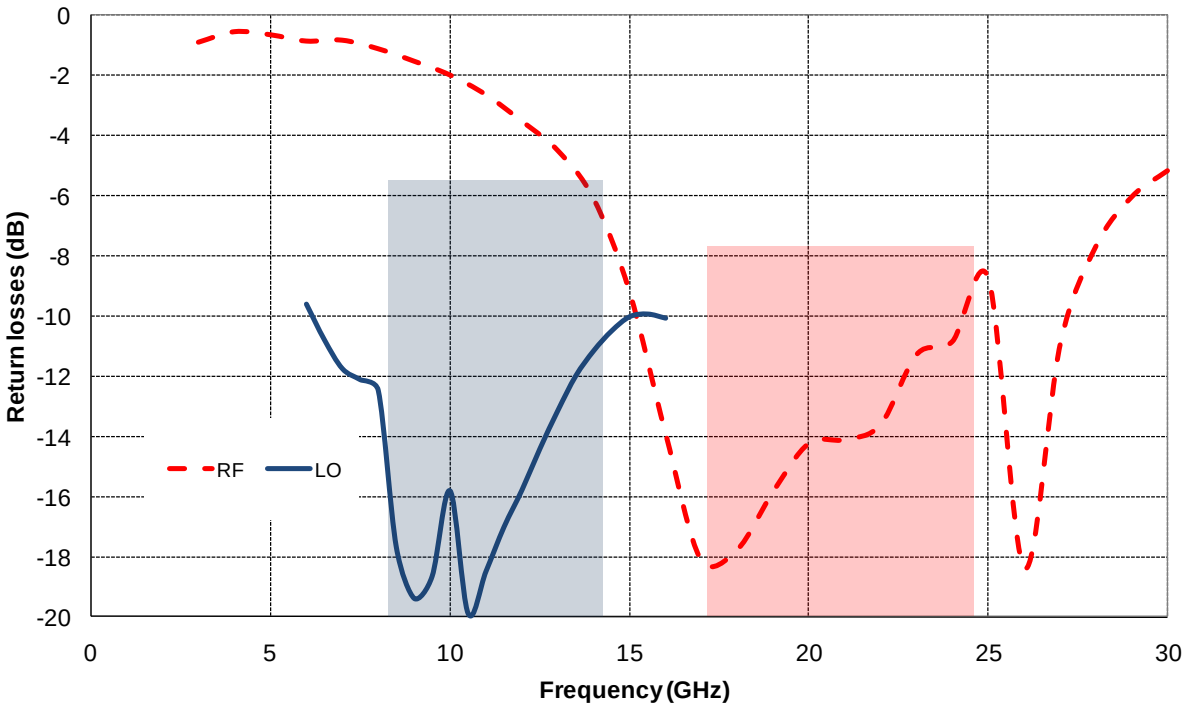
Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

IMD3 in Supradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}+F_{IF}$, F_{IF} = 3.5GHz



LO & RF return loss versus frequency



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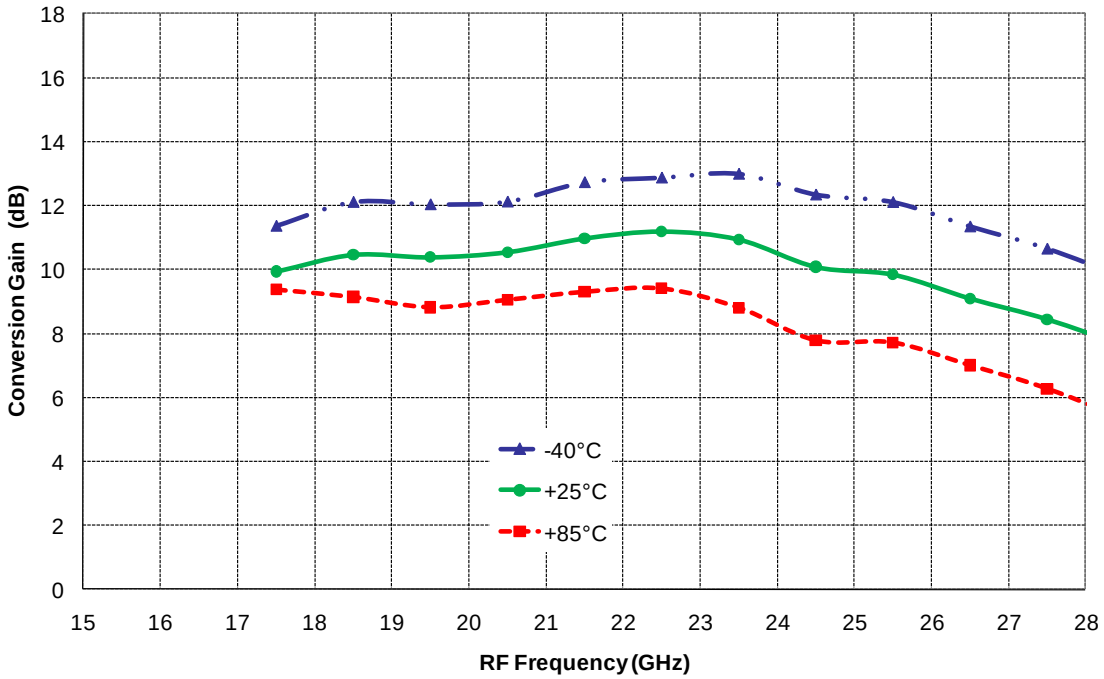
Temperature Board Measurements

T = [-40, +25, +85] °C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

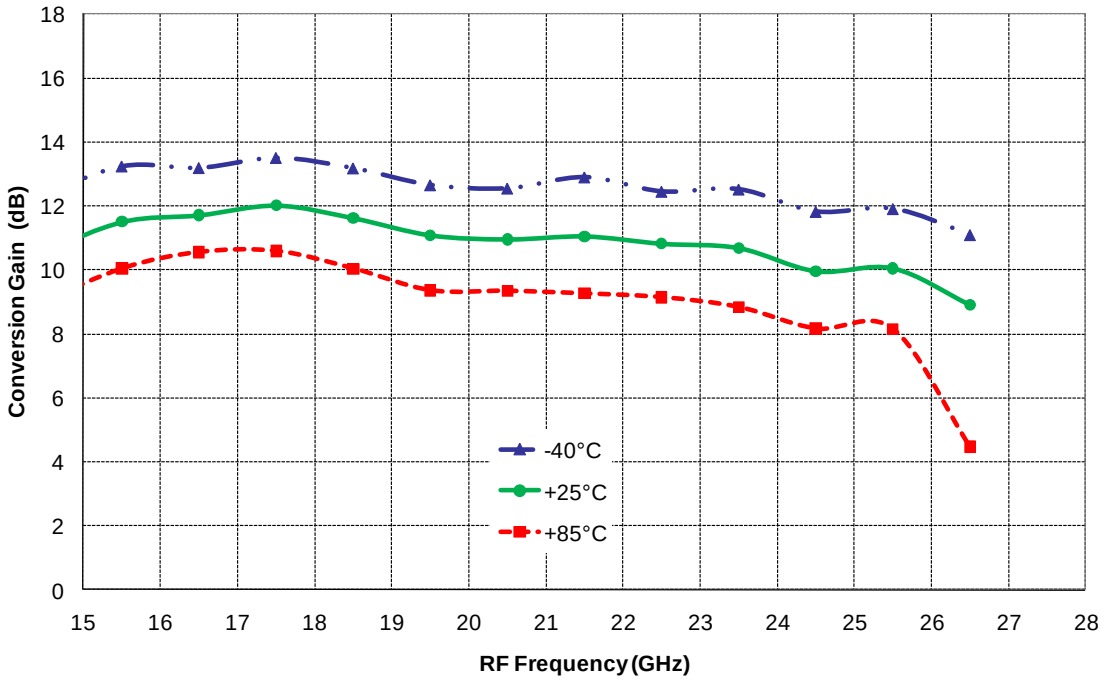
Conversion Gain in Supradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}+F_{IF}$, F_{IF} = 3.5GHz



Conversion Gain in Infradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}-F_{IF}$, F_{IF} = 3.5GHz



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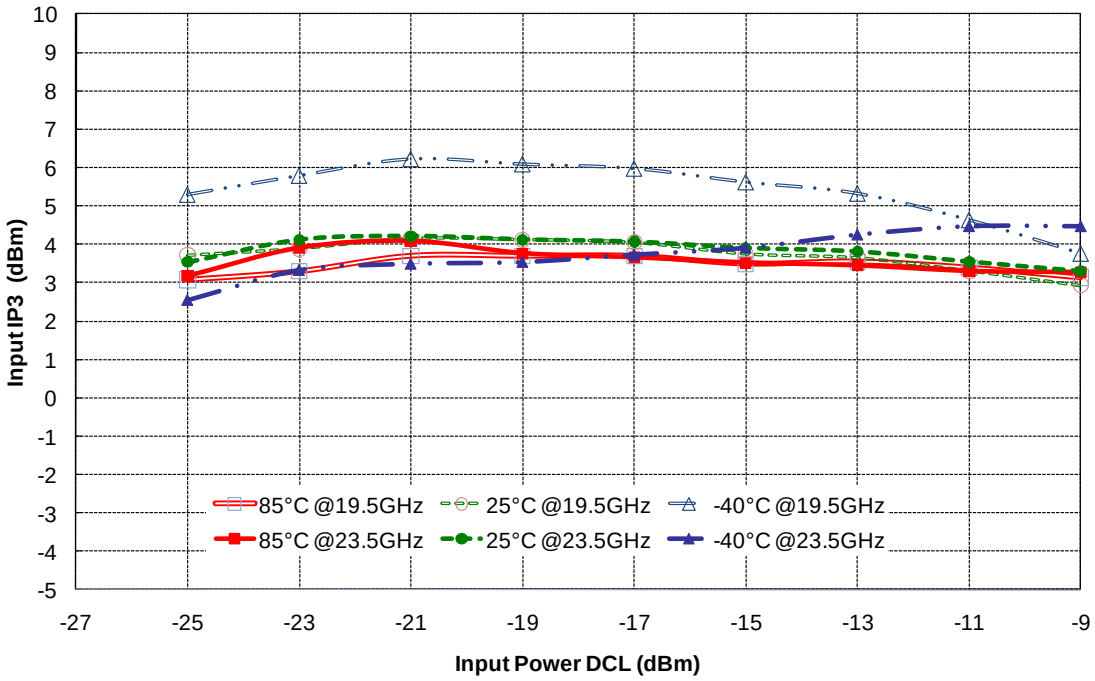
Temperature Board Measurements

T = [-40, +25, +85] °C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P_{LO} = 0dBm

Input IP3 in Supradyne Mode versus RF Frequency

$F_{RF} = 2xF_{LO}+F_{IF}$, F_{IF} = 3.5GHz



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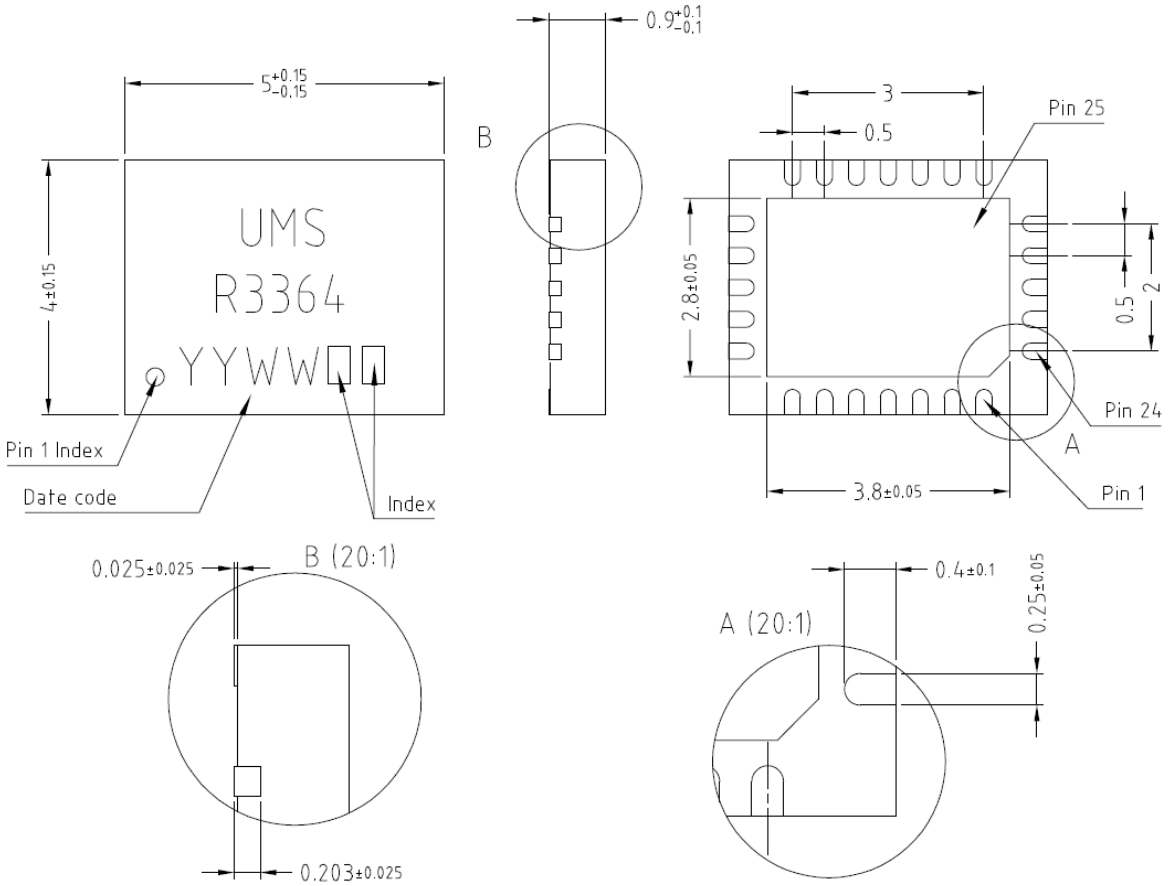
Package outline (1)



Matt tin, Lead Free	(Green)	1-	Nc	9-	VGL	17-	Nc
Units :	mm	2-	Nc	10-	VDL	18-	Nc
From the standard :	JEDEC MO-220	3-	Nc	11-	VGM	19-	Nc
	(VGGD)	4-	Gnd(2)	12-	VD	20-	IF_I out
25-	GND	5-	RF in	13-	Nc	21-	Gnd(2)
		6-	Gnd(2)	14-	Gnd(2)	22-	IF_Q out
		7-	Nc	15-	LO in	23-	Nc
		8-	Nc	16-	Gnd(2)	24-	Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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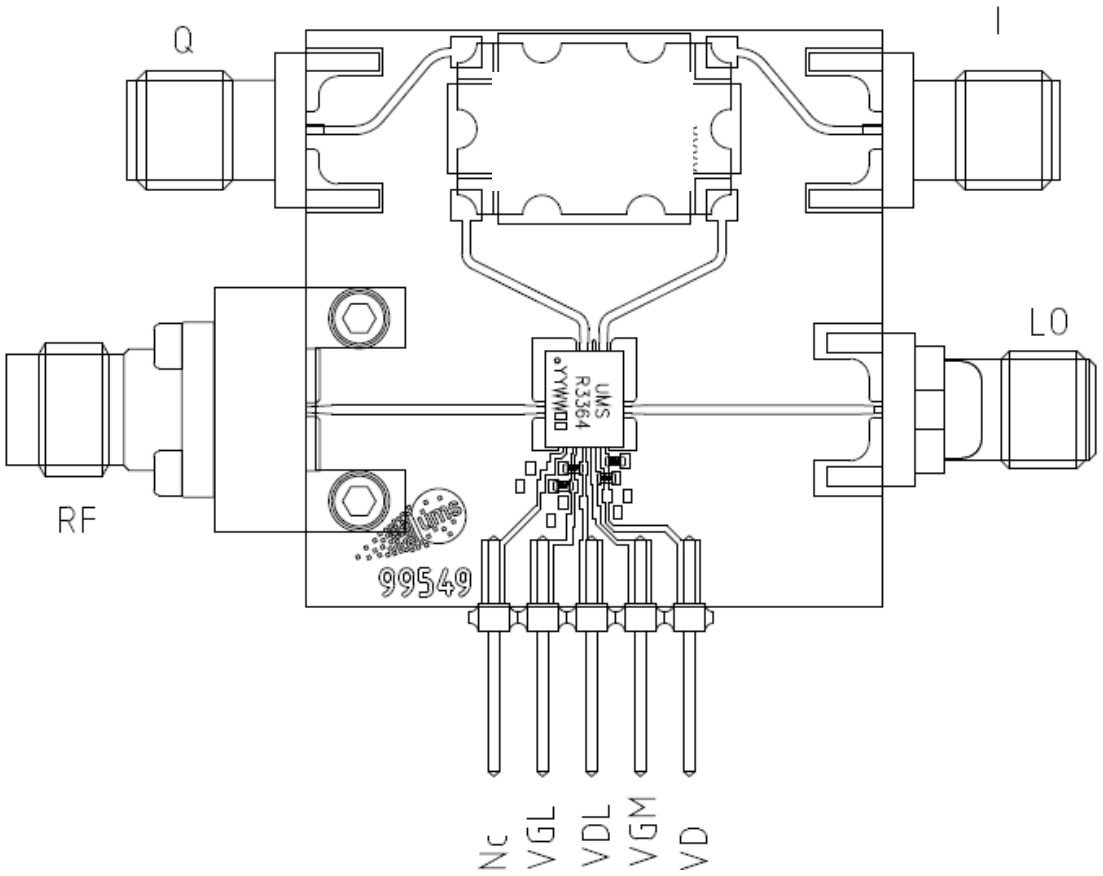
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Hybrid coupler 90° 2-4GHz

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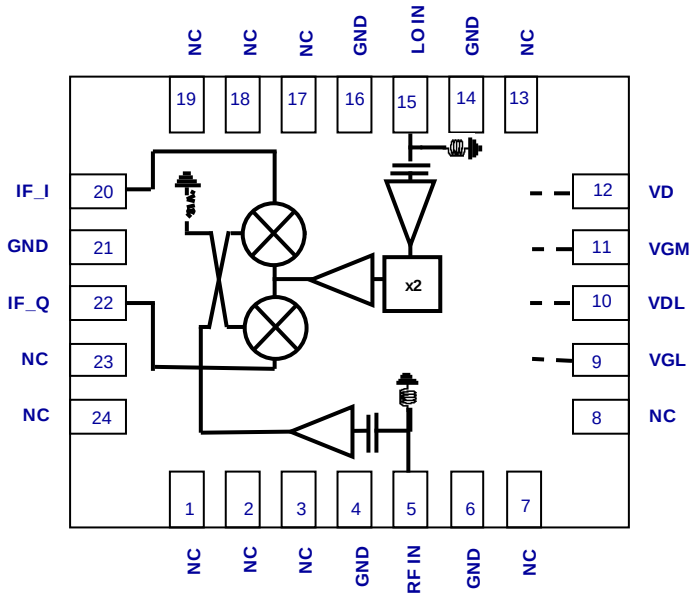
Notes

Due to ESD protection circuits on RF and LO input, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses.



ESD protections are also implemented on gate accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

Biasing Options

In order to improve the conversion gain or the input IP3, the biasing could be tuned.
VGL voltage allows controlling IDL current.
Table below gives the typical value for main characteristics

	VD=VDL= 4.0V IDL= 75mA	**VD=VDL= 4.5V IDL= 110mA**
Conversion Gain (dB)	11	12.5
Noise Figure (dB)	2.7	2.6
Input IP3 (dBm)	+1	+3
VGL (V)	-0.5	-0.4
ID (mA)	245	250
ID +IDL (mA)	320	360
Total DC power consumption (mW)	1280	1620

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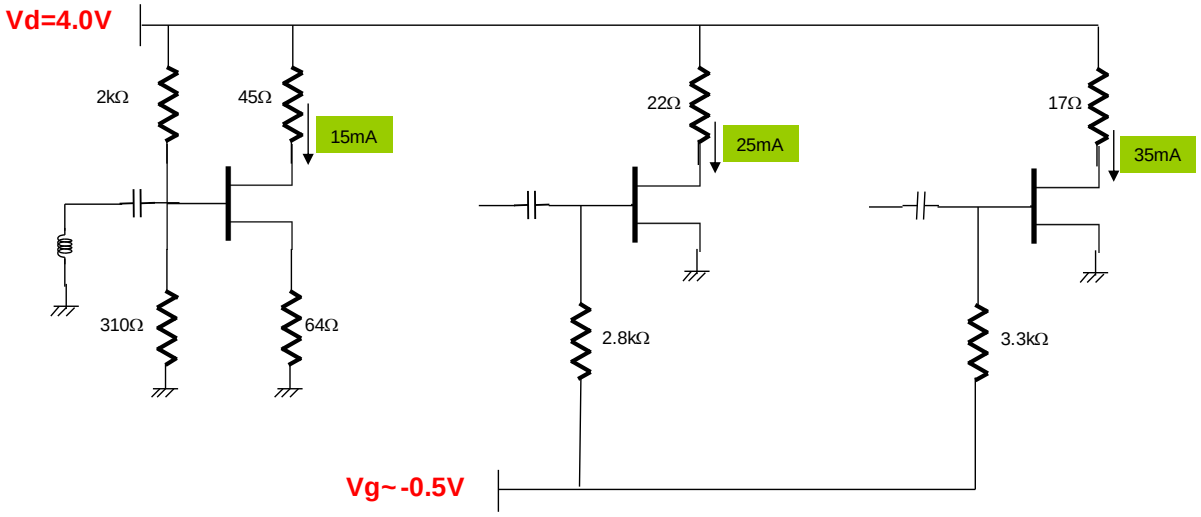
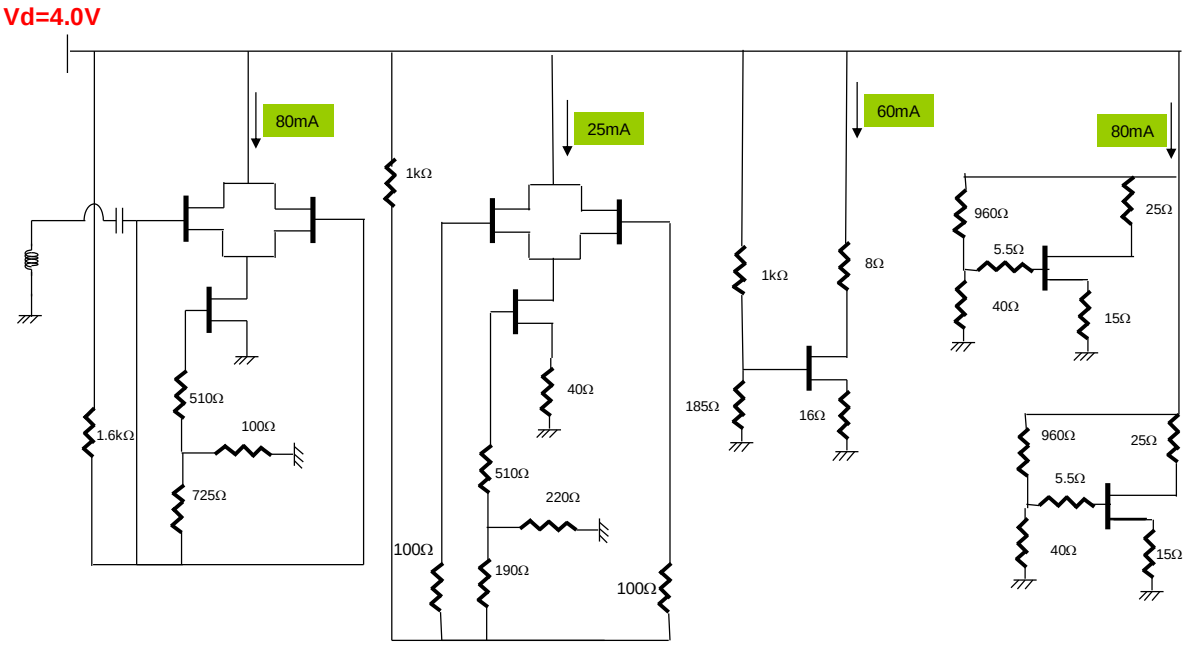
DC Schematic

LNA: 4V, 75mA



LO Buffer: 4V, 245mA



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package:	CHR3364-QEG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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