# PRELIMINARY DATASHEET

# CGY2120XUH/C1

## Ultra Low Noise C-Band Amplifier

## DESCRIPTION

The CGY2120XUH is a high performance GaAs single stage Low Noise Amplifier MMIC designed to operate on the C band.

The CGY2120XUH has an exceptionally low noise figure of 0.5 dB with 13 dB of gain. It can be used in Radar, Telecommunication and Instrumentation applications.

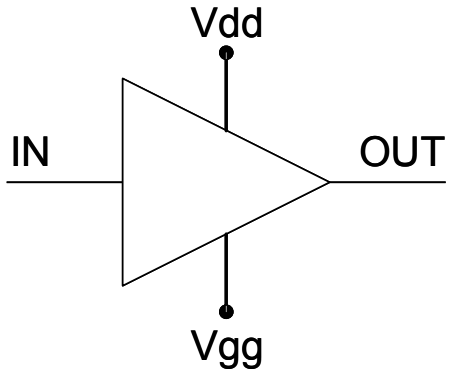
The die is manufactured using OMMIC's Advanced 70 nm gate length high Indium content MHEMT Technology. The MMIC uses gold bonding pads and backside metallisation and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

## FEATURES

- Operating Range : 5 GHz to 7 GHz
- Noise Figure : 0.5 dB at 6 GHz
- Gain : 13.2 dB at 6 GHz
- Input Return Loss : > 6 dB at 6 GHz
- Output Return Loss : > 12 dB at 6 GHz
- Chip size = 1.5 mm x 2.0 mm
- Tested, Inspected Known Good Die (KGD)
- Samples Available

## APPLICATIONS

- Radar
- Instrumentation
- Telecommunications




*Block Diagram of the CGY2120XUH Low Noise Amplifier*

RoHS Compliant

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$T_{amb}$ = 25 °C unless otherwise specified.

| Symbol | Parameter | Conditions | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Drain voltage | | 0 | 1.2 | V |
| $I_D$ | Total Drain current | | | 55 | mA |
| $V_{GG}$ | Gate supply voltage | $V_D$ open-circuited | -2.5 | 0 | V |
| $T_{stg}$ | Storage temperature | | -55 | +150 | ° C |
| $T_j$ | Junction temperature | | | +150 | ° C |
| $T_{amb}$ | Ambient temperature | | -40 | +85 | ° C |

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | UNIT |
|---|---|---|---|
| $R_{th(j-a)}$ | Thermal resistance from junction to backside ($T_a$ = 25 °C) | TBD | ° C/W |

## DC & RF CHARACTERISTICS

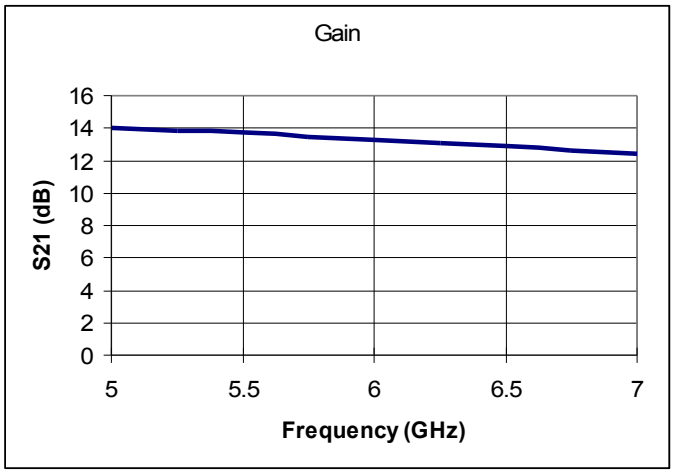
$T_{amb}$ = 25 °C, On-wafer measurement results, using 50 ⇆ RF probes unless stated otherwise.

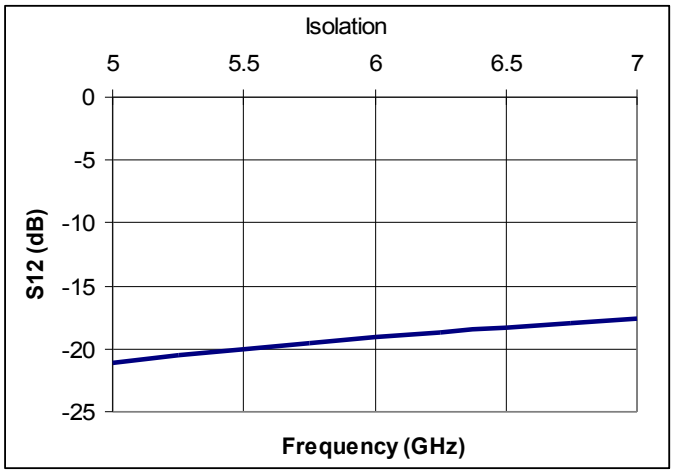
| Symbol | Parameter | Conditions | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| ***DC characteristics*** | | | | | | |
| $V_{DD}$ | Drain voltage | | | 1 | +1.2 | V |
| $I_{DD}$ | Drain current | | | 50 | | mA |
| $V_{GG}$ | Gate supply voltage | | -2.5 | -0.15 | 0 | V |
| ***RF characteristics*** | | | | | | |
| BW | Useful bandwidth | | 5 | | 7 | GHz |
| Gain | Reference Gain | F = 6 GHz | | 13.2 | | dB |
| S11 | Input return loss | | | -6.8 | -6 | dB |
| S22 | Output return loss | | | -12 | -6 | dB |
| S12 | Isolation | F = 6 GHz | | -19 | | dB |
| NF | Noise Figure | F = 6 GHz | | 0.5 | | dB |

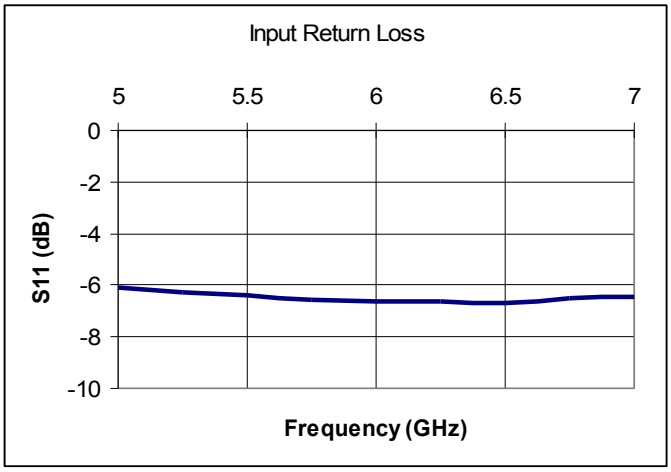
**Caution :** This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

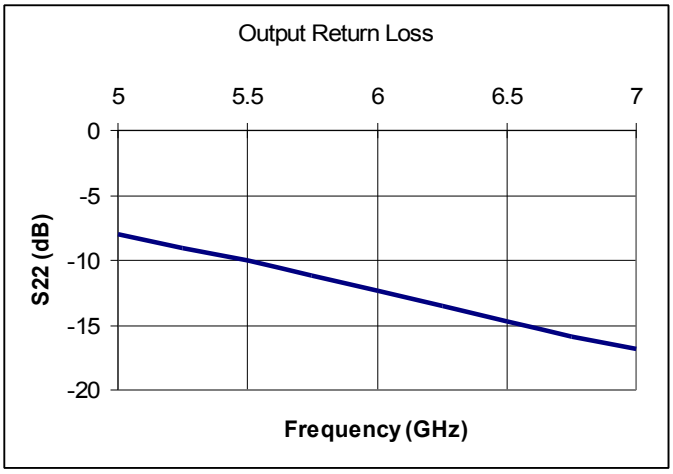
## MEASURED PERFORMANCE

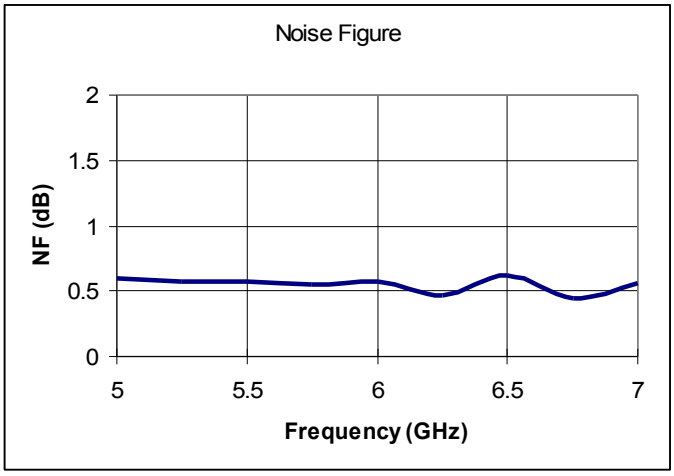
$T_{amb}$ = 25 °C, $V_{DD}$ =1V, $I_{DD}$ = 50 mA. On-wafer measurement results, using 50 ⇆ RF probes




**NB** :This product was originally designed to achieve optimal matching and NF performances with bondwires on both ends of the circuit, whereas the presented results were obtained on wafer, using 50 ⇆ RF probes.

# CGY2120XUH/C1 TYPICAL SCATTERING PARAMETERS

$T_{amb}$ = 25 °C, $V_{DD}$ =1V, $I_{DD}$ = 50 mA. On-wafer measurement results, using 50 ⇆ RF probes

| Frequency (GHz) | \|S11\| (dB) | Ang S11 (°) | \|S12\| (dB) | Ang S12 (°) | \|S21\| (dB) | Ang S21 (°) | \|S22\| (dB) | Ang S22 (°) |
|---|---|---|---|---|---|---|---|---|
| 4 | -4.823 | -80.1 | -24.05 | 132.1 | 14.28 | 155.9 | -4.839 | -90.55 |
| 4.25 | -5.201 | -86.35 | -23.13 | 124.5 | 14.25 | 147.4 | -5.589 | -97.05 |
| 4.5 | -5.529 | -91.68 | -22.42 | 117.6 | 14.2 | 139.9 | -6.326 | -103.3 |
| 4.75 | -5.919 | -96.25 | -21.65 | 110.7 | 14.09 | 131.9 | -7.209 | -110.2 |
| 5 | -6.112 | -100.1 | -21.07 | 104.7 | 14.01 | 125.2 | -8.054 | -116.9 |
| 5.25 | -6.289 | -103.2 | -20.5 | 98.56 | 13.84 | 118.3 | -9.026 | -124.2 |
| 5.5 | -6.398 | -106.5 | -20 | 93.02 | 13.72 | 112.1 | -10.03 | -132 |
| 5.75 | -6.556 | -108.1 | -19.52 | 87.41 | 13.43 | 105.9 | -11.14 | -140.3 |
| 6 | -6.655 | -110.7 | -19.09 | 82.05 | 13.29 | 99.46 | -12.33 | -149.7 |
| 6.25 | -6.648 | -112.4 | -18.67 | 77.28 | 13.07 | 94.07 | -13.5 | -160.3 |
| 6.5 | -6.664 | -114.3 | -18.32 | 72.41 | 12.85 | 88.19 | -14.68 | -172 |
| 6.75 | -6.537 | -116.1 | -17.96 | 67.58 | 12.64 | 83.06 | -15.87 | 174.1 |
| 7 | -6.469 | -118 | -17.63 | 62.74 | 12.41 | 77.66 | -16.88 | 158.4 |
| 7.25 | -6.312 | -120 | -17.29 | 57.95 | 12.17 | 72.96 | -17.59 | 140.7 |
| 7.5 | -6.243 | -121.6 | -16.97 | 53.27 | 11.92 | 67.77 | -17.84 | 121.9 |
| 7.75 | -6.087 | -123.3 | -16.68 | 49.11 | 11.68 | 63.06 | -17.5 | 104.6 |
| 8 | -5.959 | -125.3 | -16.49 | 45.39 | 11.42 | 58.21 | -16.78 | 90.01 |

# APPLICATION INFORMATION

## Typical application scheme

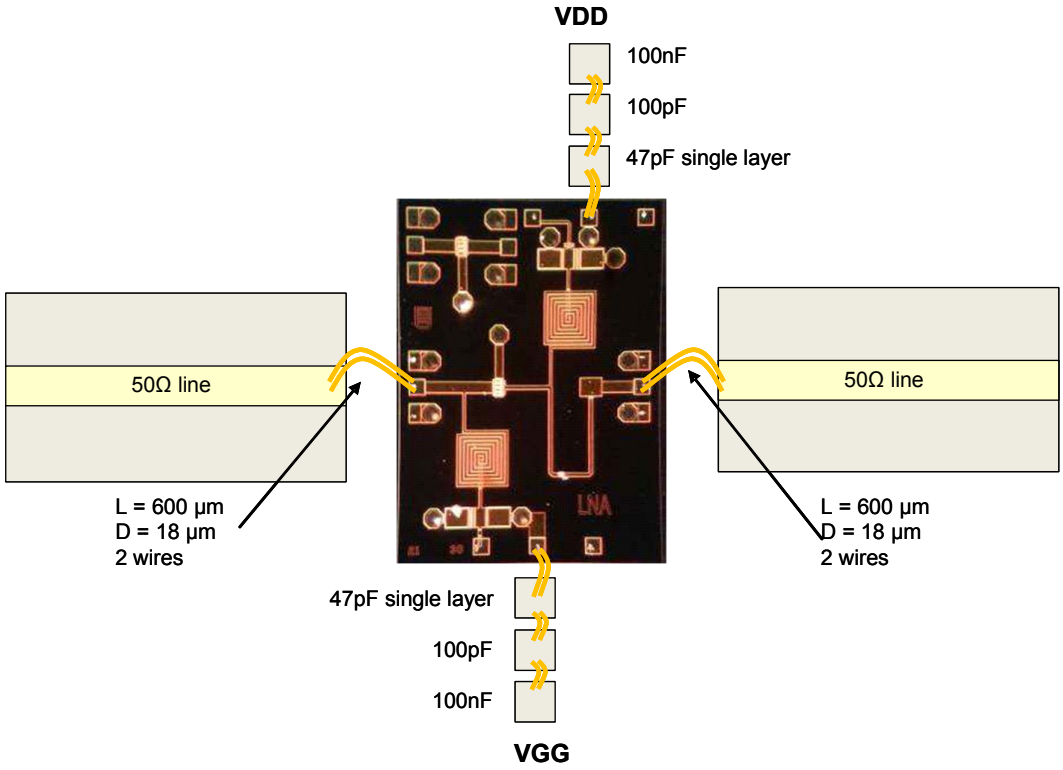
A reference module layout is shown below, where RF input and output microstrip transmission lines are used. However, coplanar transmission lines with similar performance may also be used. All path lengths and physical sizes of the components should be minimized.

All RF input and output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as small as possible to reduce parasitic inductance. Higher RF input / output inductance may result in a degradation of gain and match. Ribbon bonding technique can also be used.

All others bondings (pads $V_{DD}$ and $V_{GG}$) should be kept as short as possible.

Decoupling 47 pF and 100 pF chip capacitors (close to the chip) and 100 nF chip or SMD* capacitors (positioned at around 4mm from the chip) are used to improve the power supply rejection.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn or silver conductive epoxy material can be used for die attachment.




*CGY2120XUH/C1 module layout : Microstrip assembly*

*Surface Mount Devices

# OPERATING AND HANDLING INSTRUCTIONS

The CGY2120XUH/C1 is a very high performance MHEMT device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting and biasing conditions.

### 1- Power Supply Sequence

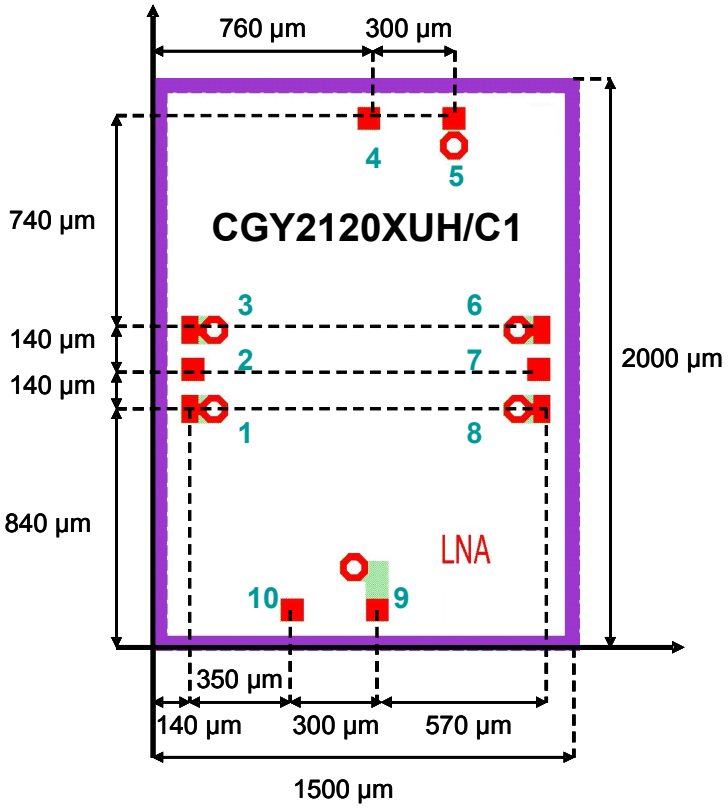
The following power supply sequence is recommended.

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting $V_{GG}$ to -2V.
c) Increase $V_{DD}$ to +1V
d) Increase the gate voltages $V_{GG}$ slowly from -2V until the drain current reaches respectively 50 mA.
e) Apply the RF input signal.

### 2- Mounting and ESD handling precautions

For high performance Integrated Circuits, such as the CGY2120XUH/C1, care must be taken when mounting GaAs MMICs so as to correctly mount, bond and hence obtain the most reliable long-term operation. The temperature, duration and material compatible with GaAs MMICs and the precautions to be taken are described in OMMIC's document "OM-CI-MV/001/PG", entitled, "Precautions for III-V products".

# PAD CONFIGURATION



## PAD POSITION

| SYMBOL | PAD | COORDINATES | | DESCRIPTION |
|---|---|---|---|---|
| | | X | Y | |
| GND | 1 | 140 | 840 | Connected to ground with on-chip via hole |
| IN | 2 | 140 | 980 | RF input |
| GND | 3 | 140 | 1120 | Connected to ground with on-chip via hole |
| $V_{DD}$ | 4 | 760 | 1860 | Drain supply voltage, must be decoupled to ground using external capacitor(s) |
| GND | 5 | 1060 | 1860 | Connected to ground with on-chip via hole |
| GND | 6 | 1360 | 1120 | Connected to ground with on-chip via hole |
| OUT | 7 | 1360 | 980 | RF Output |
| GND | 8 | 1360 | 840 | Connected to ground with on-chip via hole |
| GND | 9 | 790 | 140 | Connected to ground with on-chip via hole |
| $V_{GG}$ | 10 | 490 | 140 | Gate supply voltage, must be decoupled to ground using external capacitor(s) |

## MECHANICAL INFORMATION

| PARAMETER | | VALUE |
|---|---|---|
| Size | | 1500 x 2000 µm |
| Thickness | | 100 µm |
| Backside material | | TiAu |
| Passivation | | PECVD deposited $Si_3N_4$ |
| Bonding pad dimensions | GND RF | 80 x 100 µm |
| | IN, OUT, $V_{DD}$, $V_{GG}$, GND DC | 80 x 80 µm |

## NOTE

The die size and all pad positions refer to the mask layout, with (X=0, Y=0) at the bottom left corner of the layout. For each pad, the (X,Y) coordinates refer to the center of the pad.
Wafers are diced by sawing, with a sawline width of 35 µm (± 5 µm). A misalignment of the sawline with the middle of the dicing street (± 20 µm on all sides) may also result in a variation of ± 20 µm of the actual positions of the pads on the diced chip and an additional tolerance of ± 40 µm on the die size.

## DEFINITIONS

**Limiting values definition**
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## ORDERING INFORMATION

| Generic type | Package type | Version | Description |
|---|---|---|---|
| CGY2120XUH | Bare Die | C1 | Ultra Low Noise C-Band Amplifier |

RoHS Compliant

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