gRSC0013 C
E-band RX MMIC
81-86 GHz

Features

- E2-band coverage
- 25 dB conversion gain
- 6 dB NF
- Direct or IF down conversion

Typical applications

- E-band point-to-point radio
- Active imaging
- Automotive radar
- Fiber over radio

Description

gRSC0013 is a complete highly integrated receiver for E-band radio applications. The multifunctional chip has a x6 frequency multiplier, mixer, IF amplifier and low noise amplifier integrated on the chip. The differential IQ mixer is highly linear with low conversion loss. The frequency multiplier has low spuriouses and flat output power throughout the entire E-band. The LNA has high gain, low noise figure and being linear, making the receiver suitable for 64+ QAM modulation.

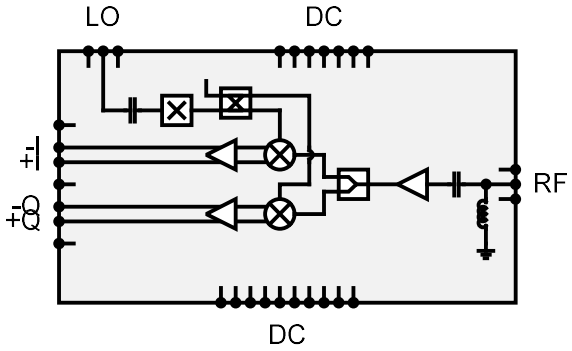

Figure 1. Block diagram of the receiver.

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Electrical performance

Table 1. Electrical performance T_A=25°C

Parameter	Min	Typ	Max	Unit
RF frequency	81		86	GHz
IF Frequency	DC		10	GHz
LO input frequency	11.8		14.3	GHz
LO input power	8	10	12	dBm
LO multiplication factor		6		
Conversion gain[1]	20	25	30	dB
LO power at RF port			-40	dBm
Image Rejection Ratio (IRR)	20	30		dB
Input referred P1dB	tbd			dBm
OIP3	20	24		dBm
IIP3[2]	-7	-5		dBm
OIP2	35	45		dBm
IIP2	10	20		dBm
NF[3]		5.5	6	dB
RF return loss	8	10		dB
IF return loss	tbd			dB
LO return loss	10	14		dB
Power consumption x6+LNA		1220		mW

Measured performance

Measurements have been performed on-wafer with RF input power = -30 dBm/tone, tone separation = 10 MHz, IF frequency = 1 GHz, T_A = 25°C and typical bias settings if not specified differently.

[1] Gain temperature coefficient is -0.05 dB/C.

[2] IIP3 can be improved with reduced gain of the LNA.

[3] The receiver noise figure is calculated using the measurement data from the LNA.

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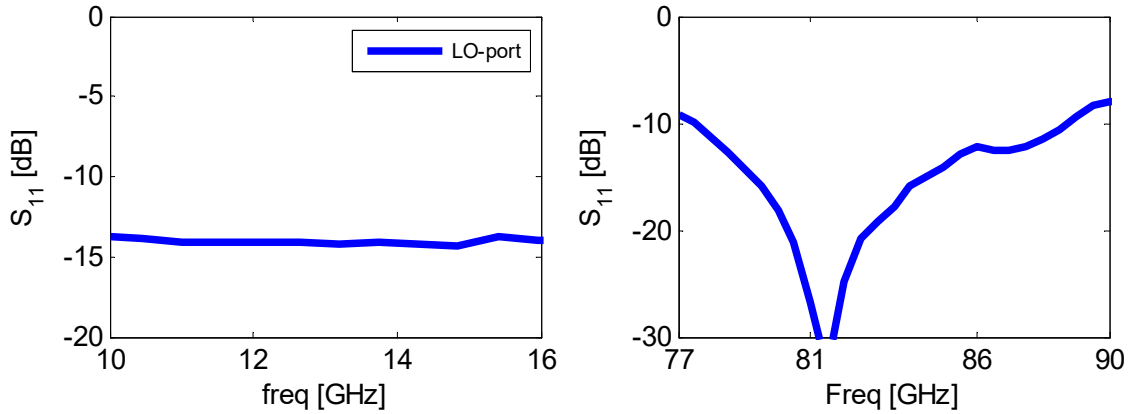

Figure 2. (Left): Input matching of the LO-port. (Right): Input matching of the LNA.

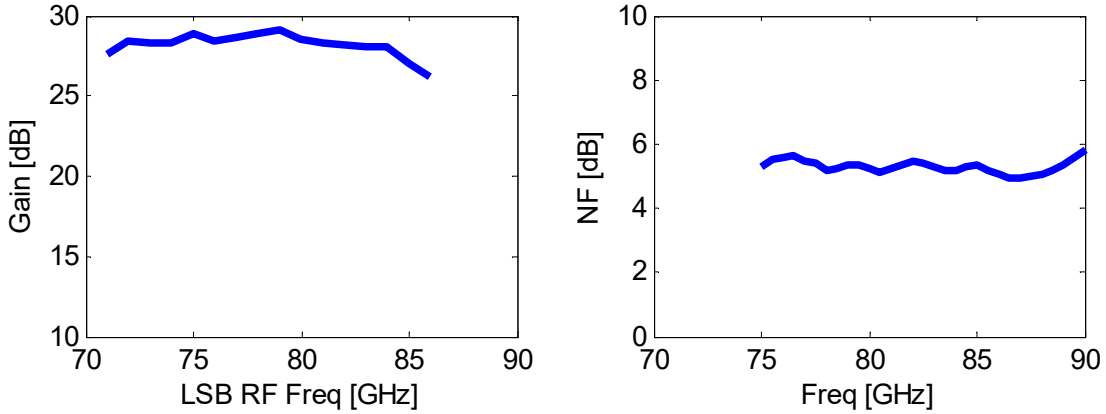

Figure 3. (Left): Conversion gain vs frequency. (Right): Measured NF of the LNA.

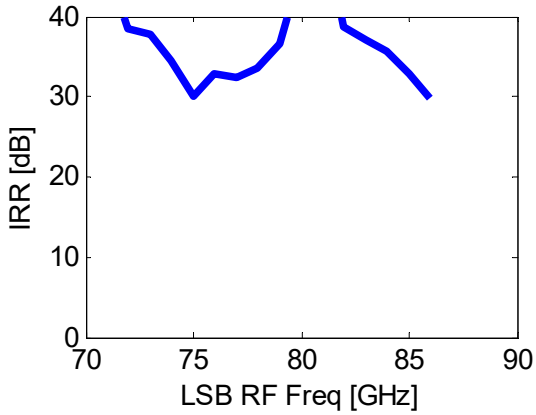

Figure 4. (Left): IRR vs frequency.

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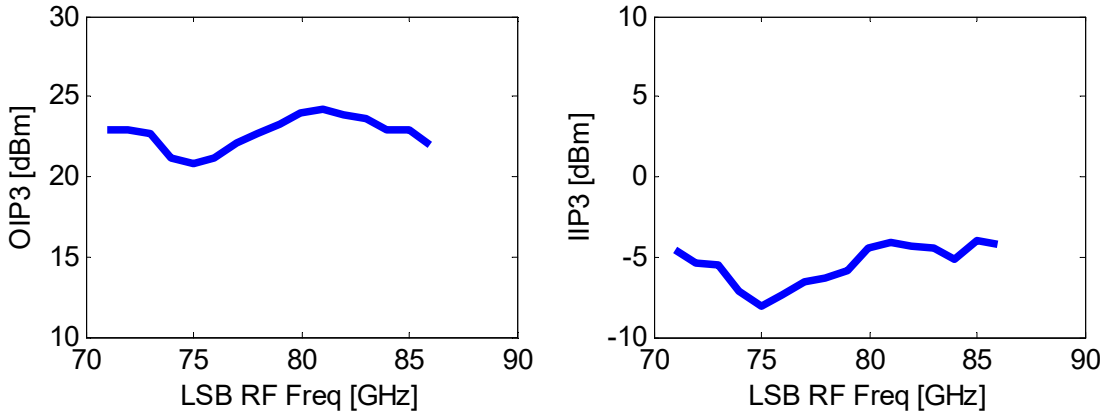

Figure 5. (Left): OIP3 vs frequency. (Right): IIP3 vs frequency.

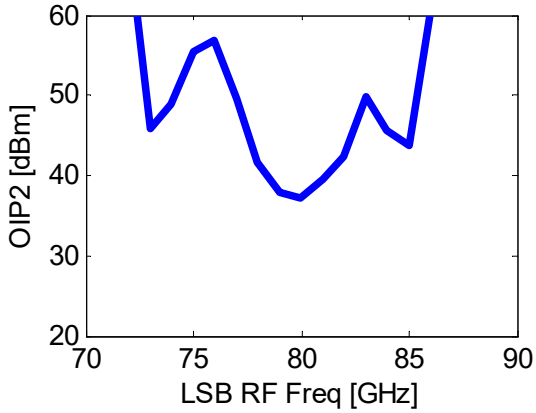

Figure 6. (Left): OIP2 vs frequency.

Settings

The bias sequence is to first apply all gates (VG…) followed by all drains (VD…). The typical drain current should be obtained by adjusting the corresponding gate. All stated drain currents are when all input signals are off.

Table 2. Electrical settings on connector P1

Connector P1	Pad No.	Settings	Function
GND	1		Ground
RF	2	Z_0 = 50 Ohm, AC coupled	Input
GND	3		Ground

Table 3. Electrical settings on connector P2

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Connector P2	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
VG_X3	1	-0.55	-0.45	-0.35	Input
VG_X2	2	-0.9	-0.8	-0.7	Input
VD_X	3	3.2	3.3 / 45	3.4 / 70[4]	Input
GND	4				Ground
VG_AMP	5	-0.6	-0.4	-0.2	Input
VD_AMP	6	3.2	3.3 / 45	3.4 / 80[4]	Input
VG_MIX	7	-1.0	-0.8	-0.6	Input

Table 4. Electrical settings on connector P3

Connector P3	Pad No.	Settings	Function
GND	1		Ground
LO	2	Z_0 = 50 Ohm, AC coupled	Input
GND	3		Ground

Table 5. Electrical settings on connector P4

Connector P4	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
VD3_LNA[5]	1	4.9 / 113	5 / 123	5.1 / 133	Input
VS3_LNA[5]	2	-1.6 / 110	-1.5 / 120	-1.4 / 130	Input
VD2_LNA	3	1.9	2.0 / 65	2.1 / 120[4]	Input
GND	4				Ground
VG2_LNA	5	-0.7	-0.5	-0.3	Input
VD1_LNA	6	1.1	1.2 / 10	1.3 / 30[4]	Input
VG1_LNA	7	-0.8	-0.6	-0.4	Input

Table 6. Electrical settings on connector P5

Connector P5	Pad No.	Settings	Function

[4] Maximum current level before damage. Not for improved performance.

[5] The current on VD3_LNA needs a sink lower than ground, i.e. VS3_LNA. The current difference between ID3_LNA and IS3_LNA should be in the order 3±2 mA.

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GND	1		Ground
I+	2	Z_0 = 100 Ohm differential impedance, DC coupled. Output DC voltage level is 3±0.5 V.	Output
I-	3		Output
GND	4		Ground
Q+	5	Z_0 = 100 Ohm differential impedance, DC coupled. Output DC voltage level is 3±0.5 V.	Output
Q-	6		Output
GND	7		Ground

Table 7. Absolute Maximum Ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
RF in	+7 dBm
LO input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

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Outline drawing

Mechanical drawing with pad locations is also available in dxf-file format on the web. Substrate thickness is 50 µm (GaAs).

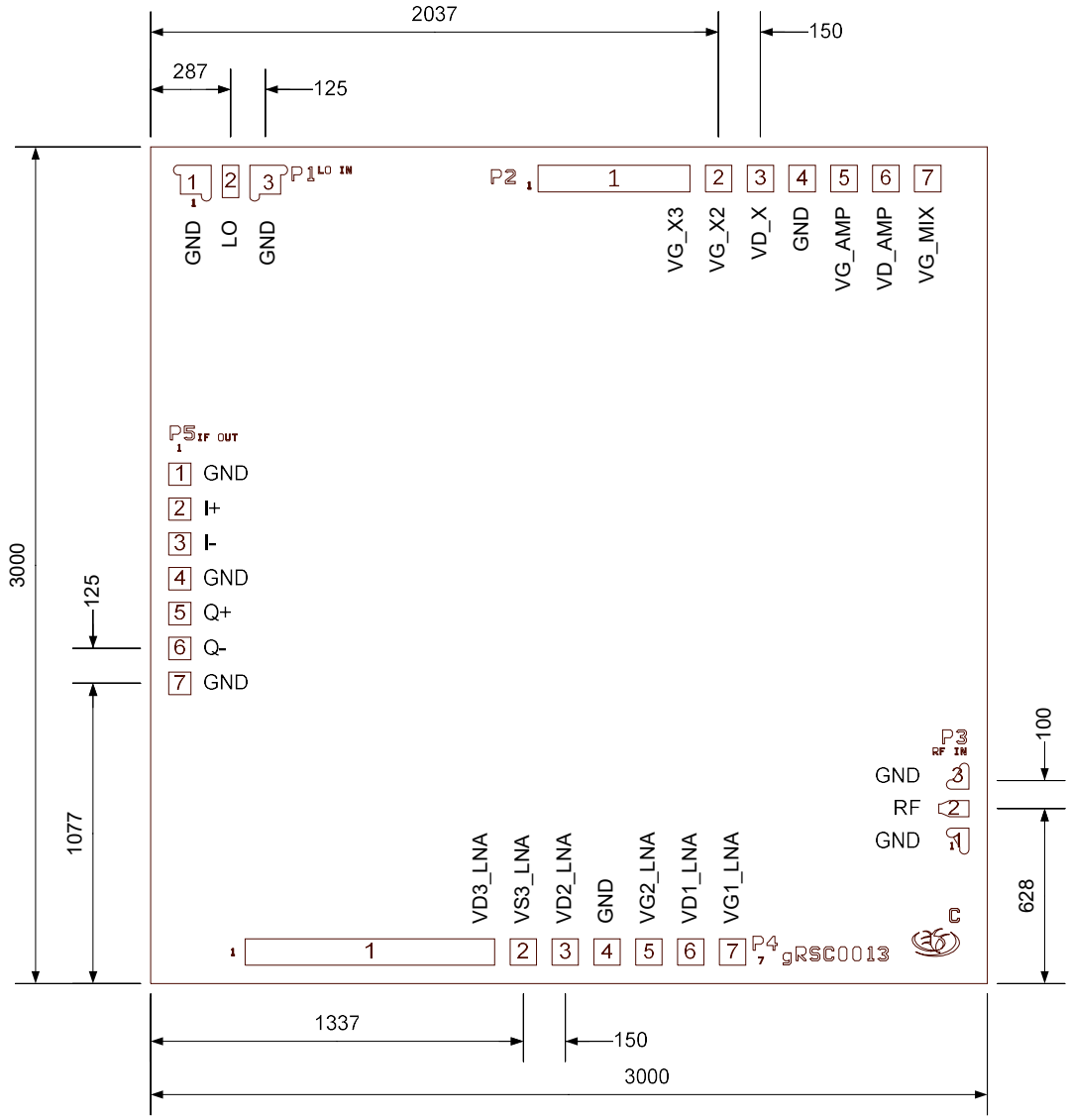

Figure 7. Outline drawing of the gRSC0013 MMIC. Dimensions are in um.

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