ZETTA SD NAND Product Datasheet

Commercial Grade

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1. Product Description

Zetta SD NAND is an embedded storage solution designed in a LGA8 package form. The operation of SD NAND is similar to an SD card which is an industry standard.

SD NAND consists of NAND flash and a high-performance controller. 3.3V supply voltage is required for the NAND area (VCC). SD NAND is fully compliant with SD3.0 interface, which is utilized by most of general CPU. The advantages of the SD NAND include high quality, low power consumption and cost performance.

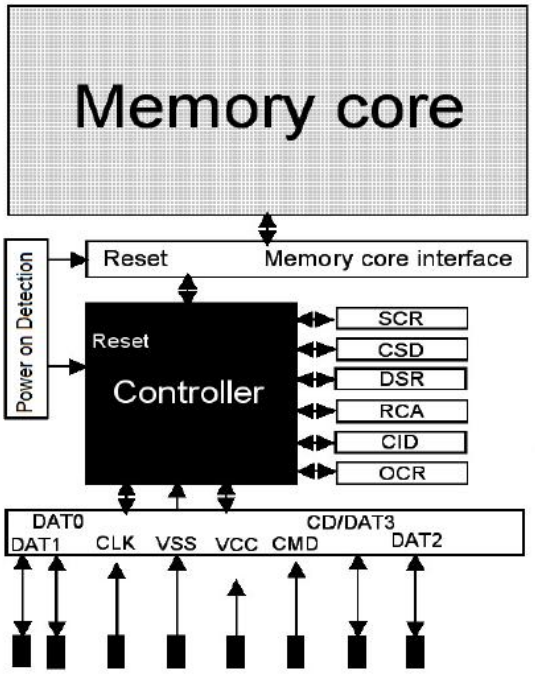
2. Product List

Capacity	Part number	Package	Size	Temp. Range
8Gb (MLC)	ZDSD08GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25°C to +85°C
16Gb (MLC)	ZDSD16GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25°C to +85°C
32Gb (MLC)	ZDSD32GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25°C to +85°C
64Gb (MLC)	ZDSD64GLGEAG-R	LGA8 (Land Grid Array)	8x6.2mm	-25°C to +85°C

3. Features

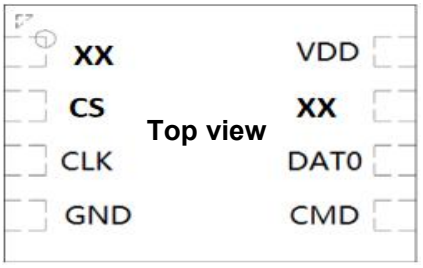
- √ Support up to 208Mhz clock frequency
- √ Support 1/4 bit mode
- √ Built-in HW ECC Engine and highly reliable NAND management mechanism
- √ High Speed model, Speed class 4/class 6/class 8/class10 supported.
- √ Smaller package LGA8 (Land Grid Array)
- √ Operation Conditions Temperature Range: Extended Ta = -25°C to +85°C
- √ Storage Conditions Temperature Range: Tstg = -65°C to +150°C

4. Block Diagram



5. Pin Assignments(SD Mode& SPI Mode)

SD Mode



SPI Mode

SD 4-bit mode		SD 1-bit mode		SPI mode	
CD/DAT[3]	Data line 3	N/C	Not Used	CS	Card Select
CMD	Command line	CMD	Command line	DI	Data input
GND	Ground	GND	Ground	GND	Ground
VDD	Supply voltage	VDD	Supply voltage	VDD	Supply voltage
CLK	Clock	CLK	Clock	SCLK	Clock
DAT[0]	Data line 0	DATA	Data line	DO	Data output
DAT[1]	Data line 1	N/C	Not Used	NC	Not Used
DAT[2]	Data line 2	N/C	Not Used	NC	Not Used

6. Bus Protocol

6.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

Multiplied SD cards connections are available to the host. Common VDD, VSS and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each device from host.

This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command: a command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

Response: a response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction (refer to Figure 1). This type of bus transaction transfers their information directly within the command or response structure. In addition, some operations have a data token.

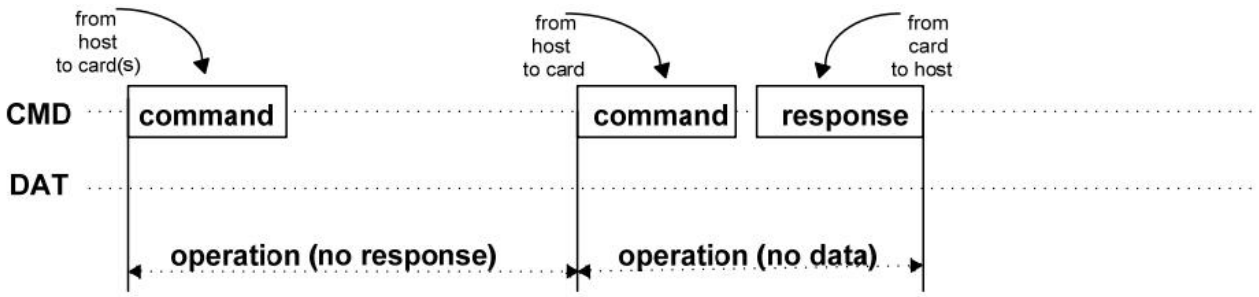


Figure 1: “no response” and “no data” Operations

Command tokens have the following coding scheme(refer to Figure 2).,Each command token is preceded by a start bit (0) and succeeded by an end bit (1). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated.

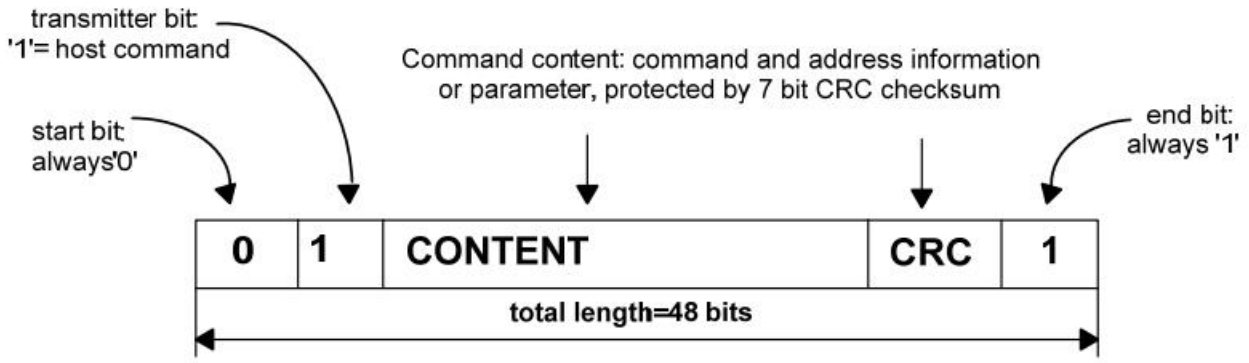
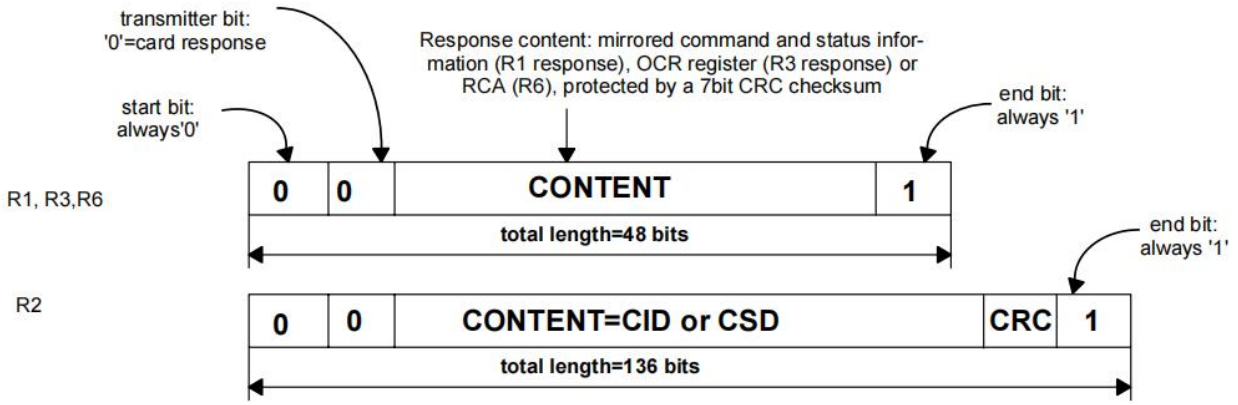


Figure 2: Command Token Format

Response tokens depending on their content. The token length is either 48 or 136 bits. (refer to Figure 3)



. **Figure 3: Response Token Format**

Data transfers to/from the SD Memory Card are done in blocks. Data blocks are always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode (refer to Figure 4).

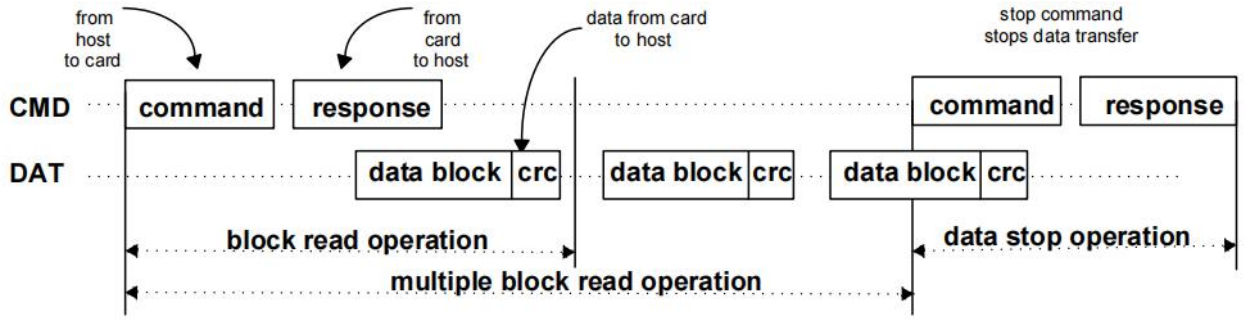


Figure 4: (Multiple) Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the data line (see Figure 5) .

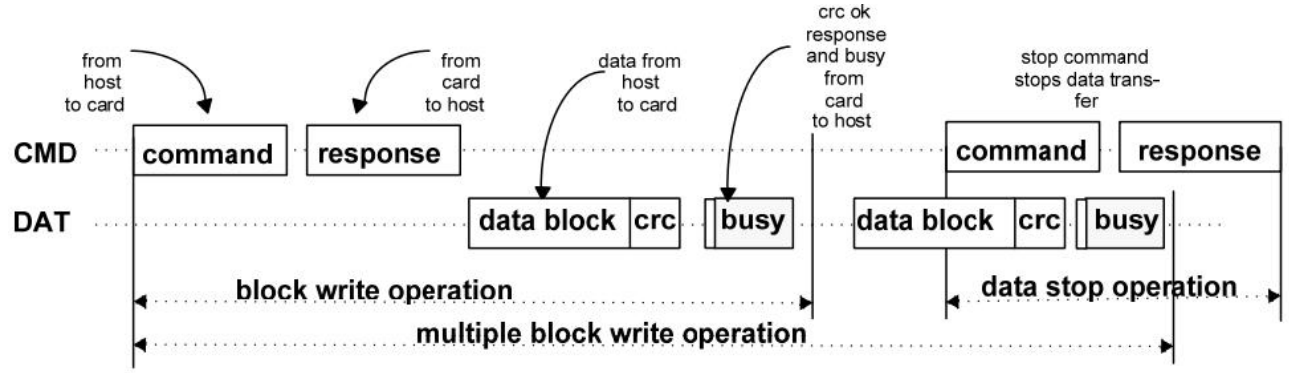


Figure 5: (Multiple) Block Write Operation

6.2 Card Initialization and Identification Process

6.2.1 SD MODE:

After the bus is activated the host starts card initialization and identification process. The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports High Capacity SD Memory card. The HCS (Host Capacity Support) bit set to 0 indicates that the host does not support High Capacity SD Memory card.

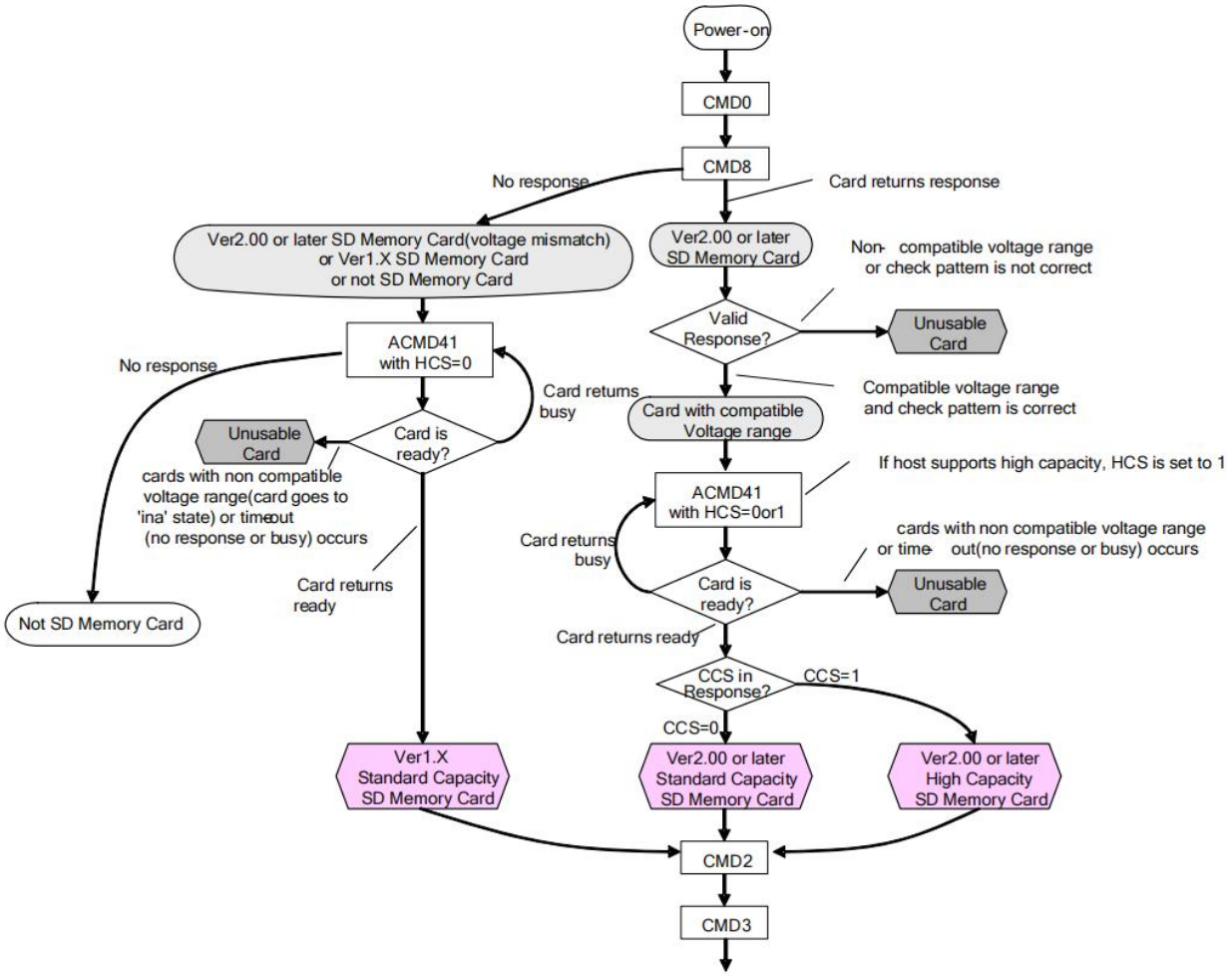


Figure 6: Card Initialization and Identification Flow (SD2.0 mode)

SD3.0 initial flow for UHS-I(IO 1.8v) switch

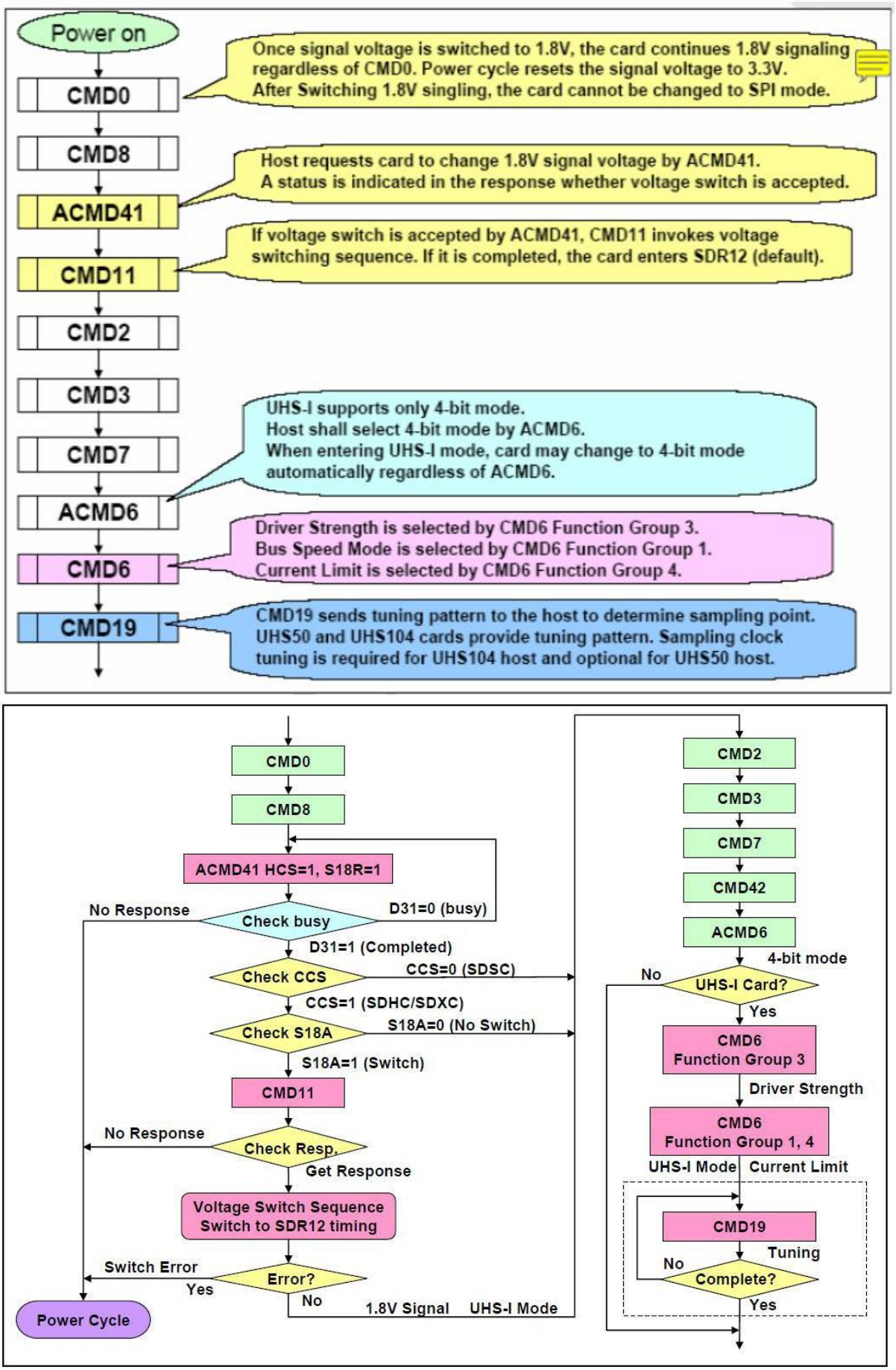


Figure 7: Card Initialization and Identification Flow (SD3.0 mode)

6.2.2 SPI MODE:

The SD Card will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response. The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available.

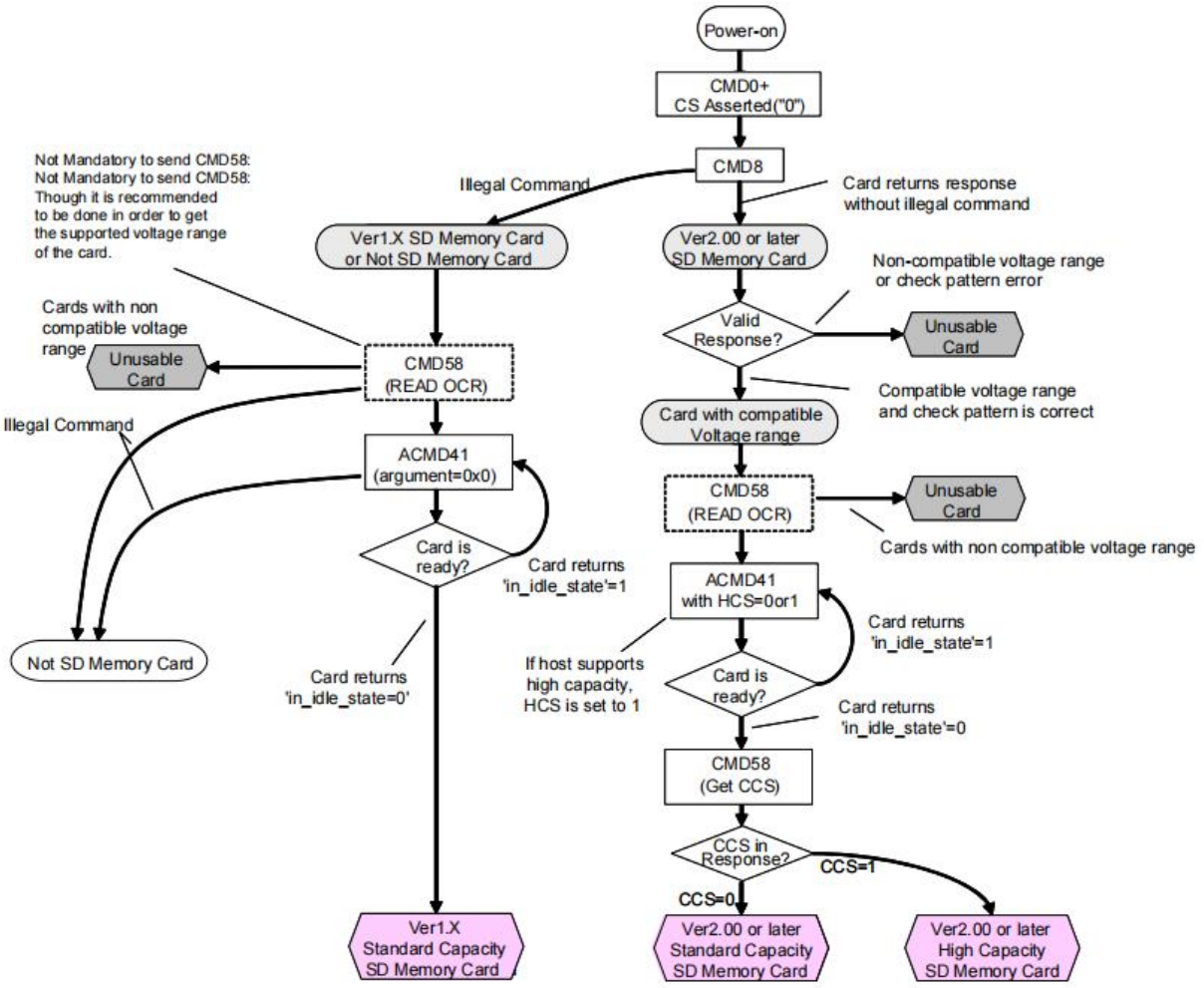


Figure 8: SPI Mode Initialization Flow

6.3 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected/deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width.

In order to change the bus width two conditions shall be met:

a) The card is in ‘tran state‘ (no data is transferred).

b) The card is not locked

A locked card will responds to ACMD6 as illegal command.

6.4 DC Characteristics

DC Characteristics

Item		Symbol	MIN.	MAX.	Unit	Note
Supply Voltage		VDD	2.7	3.6	V	
Input Voltage	High Level	VIH	VDD×0.625	VDD+0.3	V	
	Low Level	VIL	VSS-0.3	VDD×0.25	V	
Output Voltage	High Level	VOH	VDD×0.75	—	V	IOH = -2mA , VDD=V DD min
	Low Level	VOL	—	VDD×0.125	V	IOL = 2mA , VDD=V DD min
Standby Current		ICC1	—	0.2	mA	VDD = 3.3V, Clock STOP, Ta= 2 5 ℃
Operation Current (*)	Write	ICC2	—	25	mA	3.3V / 25MHz,50MHz
	Read		—	25		
Input Voltage Setup Time		Vrs	—	250	ms	From 0V to VDD min

Peak Voltage and Leak Current

Item	Symbol	Min.	Max.	Unit	Note
Peak voltage on all lines		-0.3	VDD+0.3	V	
Input Leakage Current for all pins		-10	10	uA	
Output Leakage Current for all outputs		-10	10	uA	

Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	RCMD RDAT	10	100	kΩ	
Total bus capacitance for each signal line	CL	—	40	pF	1 card CHOST+CBUS≤30pF
Card capacitance for signal pin	CCARD	—	10	pF	
Pull up Resistance inside card (pin1)	RDAT3	10	90	kΩ	
Capacity Conneted to Power line	CC	—	5	uF	

Note: WP pull-up (Rwp) Value is depend on the Host Interface drive circuit.

7 Internal Information

7.1 Registers

The SD NAND has six registers and SD Status information: OCR, CID, CSD, RCA,DSR, SCR and SD Status.

DSR IS NOT SUPPORTED in this card.

SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative CardAddress
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Cards special features
SD Status	512	Status bits and Card features

7.1.1 OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.

OCR register definition

OCR bit position	OCR Fields Definition	
0-3	reserved	
4	reserved	
5	reserved	
6	reserved	
7	Reserved for Low Voltage Range	
8	reserved	
9	reserved	
10	reserved	
11	reserved	
12	reserved	
13	reserved	
14	reserved	
15	2.7-2.8	VDD Voltage Window
16	2.8-2.9	
17	2.9-3.0	
18	3.0-3.1	
19	3.1-3.2	
20	3.2-3.3	
21	3.3-3.4	
22	3.4-3.5	
23	3.5-3.6	
24-29	reserved	
30	Card Capacity Status (CCS)[1]	
31	Card power up status bit (busy)[2]	

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.

7.1.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

CID Register

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always 1	-	1	[0:0]

7.1.3 CSD Register

CSD is Card-Specific Data register provides information on 128bit width. Some field of this register can writable by PROGRAM_CSD (CMD27).

CSD Register(2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

Cell Type:R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable

Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN" .

Host System should refer this value before one data block size erase.

7.1.4 RCA Register

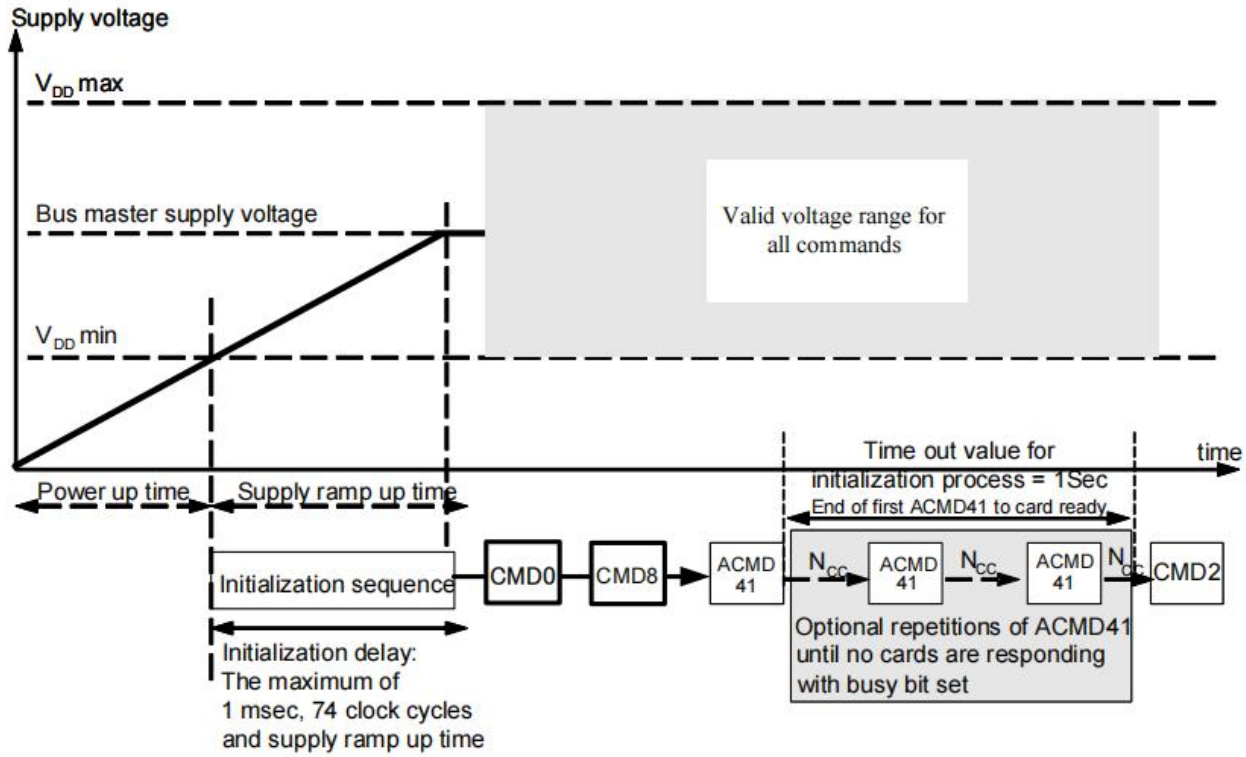
The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

8 Power Scheme

8.1 Power Up

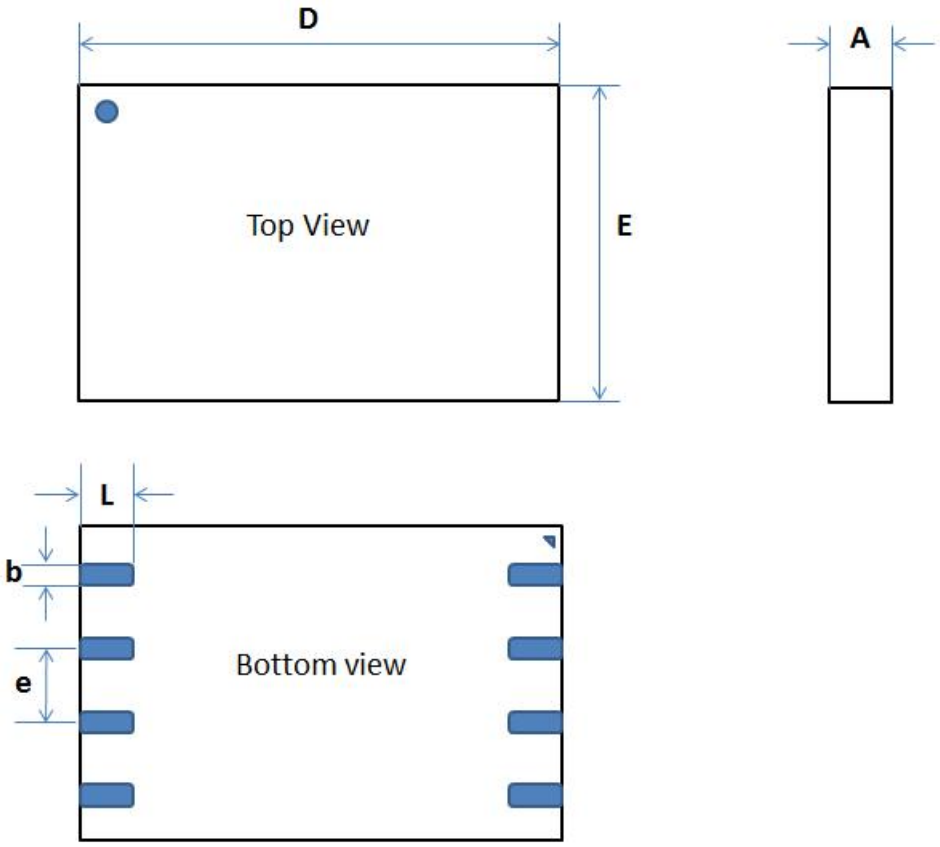
Power up time is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

Supply ramp up time provides the time that the power is built up to the operating level (the bus master supply voltage) and the time to wait until the SD card can accept the first command,The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

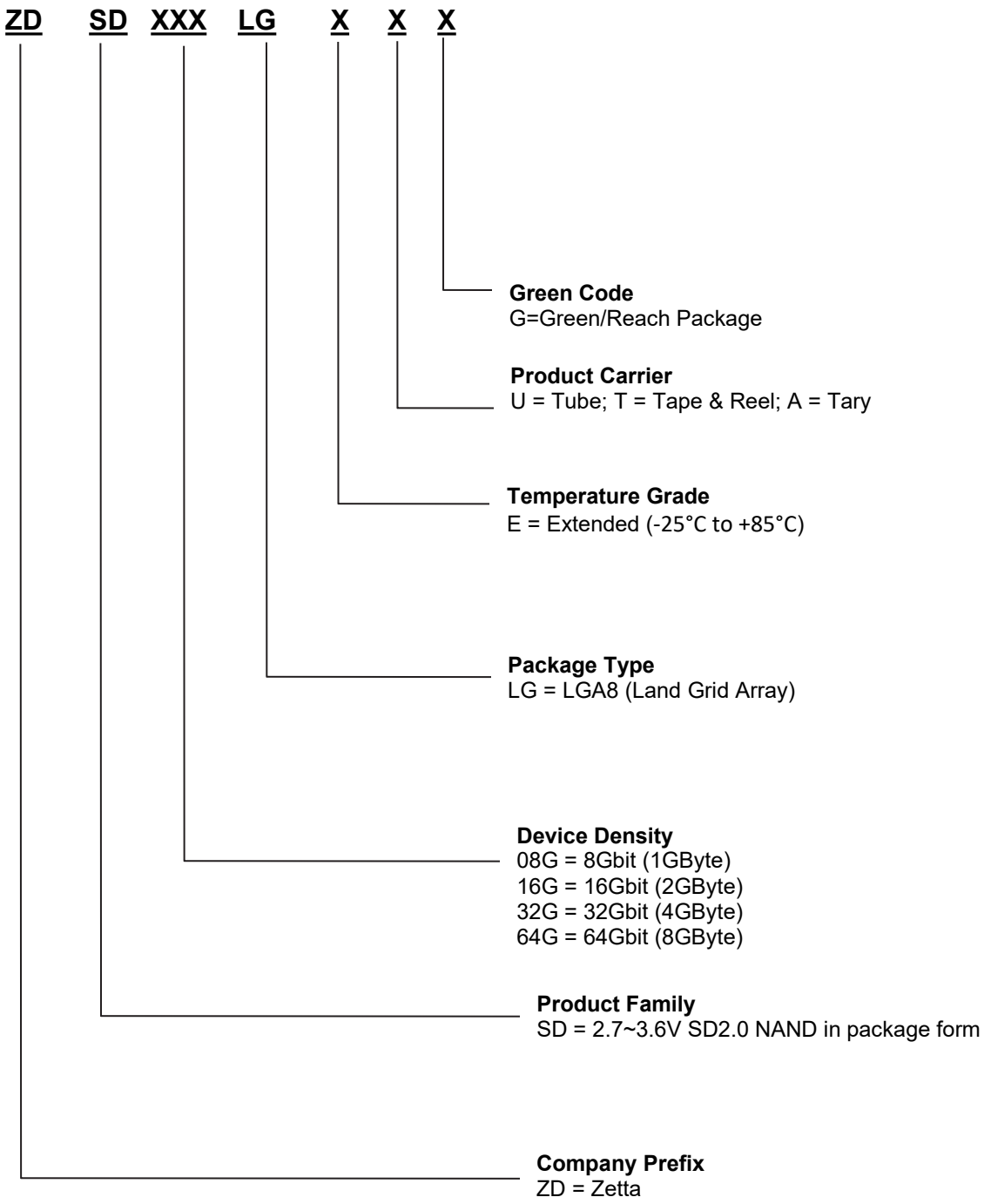


9. Package Dimensions

LGA8 (SLC 8x6mm/MLC 8x6.2mm) (Land Grid Array)



Symbol / Unit		A	b	D	E-SLC	E-MLC	e	L
Mm	Min	0.75	0.55	7.95	5.90	6.10		0.75
	Norm	0.80	0.60	8.00	6.00	6.20	1.27	0.80
	Max	0.85	0.65	8.05	6.10	6.30		0.85

10. Ordering Information

The ordering part number is formed by a valid combination of the following