

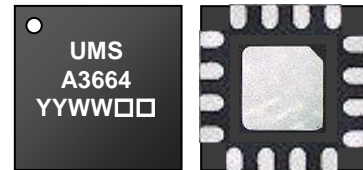
5-21GHz Driver Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA3664-QAG is a two-stage self-biased general purpose monolithic medium power amplifier.

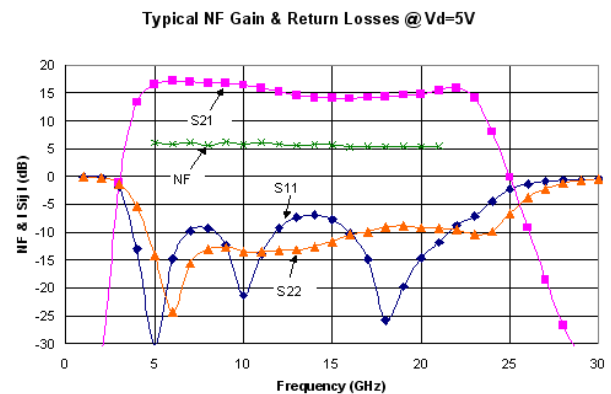
The circuit is manufactured with a power pHEMT process: 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.



It is available in leadless SMD package.

Main Features

- Broadband performances: 5-21GHz
- 20.5dBm saturated output power
- 15dB gain
- DC bias: Vd=5Volt @ Id=120mA
- 16L-QFN3x3
- MSL1



Main Characteristics

Tamb = +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5		21	GHz
G	Small signal gain	12.5	15		dB
Psat	Saturated Output Power	19	20.5		dBm
Id_small_signal	Bias current		120		mA

ESD Protections: Electrostatic discharge sensitive device observe handling precautions

Electrical Characteristics

Tamb = +25°C, Vd= +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5		21	GHz
G	Small signal gain	12.5	15		dB
P1dB	CW output power at 1dB compression	17.5	19.5		dBm
Psat	Saturated Output Power	19	20.5		dBm
C/I3	C/I3 @ Pin/tone=-8dBm , Vd=5V 5 to 7.5GHz 7.5 to 16.5GHz 16.5 to 20GHz		40 34 33		dB
dBS11	Input Return Loss		-8	-6	dB
dBS22	Output Return Loss		-10	-8	dB
NF	Noise figure		6		dB
Vd	Drain Supply Voltage		5		V
Id_small signal	Bias current		120		mA

These values are representative of onboard measurements as defined on the drawing 96272 (see below).

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vds	Drain bias voltage_small signal	6.0	V
Ids	Drain bias current_small signal	175	mA
Vg	Gate bias voltage	-2 to +0.4	V
Ig	Gate bias current	0.7	mA
Vgd	Maximum negative gate drain Voltage (Vg-Vd)	-8	V
Pin	Maximum continuous input power	+10	dBm
Ta	Operating temperature range	-40 to +85	°C
Tj	Junction temperature	175	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

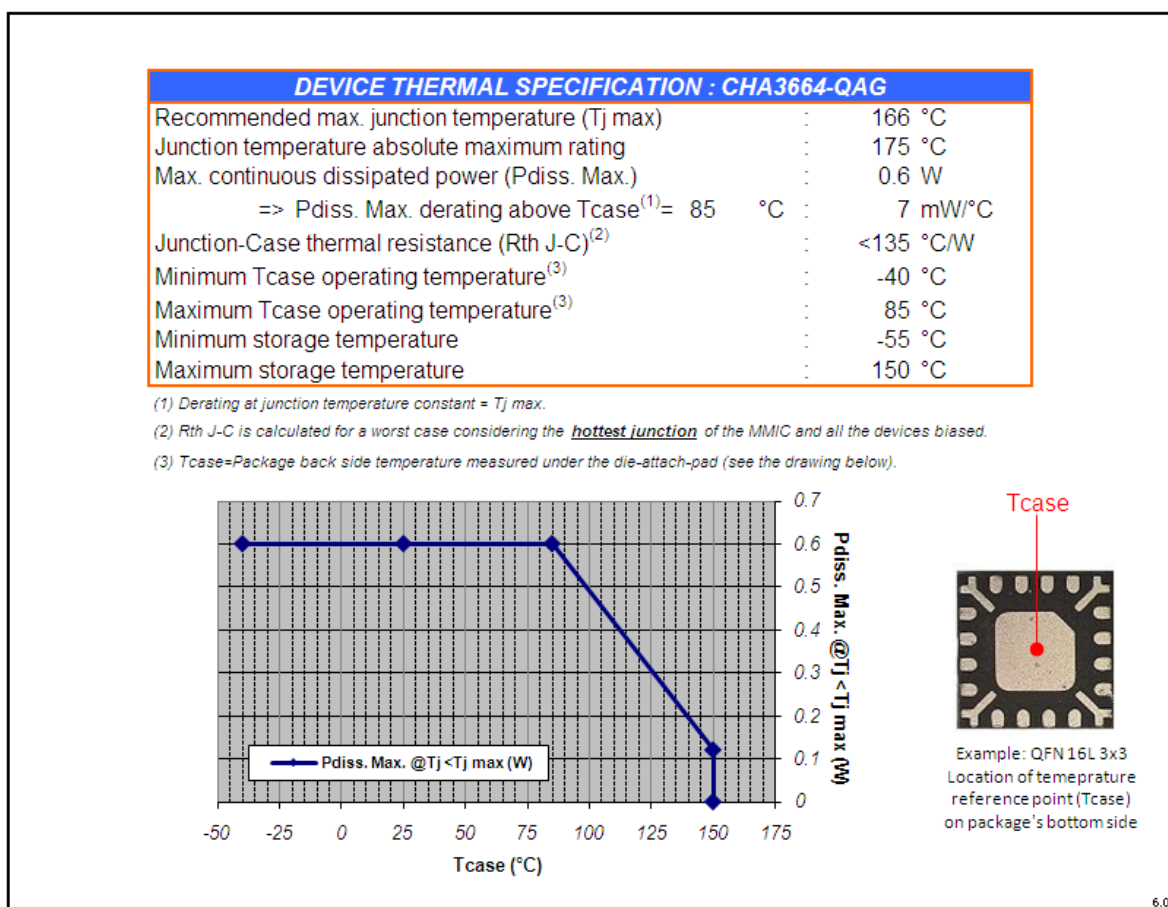
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (T_{case}) as shown below.

The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max}$) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters for low current configuration

Tamb = +25°C, Vd = +5V

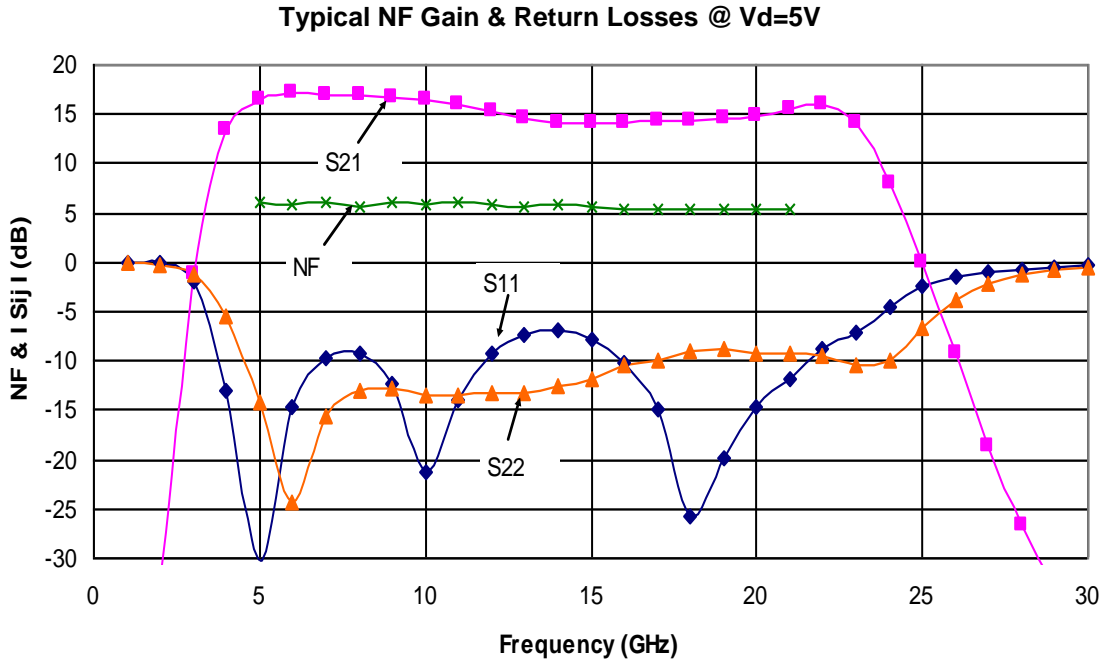
F (GHz)	S11	S11	S12	S12	S21	S21	S22	S22
	dB	∠°	dB	∠°	dB	∠°	dB	∠°
1	0.0	-37.5	-65.4	93.7	-39.0	165.1	-0.1	-31.1
2	-0.1	-79.3	-65.8	135.7	-31.9	-53.5	-0.2	-64.7
3	-1.9	-138.9	-52.1	94.9	-1.2	-108.9	-1.3	-106.0
4	-13.1	153.7	-41.7	65.8	13.3	114.1	-5.4	-151.3
5	-30.2	77.2	-37.7	-13.0	16.5	7.1	-14.2	178.5
6	-14.8	-20.8	-37.3	-71.7	17.2	-74.2	-24.3	-111.7
7	-9.8	-68.0	-38.1	-121.2	17.0	-140.4	-15.6	-96.2
8	-9.3	-109.4	-37.9	-165.4	16.8	162.3	-13.1	-119.4
9	-12.3	-155.3	-38.2	151.2	16.7	108.7	-12.7	-142.6
10	-21.4	119.1	-37.9	105.3	16.4	56.6	-13.5	-163.2
11	-13.9	-7.9	-39.2	65.9	15.9	6.9	-13.5	-177.4
12	-9.3	-55.2	-41.0	27.4	15.2	-40.5	-13.3	151.9
13	-7.4	-90.7	-41.9	0.4	14.6	-85.0	-13.2	115.2
14	-7.0	-124.1	-44.1	-30.3	14.2	-128.6	-12.6	72.9
15	-7.8	-158.0	-45.2	-59.9	14.1	-172.4	-11.7	34.5
16	-10.2	164.3	-45.5	-91.7	14.0	143.0	-10.4	-0.6
17	-14.9	119.7	-46.8	-133.5	14.2	96.1	-9.9	-32.4
18	-25.9	25.4	-43.7	-163.7	14.4	47.1	-9.1	-62.1
19	-19.8	-127.4	-42.3	154.6	14.6	-5.0	-8.9	-94.7
20	-14.6	156.5	-39.5	109.2	14.8	-59.3	-9.2	-126.0
21	-11.8	70.6	-37.4	56.3	15.5	-120.0	-9.2	-158.6
22	-8.9	-31.3	-37.6	-2.7	16.0	166.6	-9.6	155.8
23	-7.1	-163.9	-40.1	-95.5	14.1	75.3	-10.5	89.3
24	-4.5	72.5	-45.4	132.9	8.0	-13.1	-9.9	13.5
25	-2.3	-5.0	-54.2	125.4	-0.2	-87.2	-6.6	-42.0
26	-1.4	-56.0	-40.4	84.2	-9.2	-149.4	-3.8	-82.6
27	-0.9	-91.1	-42.1	37.8	-18.6	158.2	-2.2	-114.4
28	-0.7	-118.5	-42.3	31.3	-26.8	109.6	-1.2	-138.2
29	-0.6	-139.9	-40.7	31.6	-32.5	63.0	-0.7	-156.8
30	-0.3	-158.8	-37.7	5.0	-34.7	16.6	-0.4	-171.3

Refer to the “definition of the Sij reference planes” section below

Typical PCB Measured Performance

Tamb = +25°C

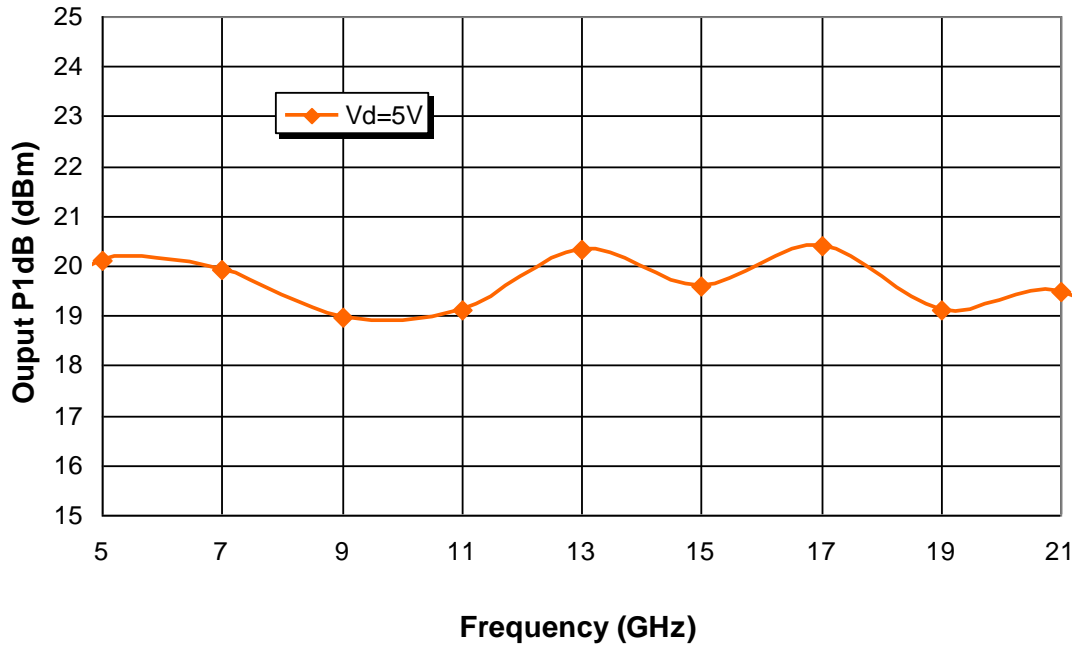
Performances obtained in the package access planes
 Refer to the “definition of the Sij reference planes” section below



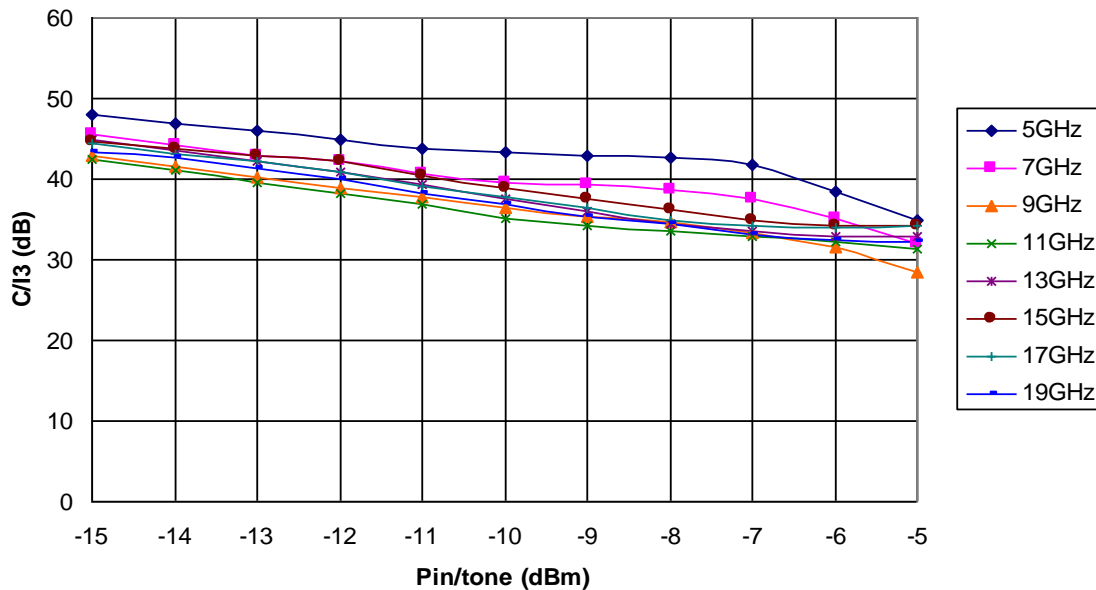
Typical PCB Measured Performance

Tamb = +25°C

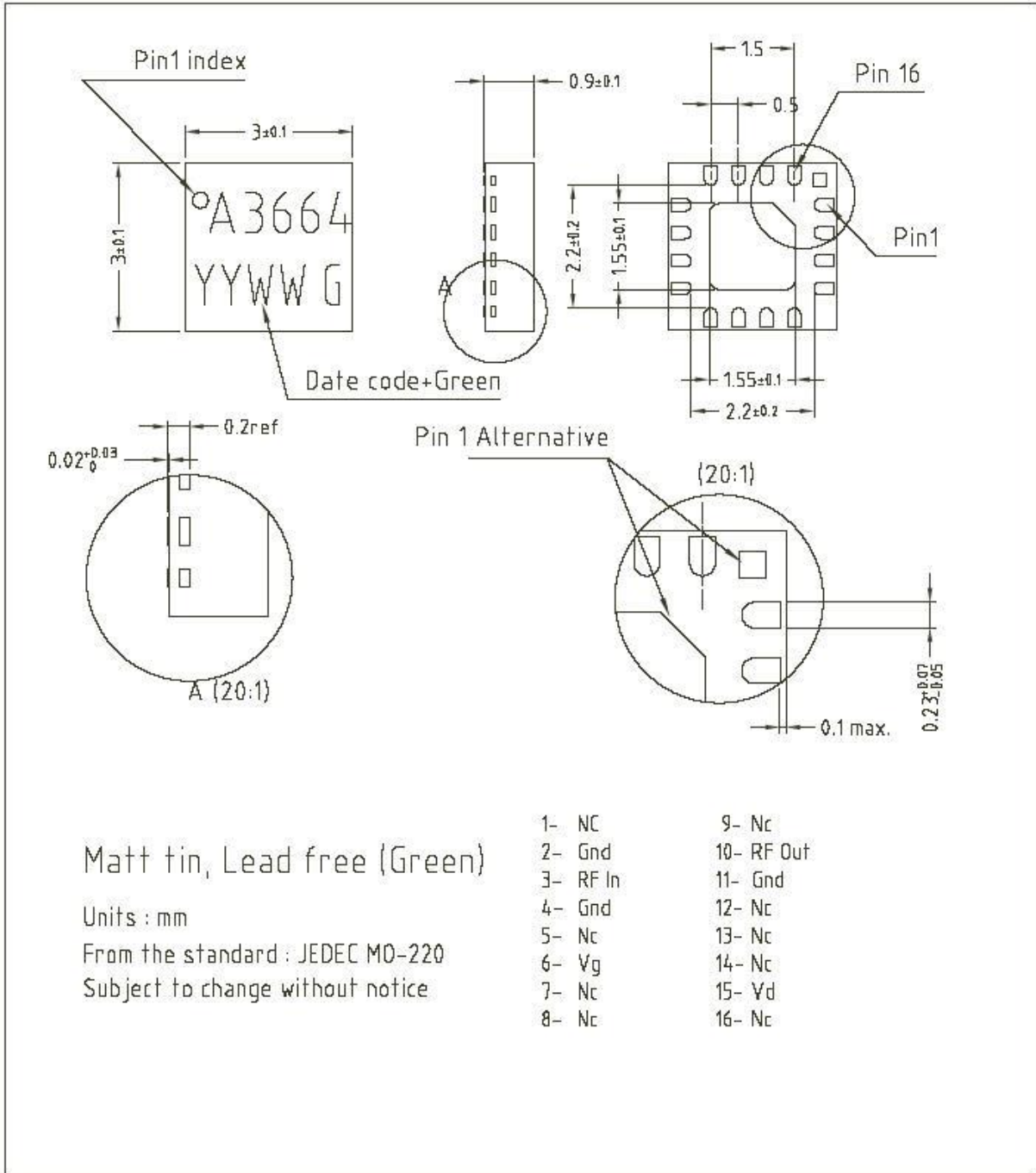
Output power @ 1dB Gain compression



Typical C/I3 versus Pin/tone (Vd=5V)



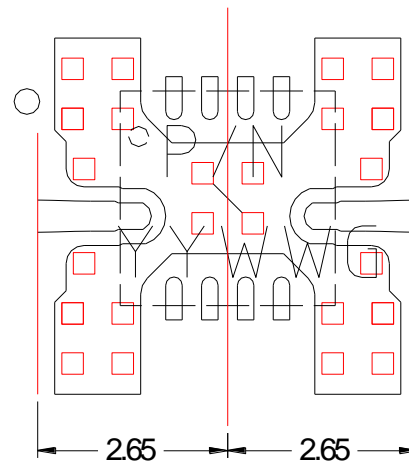
Package outline



Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board shown below under the number 96272.

The reference is the symmetrical axis of the package. The input and output reference planes are located at 2.65mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



SMD mounting procedure

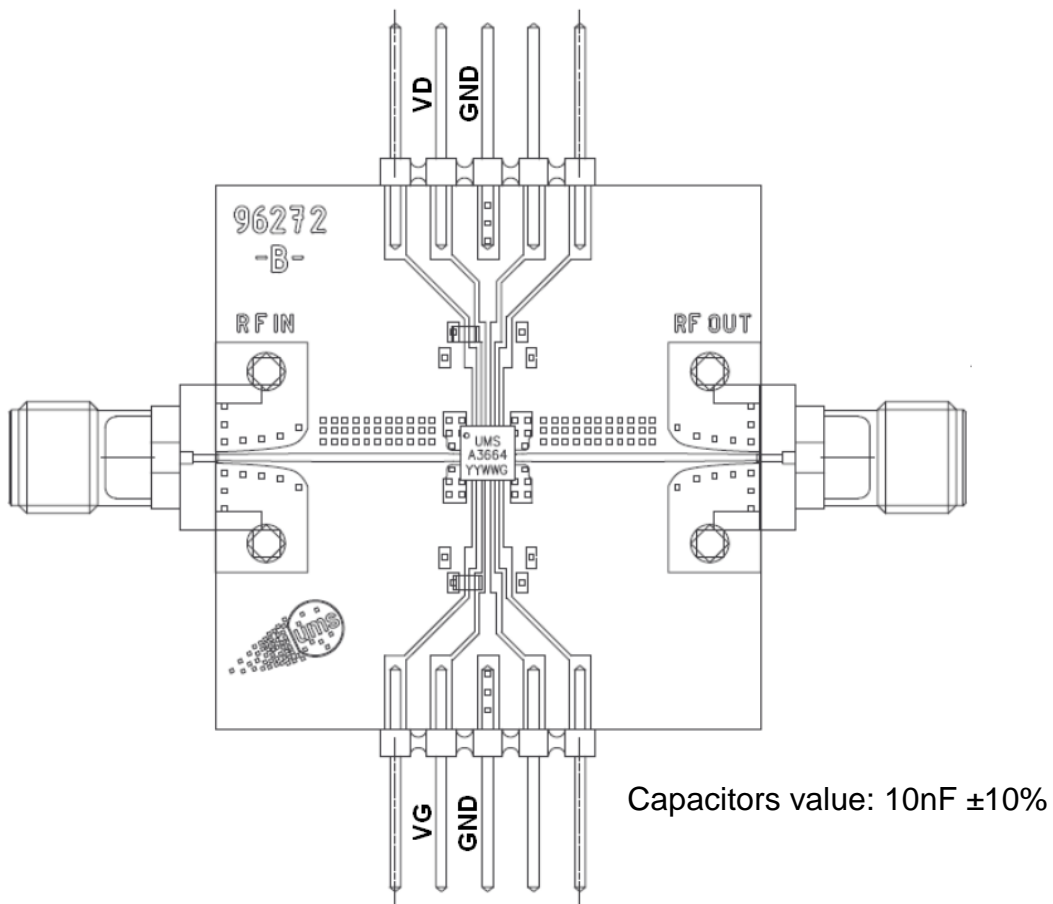
The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the assembly, the standard techniques involving a solder paste and a suitable reflow process can be used. For further details, see application note AN00017.

Notes:

Proposed Assembly board for the 16L-QFN3x3 products characterization

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Ordering Information

QFN 3x3 RoHS compliant package : CHA3664-QAG/XY
 Stick: XY = 20 Tape & reel: XY = 21

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