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S-Band 6-bit Digital Phase Shifter

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHP4012-QEG is a 6-bit phase shifter monolithic circuit, which integrates a CMOS and TTL compatible interface.

It is designed for a wide range of applications, typically defence and space systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.

UMS
P4012
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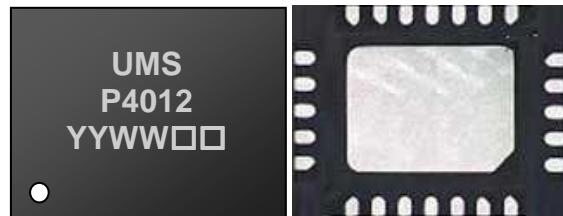
Main Features

■ Frequency range: 2.7-3.5GHz
■ 5.625°phase shifter step
■ 0-360°phase shift range
■ RMS peak phase error: 1°
■ Digital interface
■ 24L-QFN4x5
■ MSL1
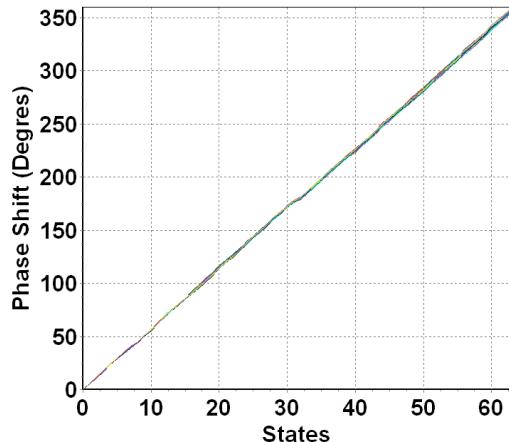
Main Characteristics

Tamb.= +25℃

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2.7		3.5	GHz
Ls	Insertion Loss		5.5		dB
RMS_PPE	RMS Peak Phase Error		1		°

Main Characteristics

Tamb.= +25℃

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2.7		3.5	GHz
PhS	Phase Shift Range	0		360	°
PhS_step	Phase Shift Step		5.625		°
PPE	Peak Phase Error		-2 / +4		°
RMS_PPE	RMS Peak Phase Error		1		°
Ls	Insertion Loss		6.0		dB
Av	Amplitude Variation		+/-0.5		dB
RMS_Av	RMS Amplitude Variation		0.2		dB
S11	Input Reflection Coefficient		-15		dB
S22	Output Reflection Coefficient		-15		dB
P1dB	Input Power at 1dB gain compression		24.5		dBm
Vctrl_L	Control Input Voltage (P1-P6) – low level	0		0.4	V
Vctrl_H	Control Input Voltage (P1-P6) – high level	2.4	3.3	7	V
V+	Positive Supply Voltage		+5		V
V-	Negative Supply Voltage		-5		V
I+	Positive Supply Current		5		mA
I-	Negative Supply Current		5		mA
SwT	Switching Time		15		ns
Top	Operating Temperature	-40		+85	℃

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Peak Phase Error (PPE) definition:

$PPE_{(i)}$ =measured_phase$(S21)_{(i)}$ – measured_phase$(S21)_{(0)}$ – theoretical_phase$_{(i)}$

where (i) is the state (from 0 to 63)

RMS Peak Phase Error (RMS_PPE) definition:

$$RMS\_PPE = \sqrt{\frac{\sum_{i=0}^{63}(PPE(i) - \overline{PPE})^2}{64}}$$

$$\text{with } \overline{PPE} = \frac{\sum_{i=0}^{63}PPE(i)}{64}$$

Insertion Losses Variation (LsV) definition:

$LsV_{(i)}$ =measured_dB$(S21)_{(i)}$ – measured_dB$(S21)_{(0)}$
where $_{(i)}$ is the state (from 0 to 63)

Absolute Maximum Ratings

Tamb.= +25℃ [1]

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply voltage	8	V
V-	Maximum DC negative supply voltage	-8	V
Vctrl	Phase shifter control voltage (Vlow, Vhigh)	-2 to +8	V
Pin	Maximum peak input power overdrive	30	dBm
Tj	Junction temperature	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +155	℃

[1] Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25℃

Symbol	Pin N°	Parameter	Values	Unit
V+	13	Positive Supply Voltage	+5	V
V-	14	Negative Supply Voltage	-5	V
Vctrl	15 to 20	Control Input Voltage	0 / 3.3	V

See "Package outline" paragraph for Pin N° references.

## Phase shifter control table

Voltage to apply on the pads P1 to P6:

| State	Phase (deg)	P6	P5	P4	P3	P2	P1	State	Phase (deg)	P6	P5	P4	P3	P2	P1
0	0	0	0	0	0	0	0	32	180	3.3	0	0	0	0	0
1	5.625	0	0	0	0	0	3.3	33	185.625	3.3	0	0	0	0	3.3
2	11.25	0	0	0	0	3.3	0	34	191.25	3.3	0	0	0	3.3	0
3	16.875	0	0	0	0	3.3	3.3	35	196.875	3.3	0	0	0	3.3	3.3
4	22.5	0	0	0	3.3	0	0	36	202.5	3.3	0	0	3.3	0	0
5	28.125	0	0	0	3.3	0	3.3	37	208.125	3.3	0	0	3.3	0	3.3
6	33.75	0	0	0	3.3	3.3	0	38	213.75	3.3	0	0	3.3	3.3	0
7	39.375	0	0	0	3.3	3.3	3.3	39	219.375	3.3	0	0	3.3	3.3	3.3
8	45	0	0	3.3	0	0	0	40	225	3.3	0	3.3	0	0	0
9	50.625	0	0	3.3	0	0	3.3	41	230.625	3.3	0	3.3	0	0	3.3
10	56.25	0	0	3.3	0	3.3	0	42	236.25	3.3	0	3.3	0	3.3	0
11	61.875	0	0	3.3	0	3.3	3.3	43	241.875	3.3	0	3.3	0	3.3	3.3
12	67.5	0	0	3.3	3.3	0	0	44	247.5	3.3	0	3.3	3.3	0	0
13	73.125	0	0	3.3	3.3	0	3.3	45	253.125	3.3	0	3.3	3.3	0	3.3
14	78.75	0	0	3.3	3.3	3.3	0	46	258.75	3.3	0	3.3	3.3	3.3	0
15	84.375	0	0	3.3	3.3	3.3	3.3	47	264.375	3.3	0	3.3	3.3	3.3	3.3
16	90	0	3.3	0	0	0	0	48	270	3.3	3.3	0	0	0	0
17	95.625	0	3.3	0	0	0	3.3	49	275.625	3.3	3.3	0	0	0	3.3
18	101.25	0	3.3	0	0	3.3	0	50	281.25	3.3	3.3	0	0	3.3	0
19	106.875	0	3.3	0	0	3.3	3.3	51	286.875	3.3	3.3	0	0	3.3	3.3
20	112.5	0	3.3	0	3.3	0	0	52	292.5	3.3	3.3	0	3.3	0	0
21	118.125	0	3.3	0	3.3	0	3.3	53	298.125	3.3	3.3	0	3.3	0	3.3
22	123.75	0	3.3	0	3.3	3.3	0	54	303.75	3.3	3.3	0	3.3	3.3	0
23	129.375	0	3.3	0	3.3	3.3	3.3	55	309.375	3.3	3.3	0	3.3	3.3	3.3
24	135	0	3.3	3.3	0	0	0	56	315	3.3	3.3	3.3	0	0	0
25	140.625	0	3.3	3.3	0	0	3.3	57	320.625	3.3	3.3	3.3	0	0	3.3
26	146.25	0	3.3	3.3	0	3.3	0	58	326.25	3.3	3.3	3.3	0	3.3	0
27	151.875	0	3.3	3.3	0	3.3	3.3	59	331.875	3.3	3.3	3.3	0	3.3	3.3
28	157.5	0	3.3	3.3	3.3	0	0	60	337.5	3.3	3.3	3.3	3.3	0	0
29	163.125	0	3.3	3.3	3.3	0	3.3	61	343.125	3.3	3.3	3.3	3.3	0	3.3
30	168.75	0	3.3	3.3	3.3	3.3	0	62	348.75	3.3	3.3	3.3	3.3	3.3	0
31	174.375	0	3.3	3.3	3.3	3.3	3.3	63	354.375	3.3	3.3	3.3	3.3	3.3	3.3

Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

The following values are representative of onboard measurements (on connector access planes) as defined on the drawing at paragrah "Evaluation mother board".

Insertion Losses versus Frequency @ All States
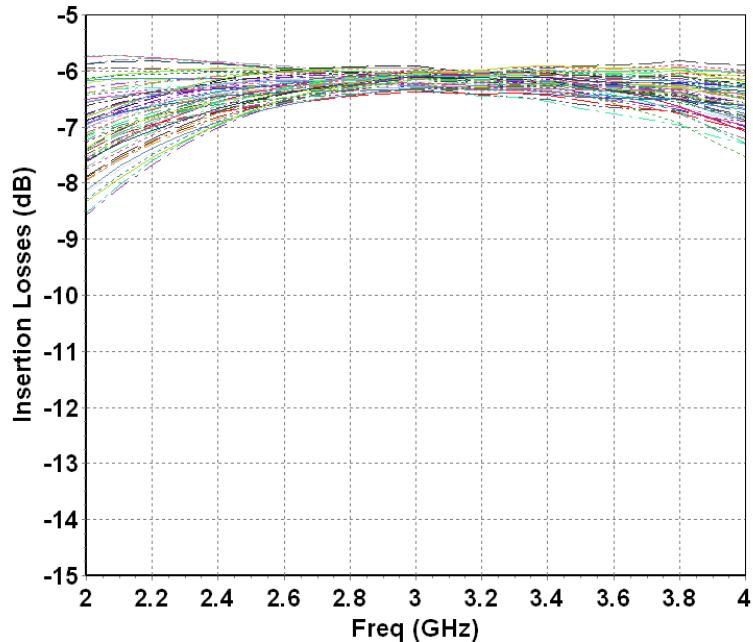

**Input Return Losses @ All States**
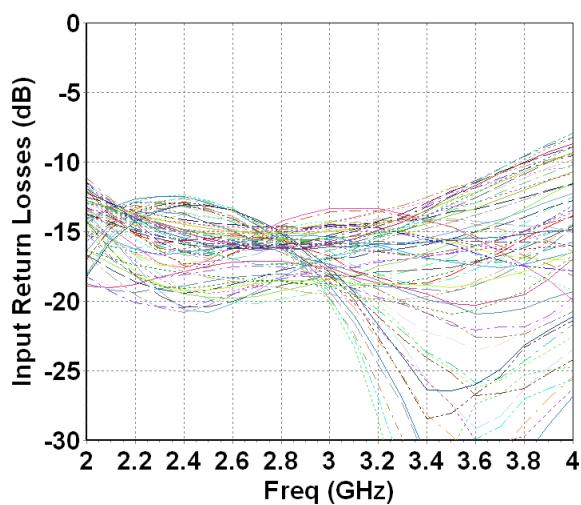
Output Return Losses @ All States
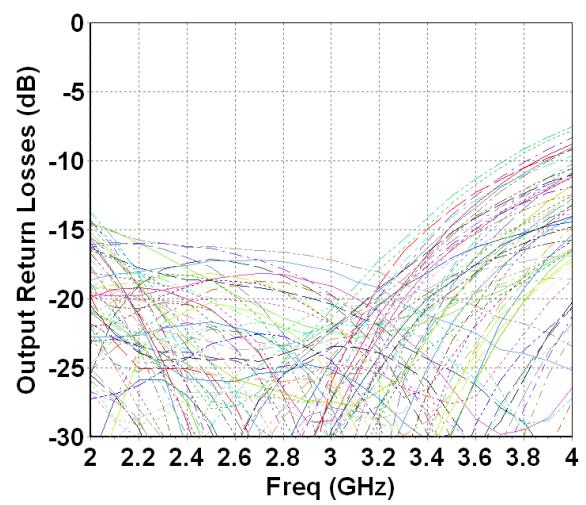
Peak Phase Error versus Frequency (All States)
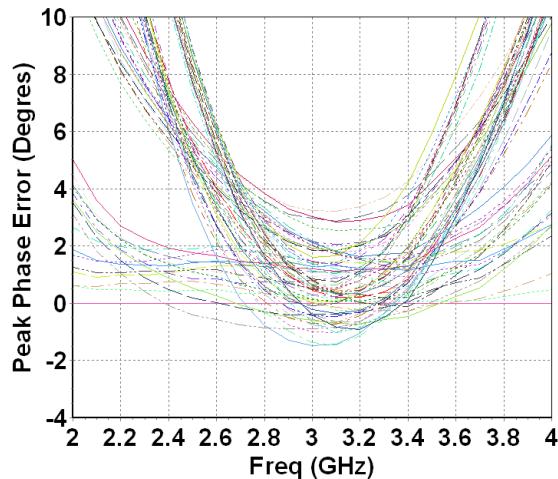

Peak Phase Error versus States (2.7GHz < Frequency < 3.5GHz)
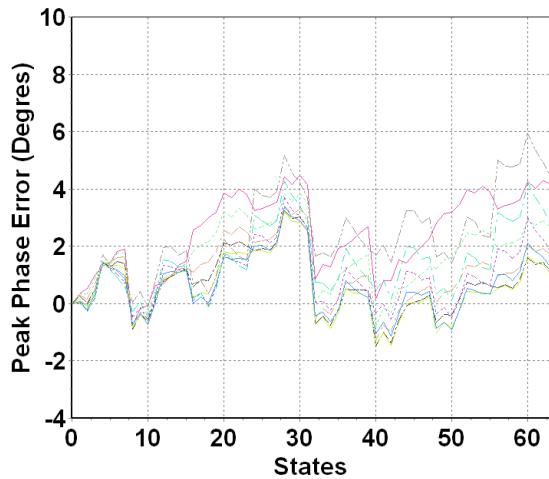
RMS Peak Phase Error versus Frequency
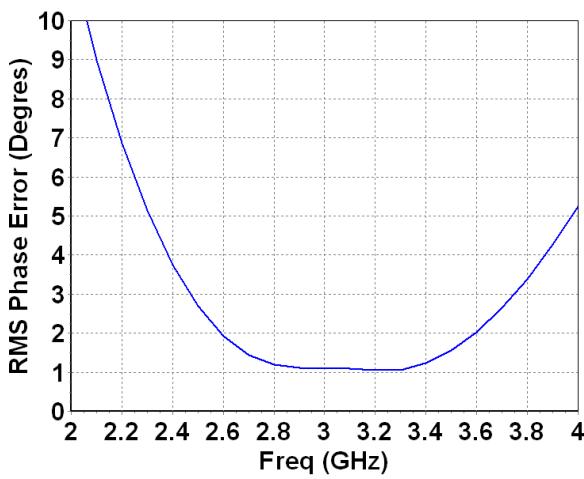
Phase Shift versus States (2.7GHz < Frequency < 3.5GHz)
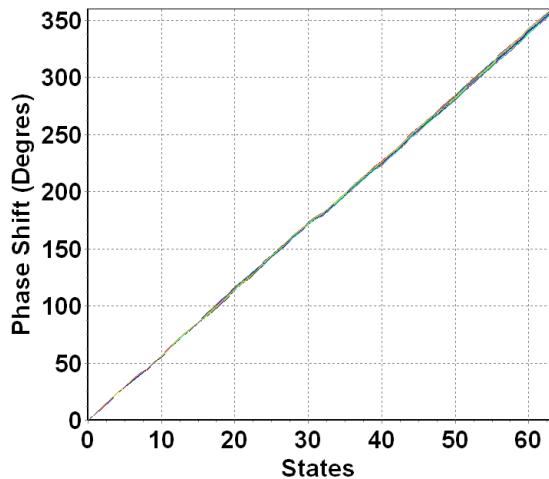
Amplitude Variation versus Frequency (All States)
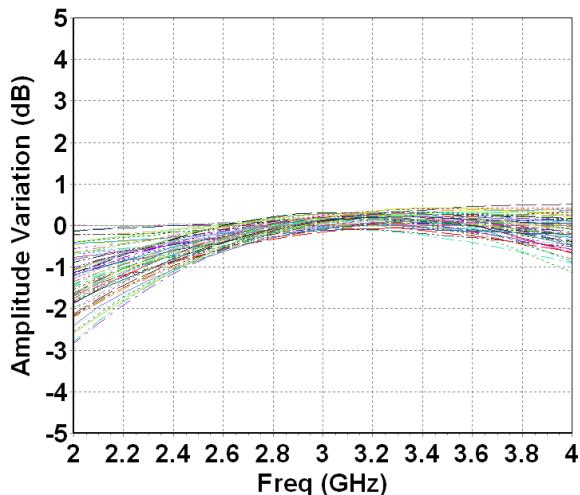
Amplitude Variation versus States (2.7GHz < Frequency < 3.5GHz)
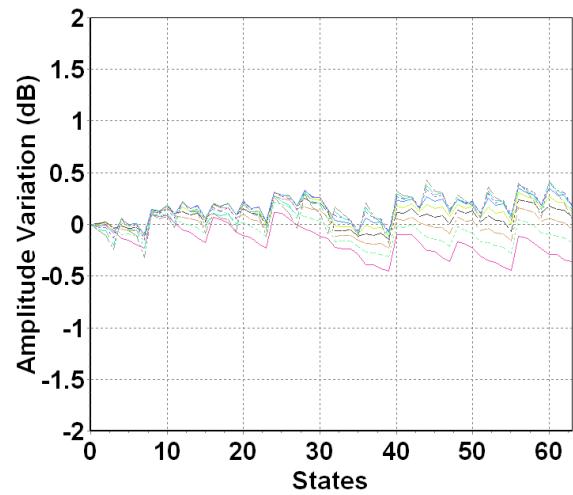
## RMS Amplitude Variation versus Frequency
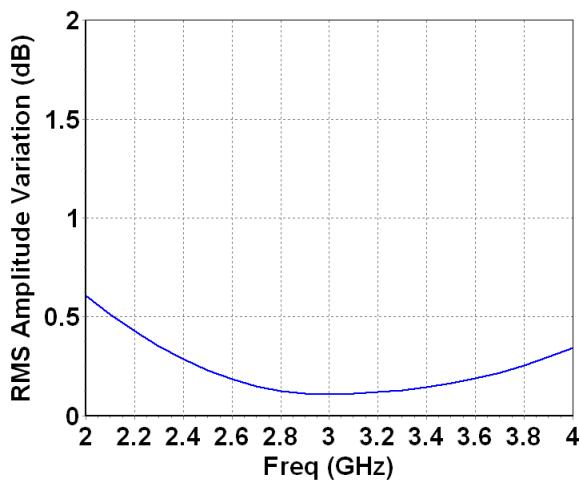
Input Power at 1dB gain compression versus Frequency
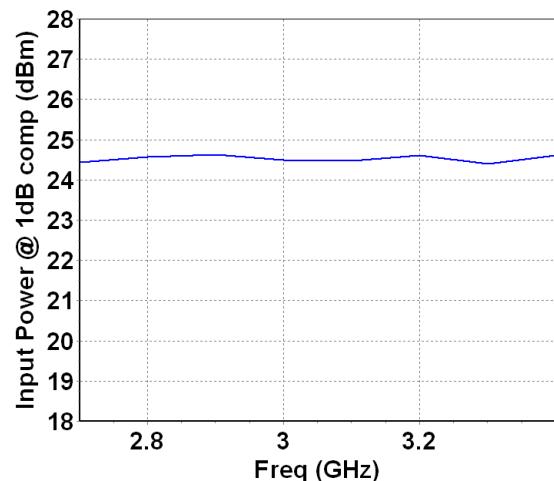
Package outline [1]
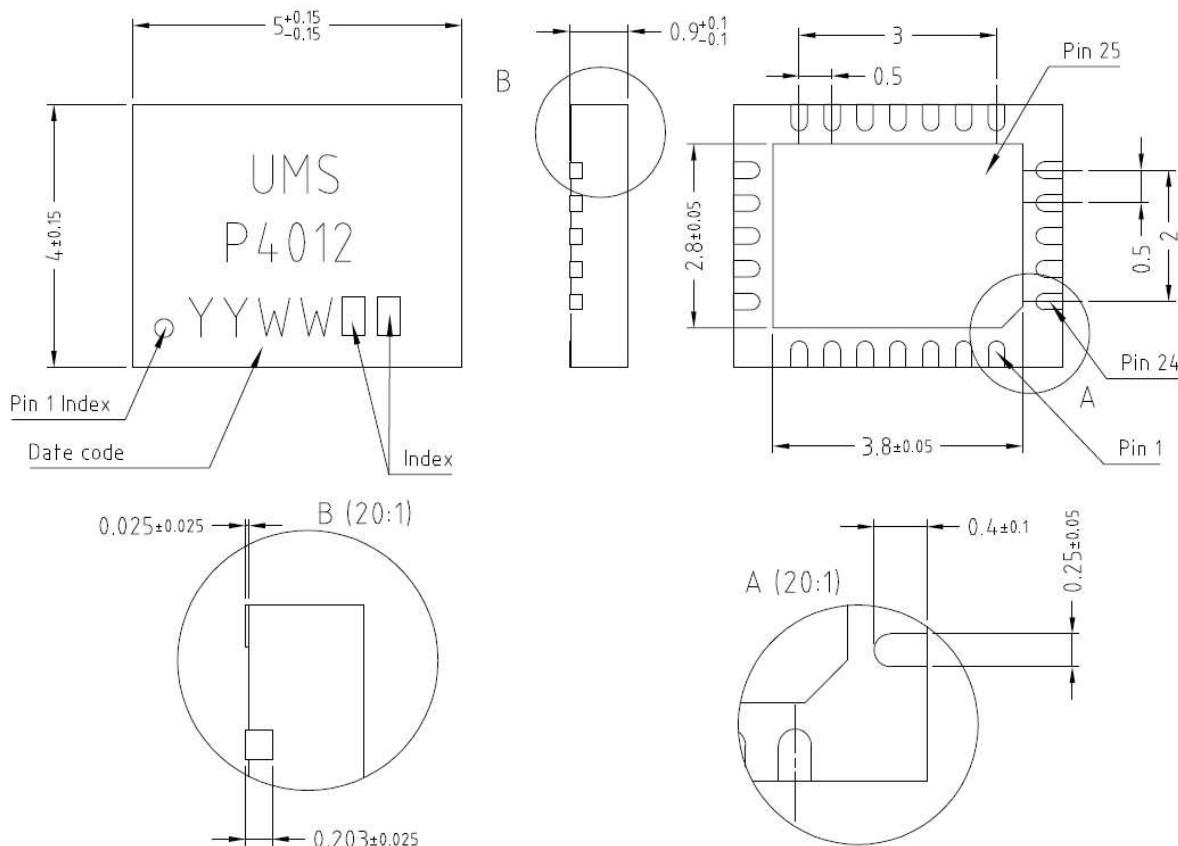
| Matt tin, Lead Free	(Green)	1-	Nc	11-	Gnd[2]	21-	Gnd[2]
Units :	mm	2-	Nc	12-	Nc	22-	RF in
From the standard :	JEDEC MO-220	3-	Nc	13-	V+	23-	Gnd[2]
	(VGHD)	4-	Nc	14-	V-	24-	Nc
25-	GND	5-	Nc	15-	P1		
		6-	Nc	16-	P2		
		7-	Nc	17-	P3		
		8-	Nc	18-	P4		
		9-	Gnd[2]	19-	P5		
		10-	RF out	20-	P6		

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Recommended package footprint
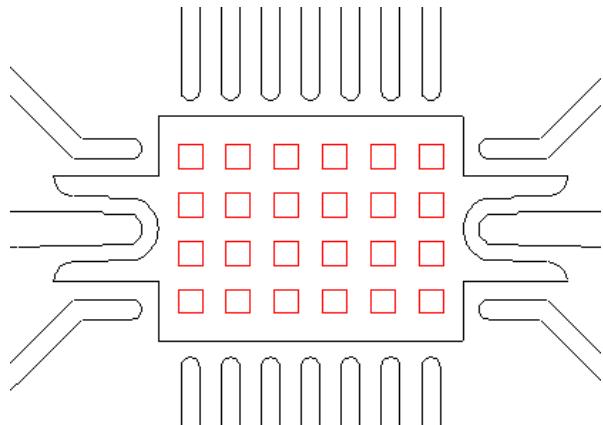
Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.

Notes

Specifications subject to change without notice

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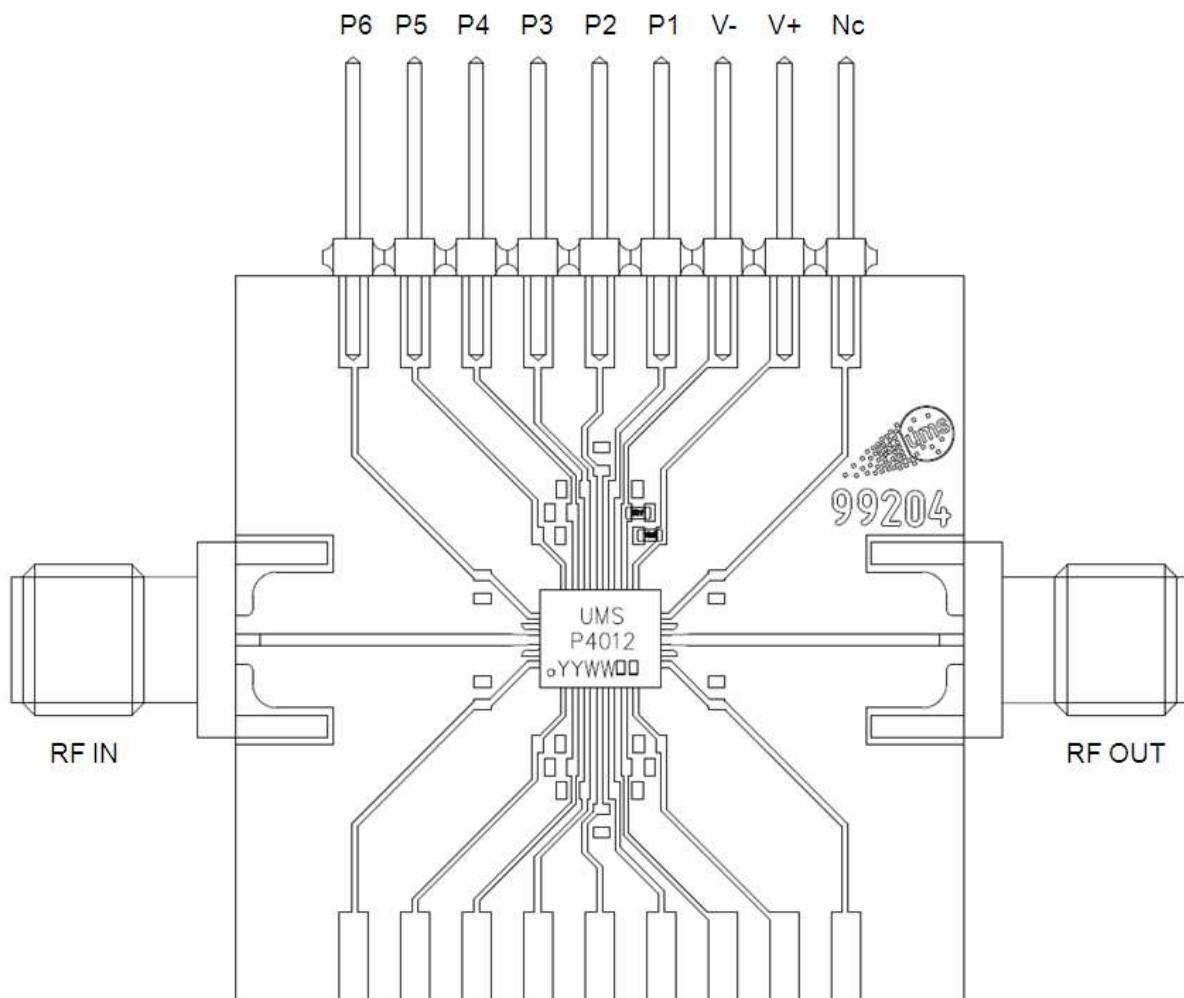
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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package: CHP4012-QEG/XY

         Stick: XY = 20   Tape & reel: XY = 21