

## Features

- 1.8 V to 5.5 V single supply
- $\pm 2.5$  V dual supply
- 3  $\Omega$  on resistance
- 0.75  $\Omega$  on resistance flatness
- 100 pA leakage currents
- 14 ns switching times
- Single 8-to-1 multiplexer CBMG708
- Differential 4-to-1 multiplexer CBMG709
- 16-lead TSSOP package
- Low power consumption
- Qualified for automotive applications
- TTL-/CMOS-compatible inputs

## Application

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching
- Battery-powered systems

## Description

The CBMG708/CBMG709 are low voltage, CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The CBMG708 switches one of eight inputs (S1 to S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The CBG709 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

Low power consumption and an operating supply range of 1.8 V to 5.5 V make the CBMG708/CBMG709 ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

These switches are designed on an enhanced sub micron process that provides low power dissipation yet gives high switching speed, very low on resistance, and leakage currents.

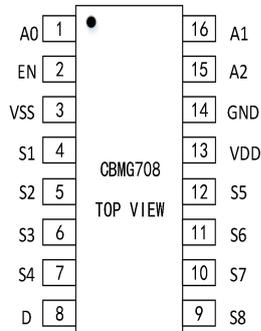
On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies.

The CBMG708/CBMG709 are available in a 16-lead TSSOP.

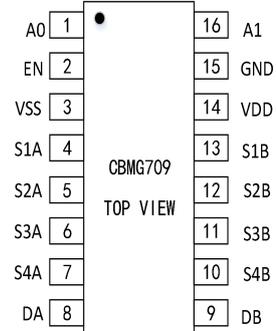
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## Pin Configurations



CBMG708 Pin Configuration



CBMG709 Pin Configuration

### CBMG708 Pin Description

Pin NO.	Pin Name	Description
1	A0	Digital Input. Channel selection control line A0
2	EN	Digital Input. Switch enable control line
3	V <sub>SS</sub>	Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, it should be tied to GND.
4	S1	Source Terminal. Can be an input or output.
5	S2	Source Terminal. Can be an input or output.
6	S3	Source Terminal. Can be an input or output.
7	S4	Source Terminal. Can be an input or output.
8	D	Drain Terminal. Can be an input or output.
9	S8	Source Terminal. Can be an input or output.
10	S7	Source Terminal. Can be an input or output.
11	S6	Source Terminal. Can be an input or output.
12	S5	Source Terminal. Can be an input or output.
13	V <sub>DD</sub>	Positive Power Supply Pin.
14	GND	Ground Reference.
15	A2	Digital Input. Channel selection control line A1
16	A1	Digital Input. Channel selection control line A2

**CBMG709 Pin Description**

Pin NO.	Pin Name	Description
1	A0	Digital Input. Channel selection control line A0
2	EN	Digital Input. Switch enable control line
3	V <sub>SS</sub>	Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, it should be tied to GND.
4	S1A	Source Terminal. Can be an input or output.
5	S2A	Source Terminal. Can be an input or output.
6	S3A	Source Terminal. Can be an input or output.
7	S4A	Source Terminal. Can be an input or output.
8	DA	Drain Terminal. Can be an input or output.
9	DB	Drain Terminal. Can be an input or output.
10	S4B	Source Terminal. Can be an input or output.
11	S3B	Source Terminal. Can be an input or output.
12	S2B	Source Terminal. Can be an input or output.
13	S1B	Source Terminal. Can be an input or output.
14	V <sub>DD</sub>	Positive Power Supply Pin.
15	GND	Ground Reference.
16	A1	Digital Input. Channel selection control line A1

**CBMG708 Truth Table**

A2	A1	A0	EN	Switch Condition
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X=Don not care

**CBMG709 Truth Table**

A1	A0	EN	Switch Condition
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X=Don not care

## Absolute Maximum Ratings <sup>(1)</sup>

- $V_{DD}$  to  $V_{SS}$  : 7V
- $V_{DD}$  to GND : -0.3V to +7V
- $V_{SS}$  to GND : +0.3V to -3.5V
- Analog Inputs<sup>1</sup> :  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$  or 30 mA, whichever occurs first
- Digital Inputs<sup>1</sup> : -0.3V to  $V_{DD}+0.3V$  or 30 mA, whichever occurs first
- Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) : 100 mA
- Continuous Current, S or D : 30 mA
- Industrial Temperature Range : -40°C to +125°C
- Storage Temperature Range : -65°C to +150°C
- Junction Temperature : 150°C
- TSSOP Package, Power Dissipation : 432mW
- $\theta_{JA}$  Thermal Impedance : 150.4°C/W
- $\theta_{JC}$  Thermal Impedance : 27.6°C/W
- Lead Temperature (Soldering, 60s) : 215°C ,Infrared (15 sec) 220°C

## Electrical Characteristics

( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $+25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	CONDITION	CBMG708,CBMG709			
		MIN	TYP	MAX	UNIT
<b>Analog Switch</b>					
Analog Signal Range		0		$V_{DD}$	V
On Resistance ( $R_{on}$ )	$S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ;		3	4.5	$\Omega$
On Resistance Match Between Channels ( $\Delta R_{on}$ )	$S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ;		0.4		$\Omega$
On Resistance Flatness( $R_{FLAT(ON)}$ )			0.75		$\Omega$
<b>Leakage Currents</b>					
Source Off Leakage, $I_S$ (Off)	$V_{DD}=5.5\text{V}$ , $V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$		$\pm 0.01$	$\pm 0.1$	nA
Drain Off Leakage, $I_D$ (Off)	$V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$		$\pm 0.01$	$\pm 0.1$	nA
Channel On Leakage, $I_D$ , $I_S$ (On)	$V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$		$\pm 0.01$	$\pm 0.1$	nA
<b>Digital Inputs</b>					
Input High Voltage, $V_{INH}$		2.4			V
Input Low Voltage, $V_{INL}$				0.8	V
Input Current $I_{INL}$ or $I_{INH}$			0.05		$\mu\text{A}$
Digital Input Capacitance, $C_{IN}$			2		pF
<b>Dynamic Characteristics</b>					
$t_{TRANSITION}$	$R_L=300\Omega$ , $C_L=35\text{pF}$ , $V_{S1}=3\text{V/0V}$ , $V_{S8}=0\text{V/3V}$		14		ns
Break-Before-Make Time Delay, $t_{OPEN}$	$R_L=300\Omega$ , $C_L=35\text{pF}$		8		ns
$t_{ON(EN)}$	$R_L=300\Omega$ , $C_L=35\text{pF}$ , $V_S=3\text{V}$		14		ns
$t_{OFF(EN)}$	$R_L=300\Omega$ , $C_L=35\text{pF}$ , $V_S=3\text{V}$		7		ns
Charge Injection	$V_S=2.5\text{V}$ , $R_S=0\Omega$ , $C_L=1\text{nF}$		$\pm 3$		pC
Off Isolation	$R_L=50\Omega$ , $C_L=5\text{pF}$ , $f=10\text{MHz}$		-60		dB
<b>Power Requirements</b>					
$I_{DD}$	$V_{DD}=5.5\text{V}$ , Digital inputs=0V or 5.5V		0.001	1.0	$\mu\text{A}$

( $V_{DD} = 3\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $+25^{\circ}\text{C}$ , unless otherwise noted.)

PARAMETER	CONDITION	CBMG708,CBMG709			
		MIN	TYP	MAX	UNIT
<b>Analog Switch</b>					
Analog Signal Range		0		$V_{DD}$	V
On Resistance ( $R_{on}$ )	$S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ;		8	14	$\Omega$
On Resistance Match Between Channels ( $\Delta R_{on}$ )	$S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ;		0.4		$\Omega$
On Resistance Flatness( $R_{FLAT(ON)}$ )			0.75		$\Omega$
<b>Leakage Currents</b>					
Source Off Leakage, $I_S$ (Off)	$V_{DD}=3.3\text{V}, V_D = 1\text{V}/3\text{ V}, V_S = 3\text{ V}/1\text{ V}$		$\pm 0.01$	$\pm 0.1$	nA
Drain Off Leakage, $I_D$ (Off)	$V_D = 1\text{ V}/3\text{ V}, V_S = 3\text{ V}/1\text{ V}$		$\pm 0.01$	$\pm 0.1$	nA
Channel On Leakage, $I_D, I_S$ (On)	$V_D = V_S = 1\text{ V or }3\text{ V}$		$\pm 0.01$	$\pm 0.1$	nA
<b>Digital Inputs</b>					
Input High Voltage, $V_{INH}$		2.0			V
Input Low Voltage, $V_{INL}$				0.8	V
Input Current $I_{INL}$ or $I_{INH}$			0.05		$\mu\text{A}$
Digital Input Capacitance, $C_{IN}$			2		pF
<b>Dynamic Characteristics</b>					
$t_{TRANSITION}$	$R_L=300\Omega, C_L=35\text{pF}, V_{S1}=2\text{V}/0\text{V}, V_{S8}=0\text{V}/2\text{V}$		18		ns
Break-Before-Make Time Delay, $t_{OPEN}$	$R_L=300\Omega, C_L=35\text{pF}$		8		ns
$t_{ON}$ (EN)	$R_L=300\Omega, C_L=35\text{pF}, V_S=2\text{V}$		18		ns
$t_{OFF}$ (EN)	$R_L=300\Omega, C_L=35\text{pF}, V_S=2\text{V}$		8		ns
Charge Injection	$V_S=1.5\text{V}, R_S=0\Omega, C_L=1\text{nF}$		$\pm 3$		pC
Off Isolation	$R_L=50\Omega, C_L=5\text{pF}, f=10\text{MHz}$		-60		dB
<b>Power Requirements</b>					
$I_{DD}$	$V_{DD}=3.3\text{V}$ , Digital inputs=0V or 3.3V		0.001	1.0	$\mu\text{A}$

## Typical Characteristics

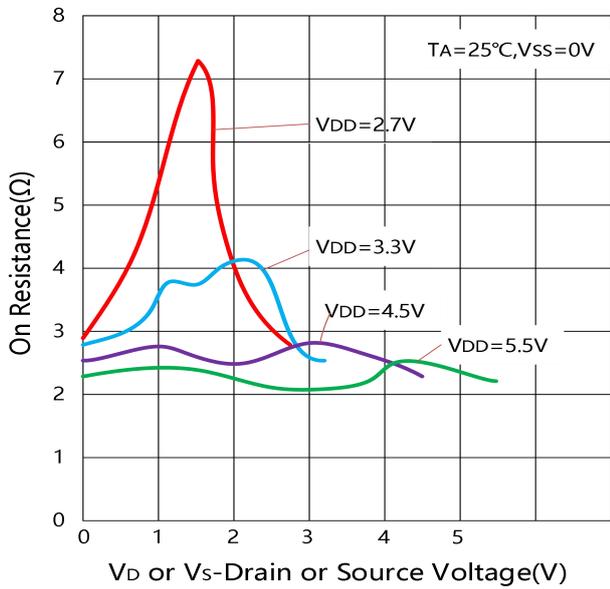


Figure 1. On Resistance as a Function of VD  
Different Temperatures,

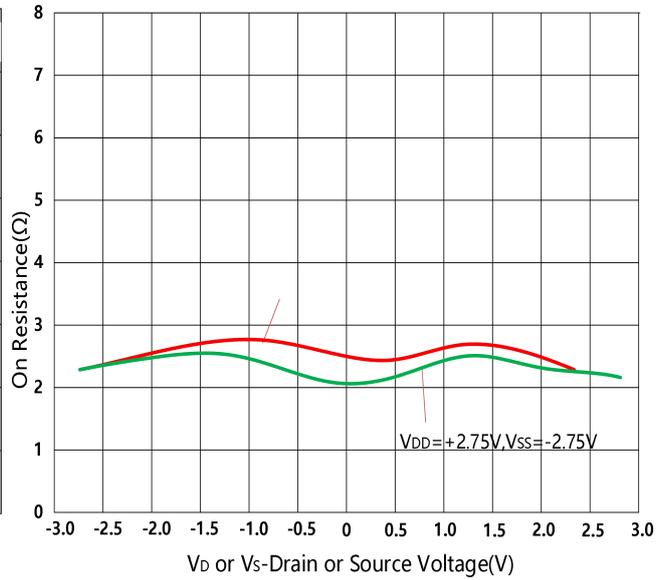


Figure 2. On Resistance as a Function of VD  
(VS) for Dual Supply

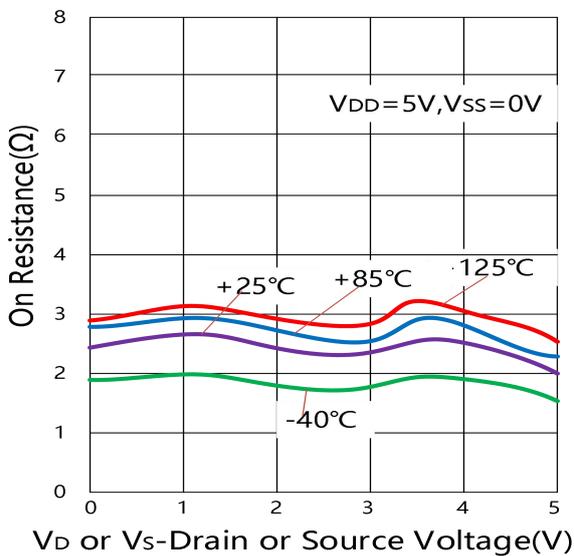


Figure 3. On Resistance as a Function of VD  
(VS) for Single Supply

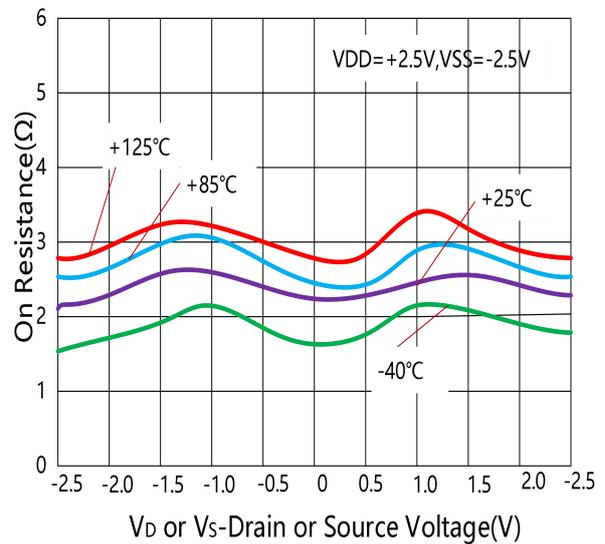
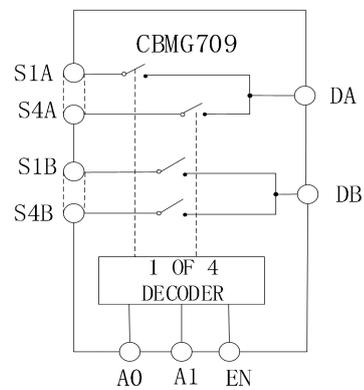
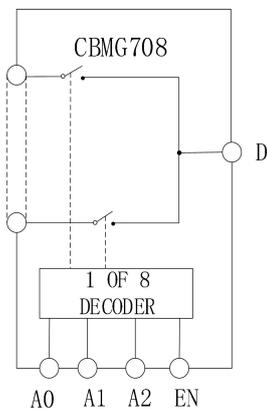


Figure 4. On Resistance as a Function of VD (VS)  
for Different Temperatures, Dual Supply

## Application Notes

When using CMOS devices, take care to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the device being subjected to stresses beyond the maximum ratings

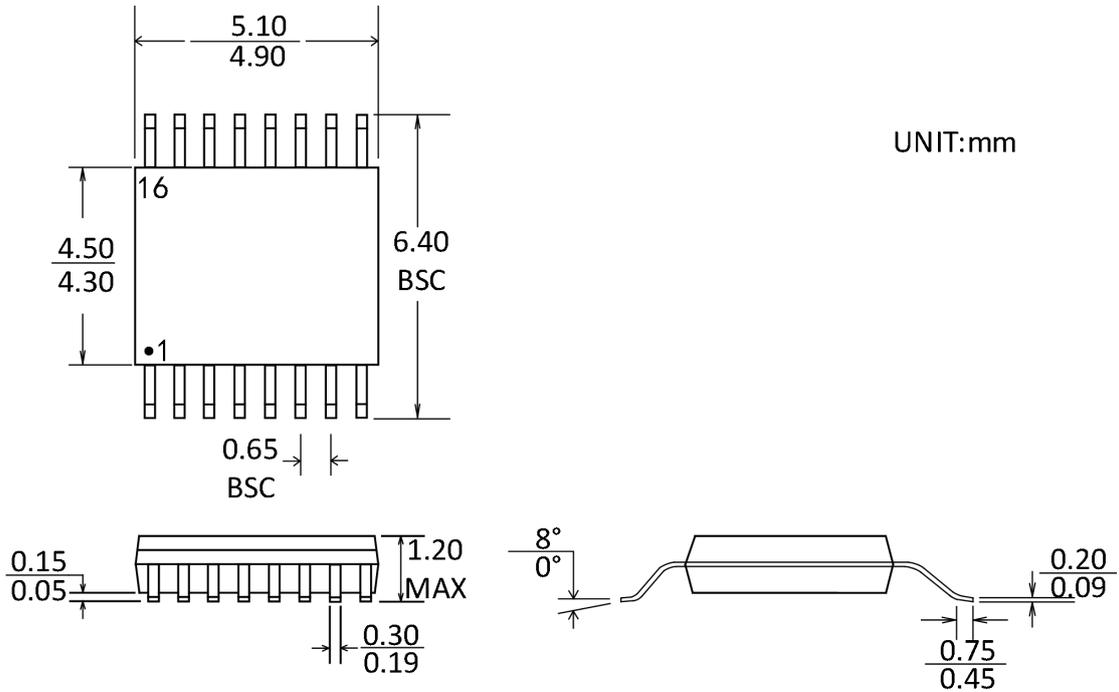
Always apply digital and analog inputs after power supplies and ground. For single-supply operation, tie VSS to GND as close to the device as possible.



**Functional Block Diagrams**

## Package Outline Dimensions

### TSSOP-16



## Package/Ordering Information

PRODUCT TYPE	OPERATING TEMPERATURE	PACKAGE	PACKAGE MARKING	NUMBER OF PACKAGES
CBMG708ATS16	-40°C~125°C	TSSOP-16	CBMG708AT	Tape and Reel, 2500
CBMG708ATS16-RL	-40°C~125°C	TSSOP-16	CBMG708AT	Tape and Reel, 3000
CBMG708ATS16-REEL	-40°C~125°C	TSSOP-16	CBMG708AT	Tape and Reel, 4000
CBMG709ATS16	-40°C~125°C	TSSOP-16	CBMG709AT	Tape and Reel, 2500
CBMG709ATS16-RL	-40°C~125°C	TSSOP-16	CBMG709AT	Tape and Reel, 3000
CBMG709ATS16-REEL	-40°C~125°C	TSSOP-16	CBMG709AT	Tape and Reel, 4000