

FEATURES

- ∩ 20/23 dBm P1dB/PSAT
- ∩ V-band coverage
- ∩ 31 dBm OIP3
- ∩ 18 dB gain

TYPICAL APPLICATIONS

- ∩ Point-to-point communication
- ∩ Instrumentation
- ∩ Fiber over radio
- ∩ WiGig

DESCRIPTION

gAPZ0038 is a medium Power Amplifier (PA) in the 60 GHz ISM frequency band suitable for WiGig V-band point-to-point communication. The PA's output stage has two parallel HEMTs to increase output power. The PA has high gain, high linearity, low input/output return loss and flat gain response.

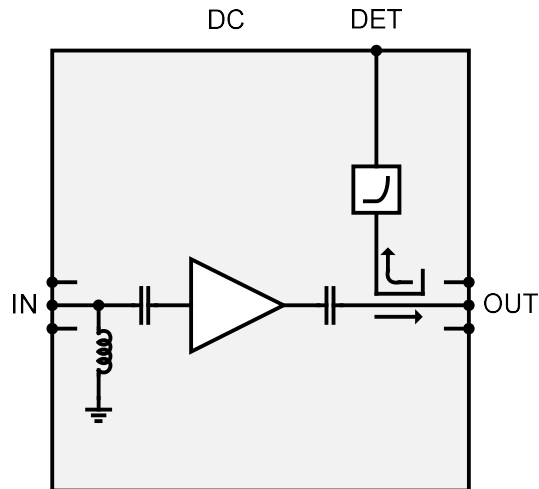


Figure 1. Block diagram of the medium PA.

ELECTRICAL PERFORMANCE

Table 1. Electrical performance $T_A=25^{\circ}\text{C}$

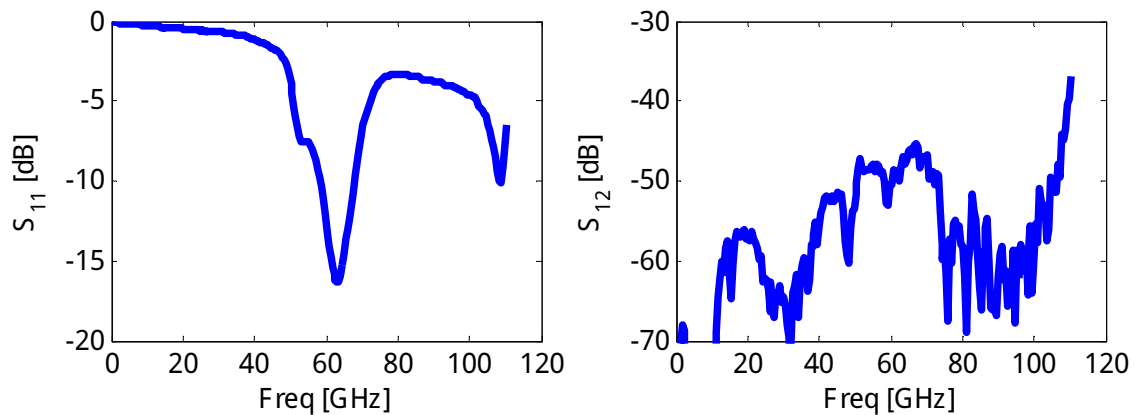
Parameter	Min	Typ	Max	Unit
Frequency	57 (55)		66 (71)	GHz
Gain	16	18	20	dB
P1dB	19	20	21	dBm
PSAT	21	23	24	dBm
OIP3	28	31	32	dBm
PAE			20	%
Input return loss	8 (7)			dB
Output return loss	10			dB
Power consumption		775		mW

MEASURED PERFORMANCE

The chip has been measured on-wafer using CW and 2-tone input test signals. The PA uses typical bias settings if not specified differently.

Table 2. Test conditions

Parameter	Setting
RF input power	-10 dBm/tone
RF input frequency	61 GHz
Frequency separation	10 MHz
Temperature	25°C



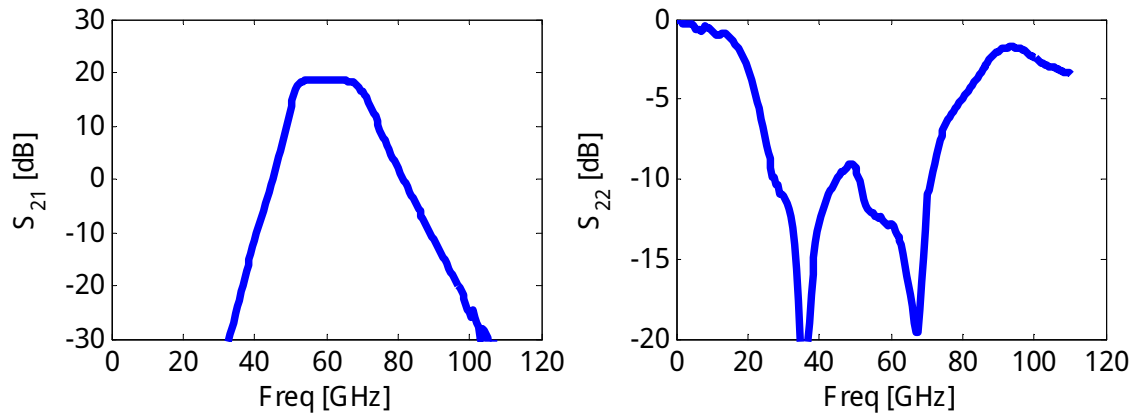


Figure 2. Small signal response from 0-120 GHz at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.

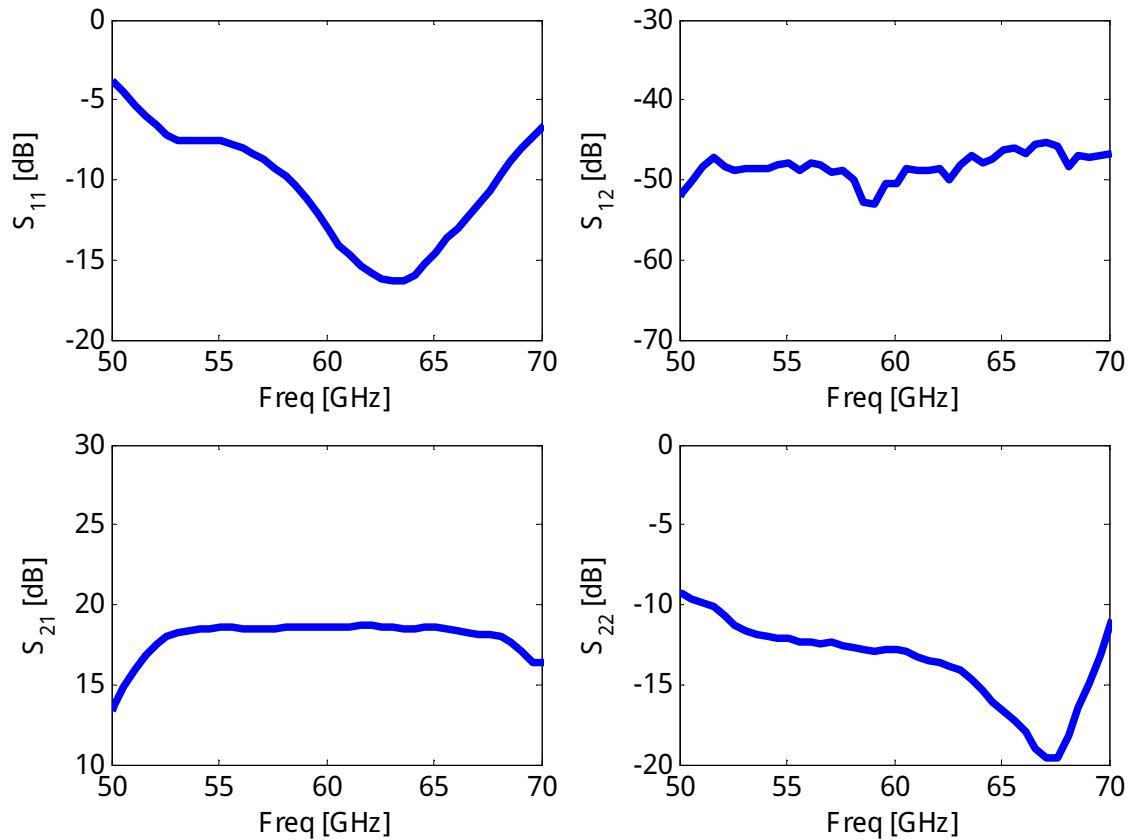


Figure 3. Small signal response within the 60 GHz ISM-band at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.

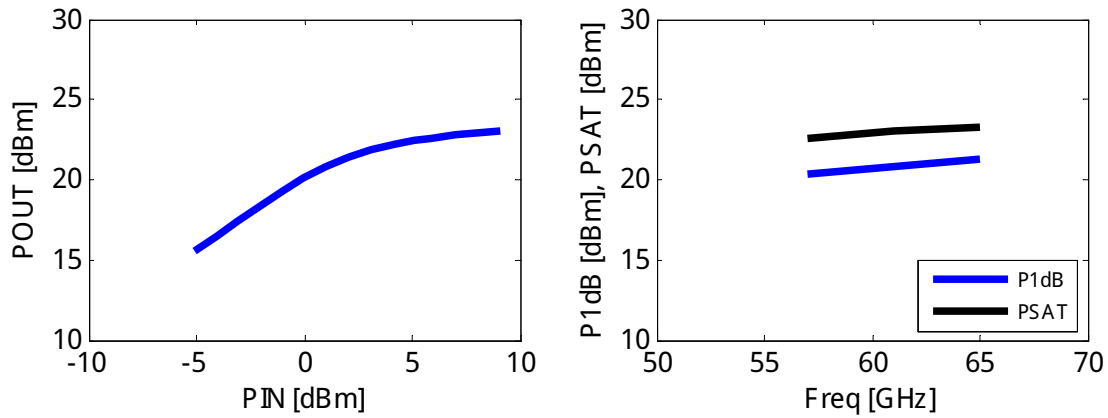


Figure 4. (Left): Output power vs input power at 61 GHz. (Right): P1dB and PSAT vs freq.

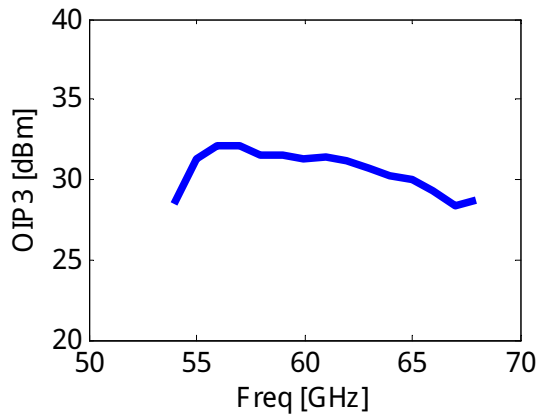


Figure 5. : OIP3 vs frequency.

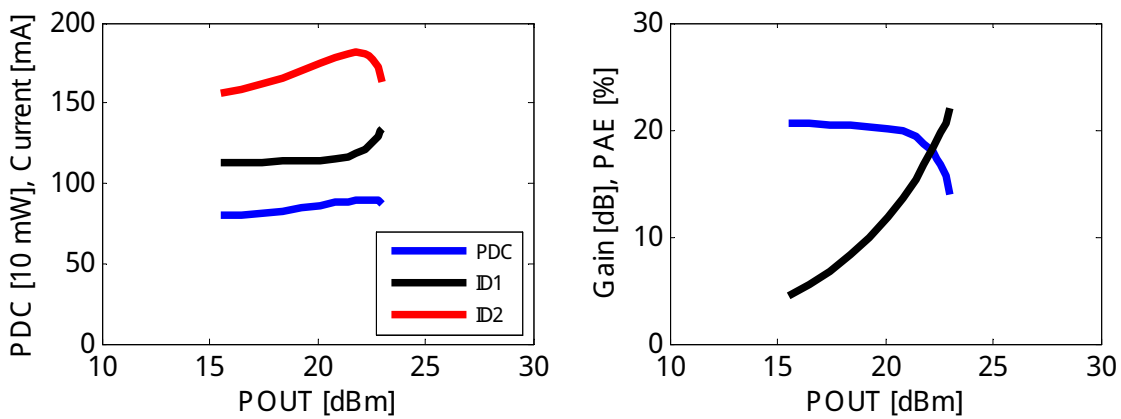


Figure 6. (Left): Power dissipation and drain currents ID1 and ID2 vs output power at 61 GHz. (Right): Efficiency and gain vs output power measured at 61 GHz.

RECOMMENDED OPERATING CONDITION

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 3-5 to obtain the specified drain currents. The drain currents are stated with no input signal.

Table 3. Electrical settings on connector P1

Connector P1	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
VOUT_DET	1	0		2.0	Output
VREF_DET	2	0	0.2		Output
VG_DET	3	-1.0	-0.8 ^[1]	-0.6	Input
VD2	4	3.2	3.3 / 150	3.4	Input
GND	5				Ground
VG2	6	-0.7	-0.5	-0.3	Input
VG1	7	-0.7	-0.5	-0.3	Input
VD1	8	2.4	2.5 / 112	2.6	Input
NC	9				NC

Table 4. Electrical settings on connector P2

Connector P2	Pad No.	Interface	I/O
GND	1		Ground
RF_OUT	2	Z ₀ = 50 Ohm, AC coupled	Output
GND	3		Ground

Table 5. Electrical settings on connector P3

Connector P3	Pad No.	Interface	I/O
GND	1		Ground
RF_IN	2	Z ₀ = 50 Ohm, AC coupled	Input
GND	3		Ground

^[1] Maximum sensitivity is achieved at threshold voltage.

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute maximum ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
ID2	360 mA
ID1	240 mA
RF input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. The substrate thickness is 50 μm (GaAs).

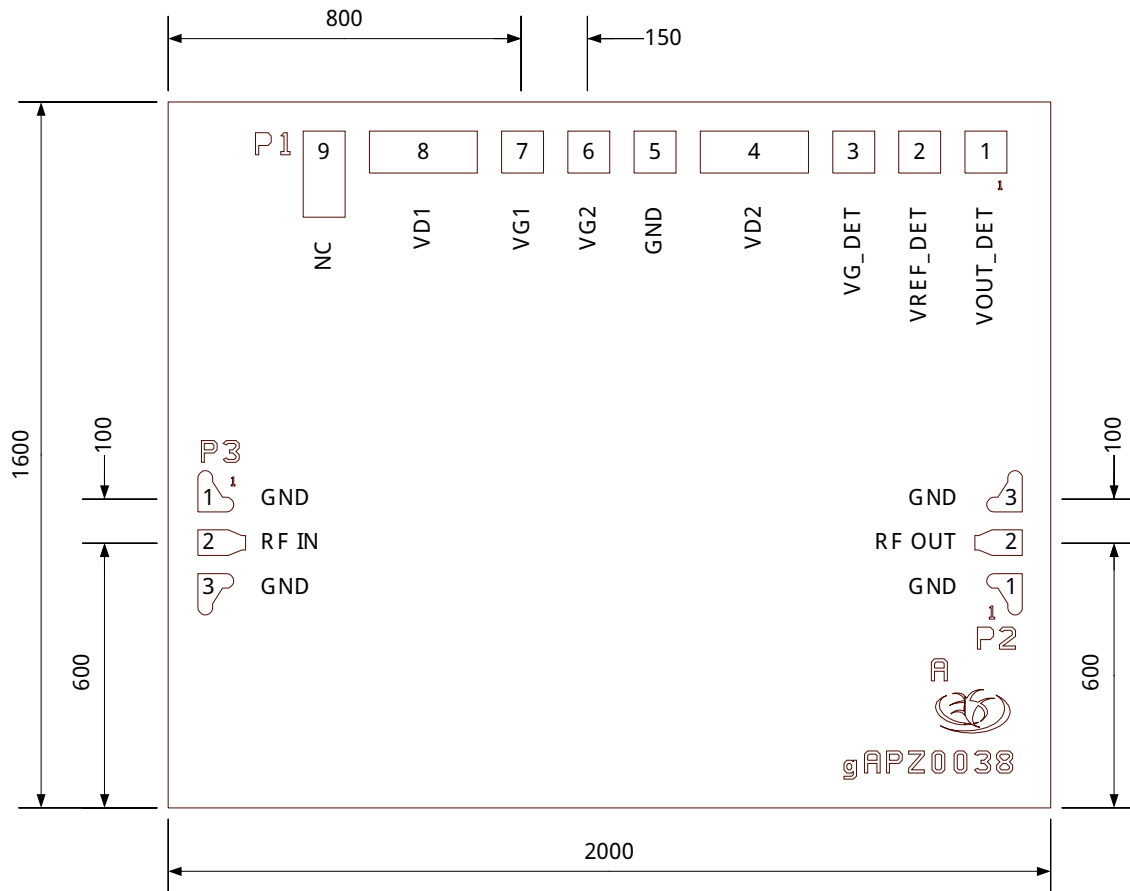


Figure 7. Outline drawing of the MMIC. Dimensions are in μm .