Preliminary Datasheet

CGY2170UH
7-bit X-Band Core Chip

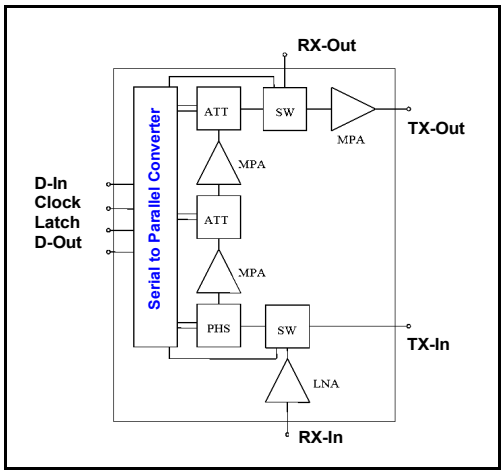
Rev 2.0

DESCRIPTION

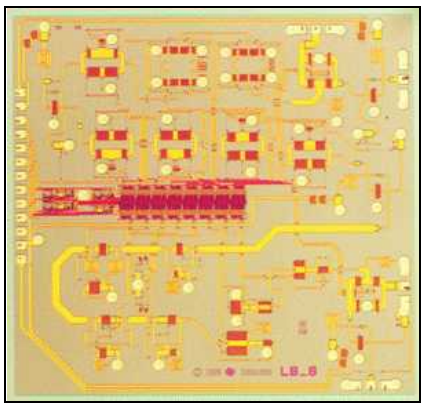
The CGY2170UH is a high performance GaAs MMIC 7–bit Core Chip operating in X-band. It includes a phase shifter, an attenuator, T/R switches, and amplification. The on chip Series to Parallel Conversion of the phase shifter, attenuator and switch control greatly simplifies the interfacing to this device.

The CGY2170UH has a nominal phase shifting range of 0 – 360° and a gain setting range of 24 dB. It covers the frequency range of 8 to 12 GHz and can be used in Radar, Telecommunication and Instrumentation applications.

This die is manufactured using OMMIC's 0.18 µm gate length PHEMT Technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.



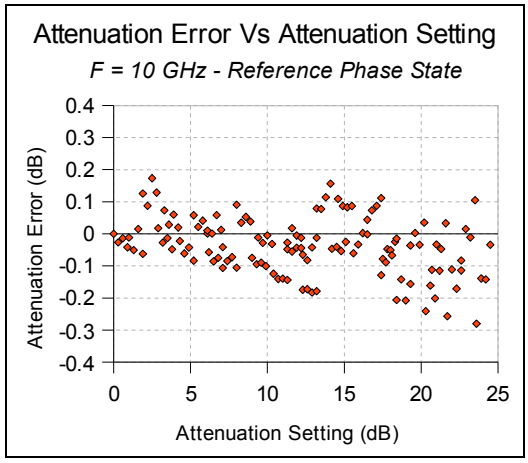
Block Diagram of the 7 bit X-band Core Chip

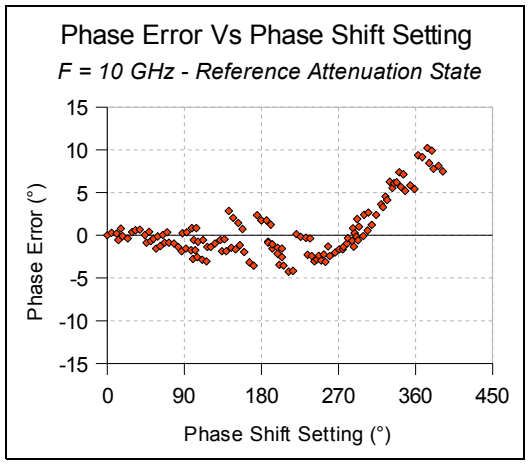


This MMIC has been developed in cooperation with TNO

FEATURES

- Operating Range : 8 GHz to 12 GHz
- Typical Gain : 8 dB at 10 GHz
- Low RMS Phase Error ≈ 5.0° @ 10 GHz
- Low RMS Amplitude Error ≈ 0.25 dB @ 10GHz
- Noise Figure : 7 dB at 10 GHz
- P1dB (out) > +12 dBm at maximum gain
- S_{11} < -14 dB at 10 GHz (all states)
- S_{22} < -18 dB at 10 GHz (all states)
- Convenient CMOS
- Total Power Consumption < 0.8 W
- Chip size = 4365 x 4165 µm ± 5 µm
- Tested, Inspected Known Good Die (KGD)
- Demonstration Boards Available
- Samples Available





APPLICATIONS

- Radar, Telecommunication & Instrumentation

LIMITING VALUES

T_{amb} = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{d1}, V_{d2a}, V_{d2b}, V_{d3}	Amplifier Drain Supplies		0	+6	V
V_{dd1}	Digital positive power-supply		0	+6	V
V_{dd2}	Digital positive power-supply 2		0	+3	V
V_{ss}	Digital negative power supply		-6	0	V
V_g	Gate Bias voltage of MPAs and LNA		-5	-2	V
P_{in}	Input power at RF Ports			+25	dBm
T_{amb}	Ambient temperature		-40	+85	° C
T_j	Junction temperature			+150	° C
T_{stg}	Storage temperature		-55	+150	° C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient (T_a = 25 °C)	35	° C/W

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CHARACTERISTICS

T_{amb} = 25 °C – RF Performance at 10 GHz unless specified

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Power Supplies						
V_{d1}	Rx mode LNA supply voltage			5		V
I_{d1}	Rx mode LNA supply current	V_g = -3 V		45		mA
V_{d2a}	MPA1 drain supply voltage			5		V
I_{d2a}	MPA1 supply current	V_g = -3 V		45		mA
V_{d2b}	MPA2 drain supply voltage			5		V
I_{d2b}	MPA2 supply current	V_g = -3 V		45		mA
V_{d3}	Tx mode MPA drain supply voltage			5		V
I_{d3}	Tx mode MPA supply current	V_g = -3 V		45		mA
V_{dd1}	Digital circuit drain supply voltage			5		V
I_{dd1}	Digital circuit supply current			1		mA
V_{dd2}	Digital circuit drain supply voltage			2.5		V
I_{dd2}	Digital circuit supply current			13		mA
V_{ee}	Digital circuit negative supply voltage			-5		V
I_{ee}	Digital circuit negative supply current			5		mA
V_g	Gate Bias voltage of MPAs and LNA			-3		V
I_g	Gate Bias current of MPAs and LNA			2.5		mA
RF Performance at 10 GHz						
G	Gain	No Attenuation		+8		dB
NF	Noise Figure	No Attenuation		7		dB
BW	Bandwidth		8		12	GHz
S_{11}	Input reflection coefficient	All states		-17		dB
S_{22}	Output reflection coefficient	All States		-20		dB
ATT_{range}	Attenuation range			24		dB
$ATT_{error\ (RMS)}$	RMS Attenuation error			0.25		dB
$ATT_{variation\ (max)}$	Attenuation variation with phase setting (max)	All Phase States	-2		+2	dB
PH_{range}	Phase range		360			°
$PH_{error\ (RMS)}$	RMS Phase error			5		°
$PH_{variation\ (max)}$	Phase variation with attenuation setting (max)	All Attenuation States	-5		+5	°
$P_{1dB\ (TX)}$	Output 1 dB compression point (TX)			+13		dBm
$P_{1dB\ (RX)}$	Output 1 dB compression point (RX)			+7		dBm
Rate	Serial data rate				150	MHz

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/001/PG” contains more information on the precautions to take.

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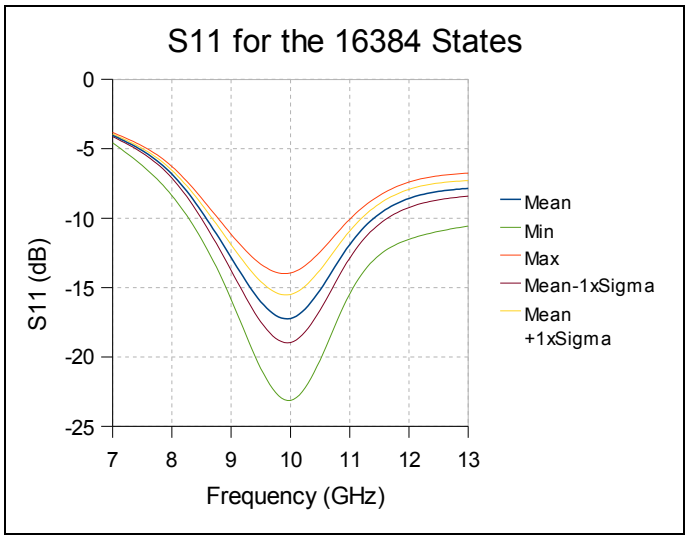
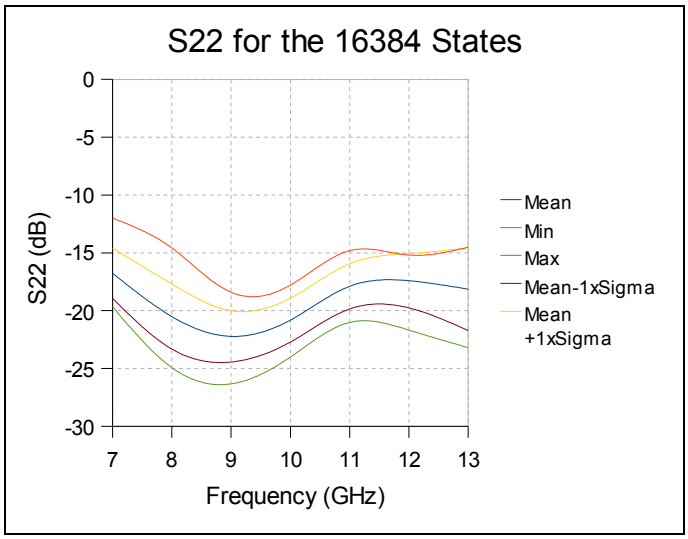
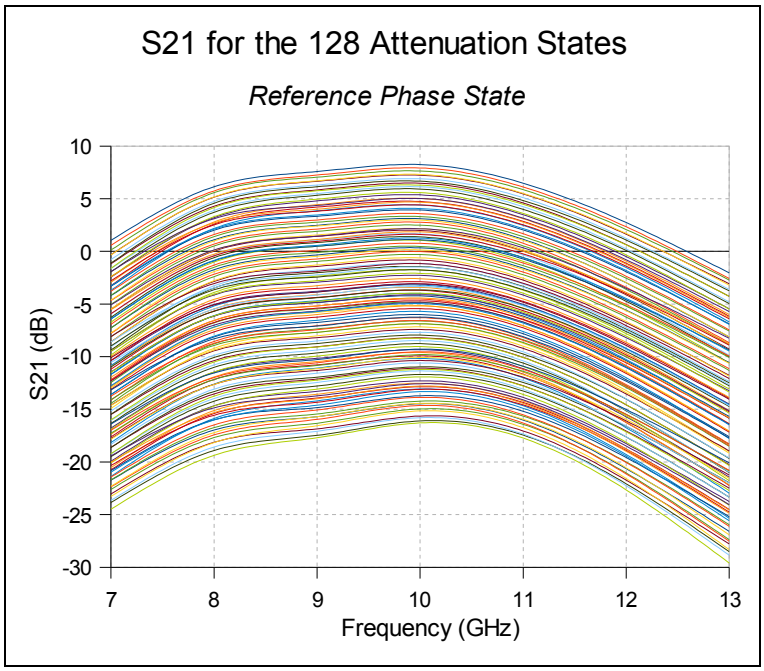
ON WAFER MEASUREMENTS – S PARAMETERS

Measured on RX ports at nominal power supplies voltage
T = 25 °C







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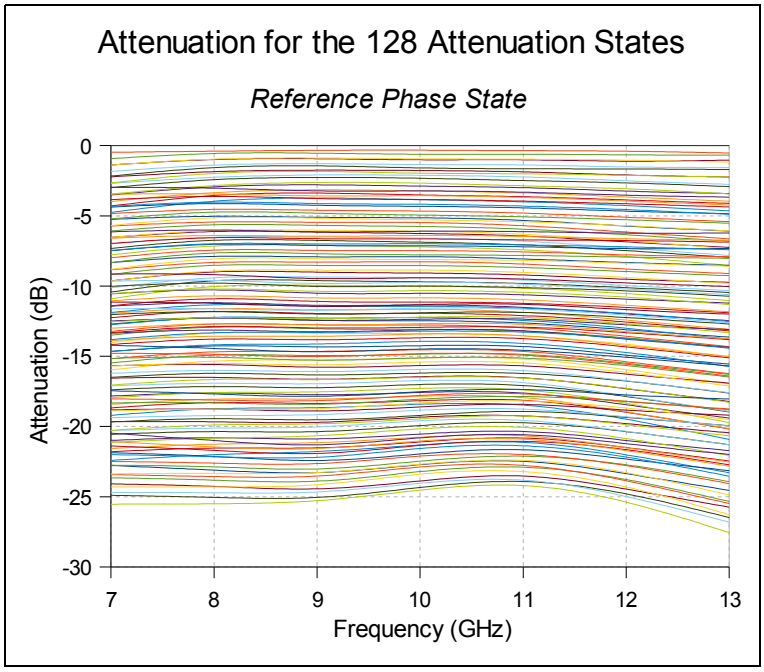
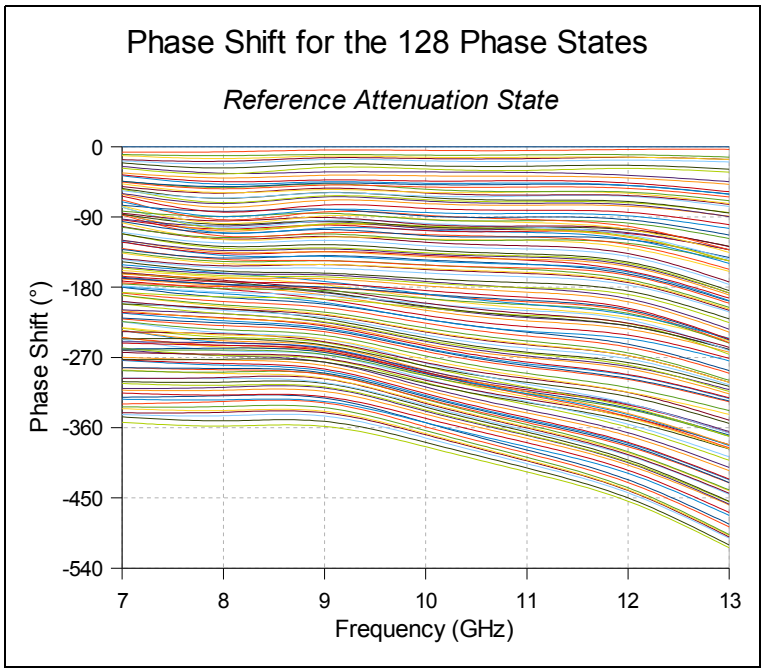
ON WAFER MEASUREMENTS – ATTENUATOR & PHASE SHIFTER RESPONSE

Measured on RX ports @ nominal power supplies voltage
T = 25 °C





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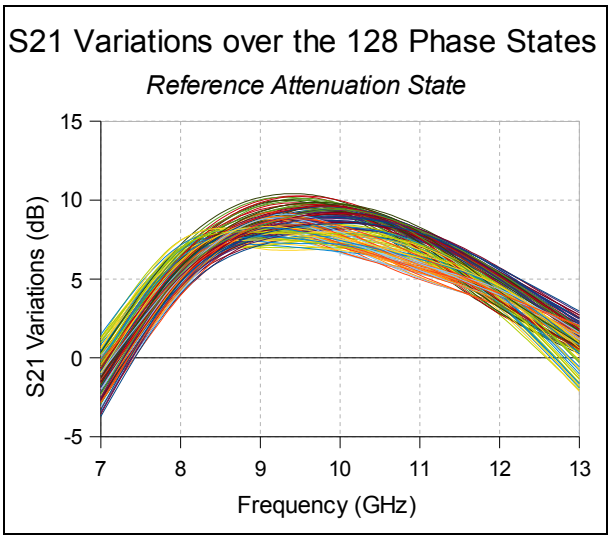
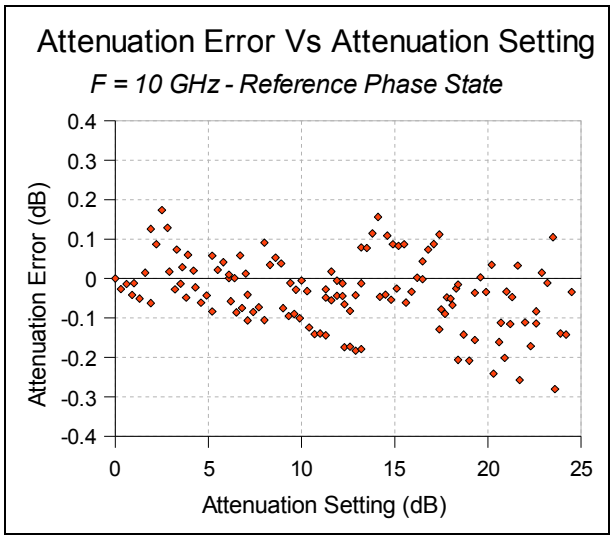
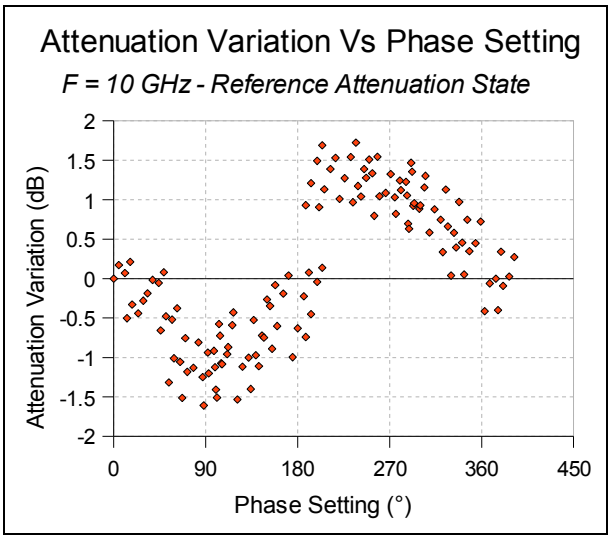
ON WAFER MEASUREMENTS – ATTENUATION ERROR

Measured on RX ports @ nominal power supplies voltage
T = 25 °C







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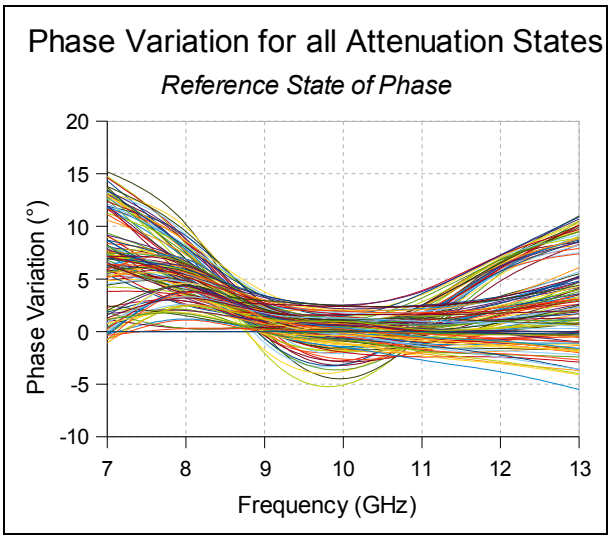
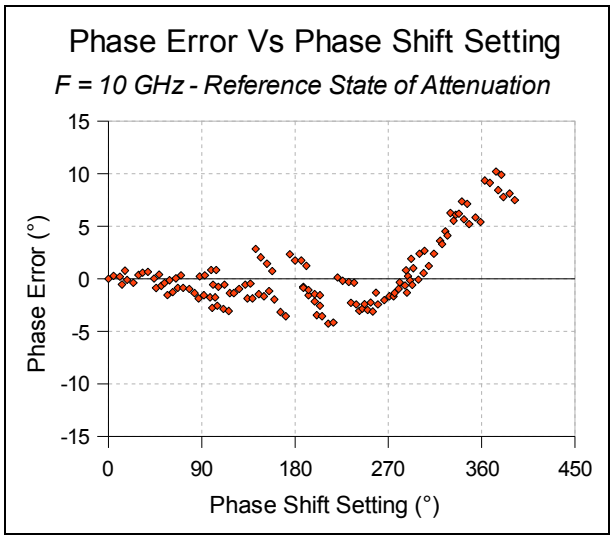
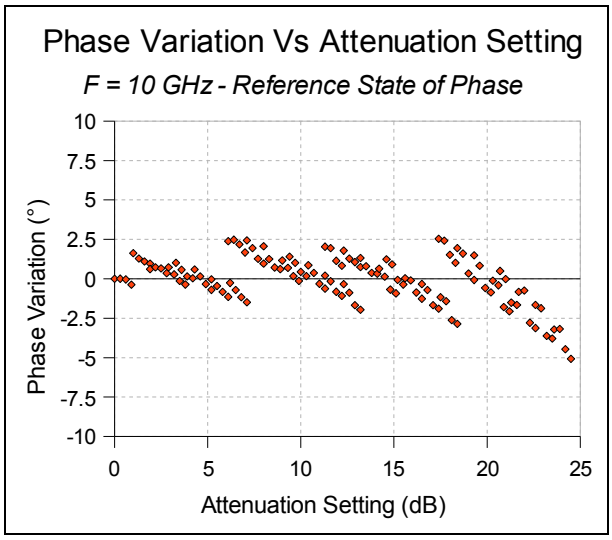
ON WAFER MEASUREMENTS – PHASE SHIFTING ERROR

Measured on RX ports @ nominal power supplies voltage
T = 25 °C







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LOGIC TRUTH TABLE

Control register bits assignments : B0 is loaded first and B15 last, see timing diagram.
Values of phase shift and attenuation given for 10 GHz.

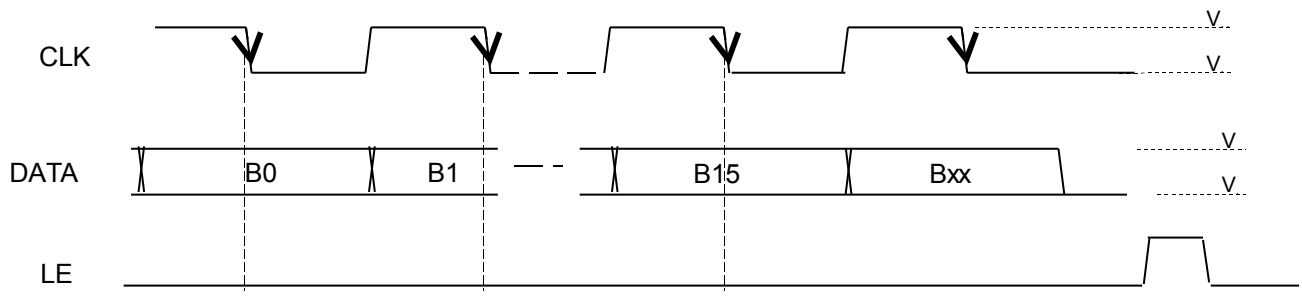
Bit number	Description	Reference state	Value
B0	Phase shifter B6	High	-188°
B1	Phase shifter B5	High	-88°
B2	Phase shifter B4	High	-54°
B3	Not used	Always low	NA
B4	Phase shifter B3	High	-33°
B5	Phase shifter B2	High	-13°
B6	Phase shifter B1	High	-11°
B7	Phase shifter B0	High	-5°
B8	Transmit/receive	High=transmit, low = receive	NA
B9	Attenuator B0	Low	0.3 dB
B10	Attenuator B1	Low	0.6 dB
B11	Attenuator B6	Low	11.3 dB
B12	Attenuator B5	Low	6.1 dB
B13	Attenuator B2	Low	1 dB
B14	Attenuator B4	Low	3.3 dB
B15	Attenuator B3	Low	1.9 dB

CONTROL VOLTAGE (CMOS STANDARD LOGIC)

State	Vmin	Vmax
Low	0 V	1 V
High	+4 V	V_{dd1}

TIMING DIAGRAM

- DATA is sampled at the falling edge of CLK.
- LE must occur when all the bits are loaded and CLK is inactive.
- An extra CLK pulse is necessary at the end with no significant DATA (total of 17 CLK pulses)
- DATA is transferred and Attenuator / Phase Shifter / Switch positions changed on high level of LE



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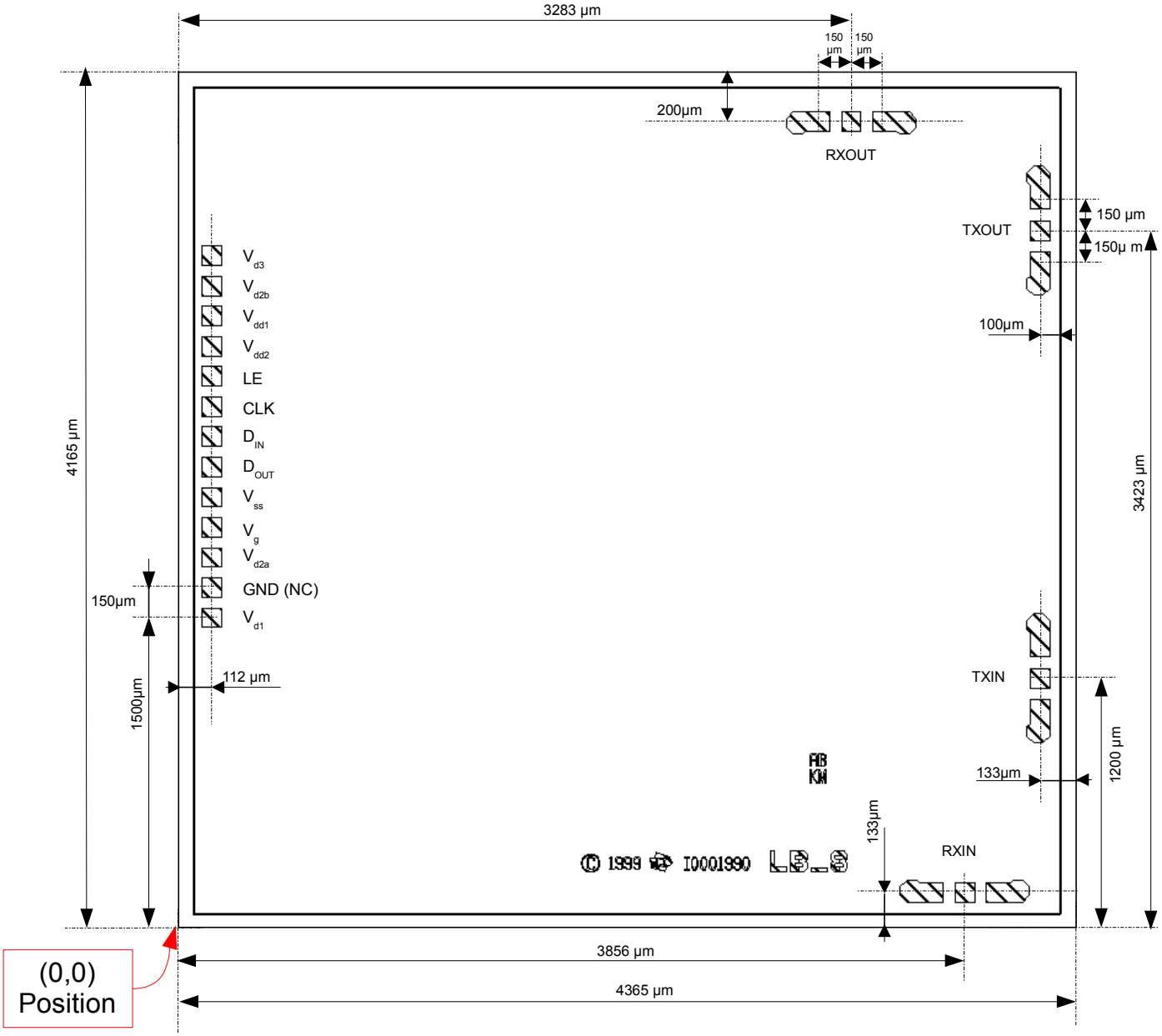
MECHANICAL INFORMATION

Chip size = 4365 x 4165 µm ± 5 µm (after wafer sawing)

- DC Pads = 100 x 100 µm spacing = 150 µm, top metal=Au
- RF Pads = 100 x 100 µm spacing = 150 µm, top metal=Au
- Chip Thickness 100 µm



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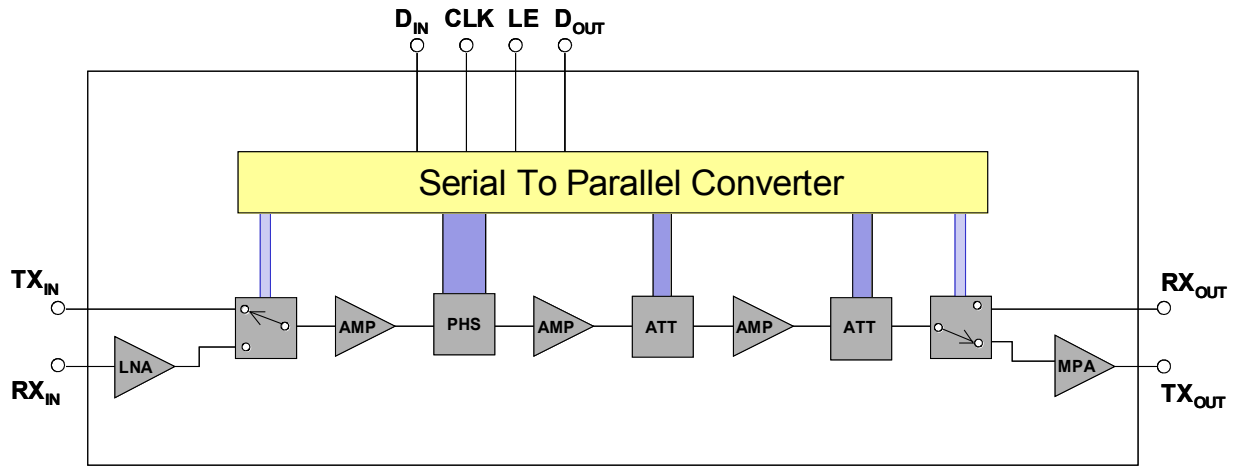
BLOCK DIAGRAM AND PAD CONFIGURATION



Block Diagram of the CGY2170UH fully Integrated X-Band T/R chip

PAD POSITION

SYMBOL	COORDINATES		DESCRIPTION
	X	Y	
V_{d1}	110	1500	Rx mode LNA power supply
V_{d2a}	110	1800	MPA power supply
V_g	110	1950	Control voltage
V_{ss}	110	2100	Digital circuit power supply
D_{OUT}	110	2250	Not used in standard configuration. Can be used for data chaining or testing
D_{IN}	110	2400	Data Input
CLK	110	2450	Clock Input
LE	110	2700	Latch Enable
V_{dd2}	110	2850	Digital circuit power supply
V_{dd1}	110	2980	Digital circuit power supply
V_{d2b}	110	3150	MPA power supply
V_{d3}	110	3300	Tx mode MPA power supply
RX_{IN}	3856	133	RF Input Port (Reception)
TX_{IN}	4232	1200	RF Input Port (Transmission)
TX_{OUT}	4232	3423	RF Output Port (Transmission)
RX_{OUT}	3283	3965	RF Output Port (Reception)

X=0, Y=0 at bottom left corner.
See Mechanical Information for more details.

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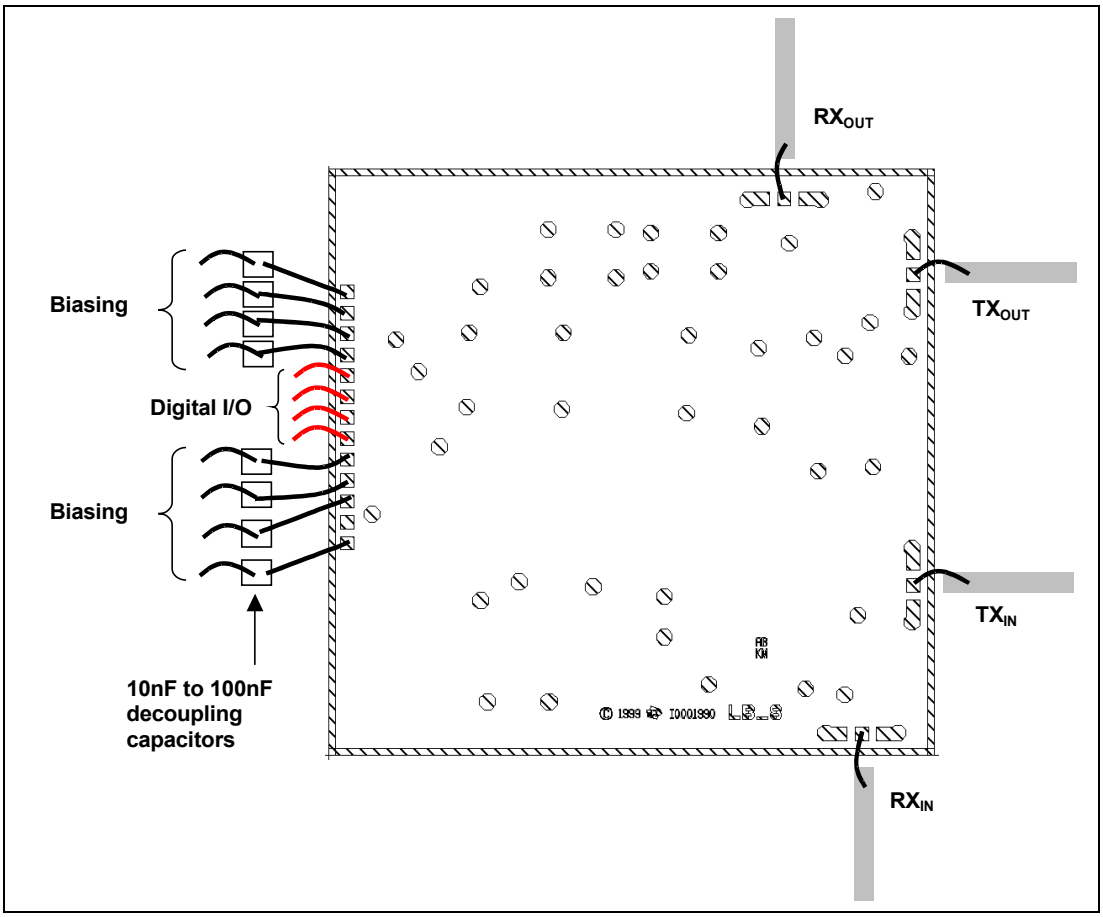
BONDING DIAGRAM AND ASSEMBLY INFORMATION



The RF interfacing bond wires or ribbon should be kept as short as possible. The RF lines should be 200 µm wide or less to minimize discontinuities associated with the connection to the MMIC Bond pads.

Normal High Frequency and Low Frequency precautions should be observed regarding the decoupling of the power supplies.

The OMMIC document “OM-CI-MV/001/PG” gives more details on the precautions to take while handling and sealing GaAs MMIC circuits as well as on the bonding and mounting conditions.

ORDERING INFORMATION

Generic type	Package type	Version	Description
CGY2170UH	Bare Die	C1	7-bit X-band Core Chip

The CGY2170UH/C1 is RoHS Compliant.

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DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
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