

# CA-IS2092 2.5kV<sub>RMS</sub> Isolated RS-485/RS-422 Transceivers with Integrated DC-DC Converter

## 1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - 0.5Mbps data rate
  - 1/8 unit load enables up to 256 nodes on the bus
  - 3V to 5.5V supply voltage range, and the CA-IS2092VW provides individual logic supply input
- **Integrated DC-DC Converter for Cable-side Power**
  - 3.3V and 5V output options ( $V_{ISO} \leq V_{CC}$ )
  - High integration with internal transformer
  - Soft-start reduces input inrush current
  - Overload and short-circuit protection
  - Thermal shutdown
- **Integrated Protection for Robust Communication**
  - 2.5kV<sub>RMS</sub> withstand isolation voltage for 60s (galvanic isolation)
  - $\pm 150\text{kV}/\mu\text{s}$  typical CMTI
  - High lifetime: >40 years
  - $\pm 20\text{kV}$  Human Body Model(HBM) ESD protection on bus I/O,  $\pm 6\text{kV}$  HBM ESD protection on logic I/O
  - True fail-safe guarantees known receiver output state
  - Wide operating temperature range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- **Wide-body SOIC16-WB(W) Package**
- **Safety Regulatory Approvals(pending)**
  - 3535V<sub>PK</sub> V<sub>IOTM</sub> and 849V<sub>PK</sub> V<sub>IORM</sub> per DIN VDE V0884-11:2017-01
  - 2.5kV<sub>RMS</sub> isolation for 1 minute per UL 1577
  - IEC 60950-1, IEC 60601-1 and EN 61010-1 certifications
  - CQC, TUV, and CSA certifications

## 2. Applications

- Industrial Automation Equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

## 3. General Description

The CA-IS2092x family of devices is galvanically-isolated RS-485/RS-422 transceivers with built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO<sub>2</sub>) insulation barrier that provides up to 2.5kV<sub>RMS</sub> (60s) of galvanic isolation and  $\pm 150\text{kV}/\mu\text{s}$  typical CMTI. Isolation improves data communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports. An integrated DC-DC converter generates the 3.3V or 5V operating voltage for the cable-side.

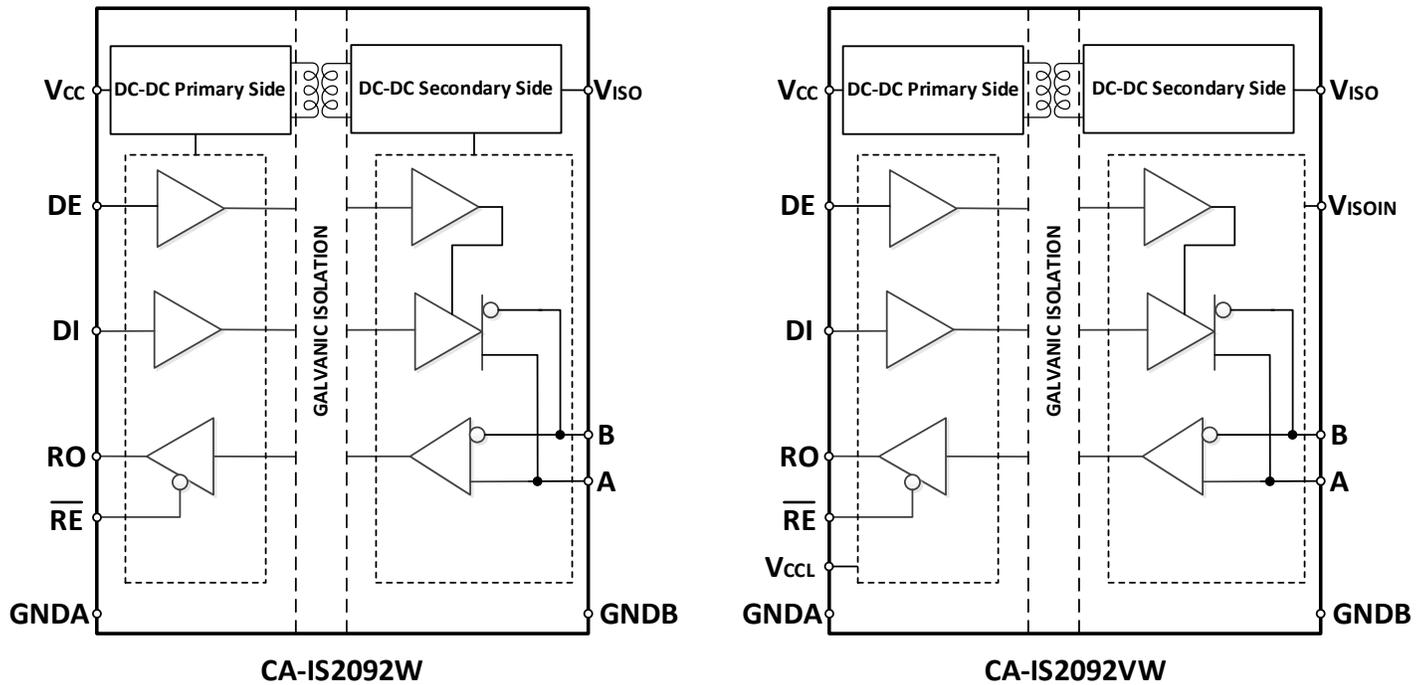
The CA-IS2092x family of devices is designed for multi-drop operation with high ESD protection of up to  $\pm 20\text{kV}$  HBM on the bus pins. The receiver is 1/8-unit load, allowing up to 256 transceivers (loads) on a common bus. These devices provide half-duplex transceivers, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements. The individual logic supply input of CA-IS2092VW allows fully compatible 2.5V to 5.5V logic on logic input/output lines.

The CA-IS2092x series devices are available in wide-body 16-pin SOIC package which are the industry standard isolated RS-485/RS-422 package, and operate over  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS2092W CA-IS2092VW	SOIC16-WB(W)	10.30 mm × 7.50 mm

CA-IS2092x Function Diagram



#### 4. Ordering Information

Table 4-1. Ordering Information

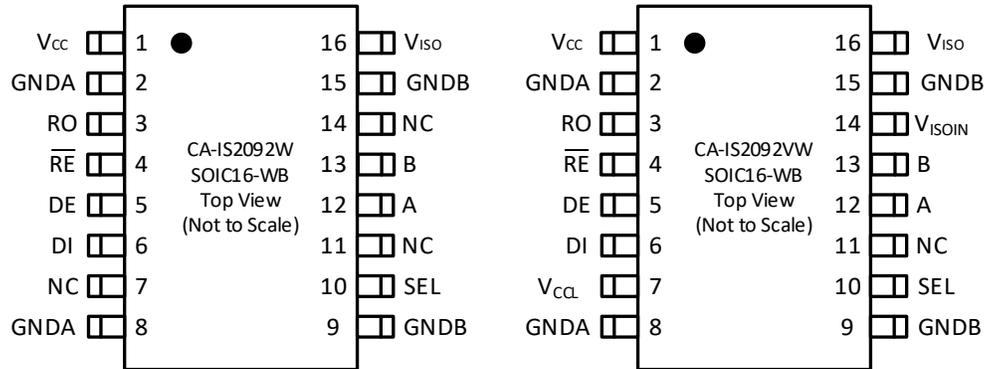
Part Number	Full/half duplex	Data Rate (Mbps)	V <sub>ISO</sub> (V)	V <sub>DDL</sub>	Package
CA-IS2092W	Half-Duplex	0.5	3.3/5.0	N/A	SOIC16-WB(W)
CA-IS2092VW	Half-Duplex	0.5	3.3/5.0	Yes	SOIC16-WB(W)

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### 5. Revision History

Revision Number	Description	Page Changed
Version 1.00	Preliminary Version	N/A
Version 1.01	Changed $t_{PHZ}, t_{PLZ}$ value.	10
Version 1.02	Updated POD.	25
Version 1.03	Changed UL certification information.	7

**6. Pin Configuration and Description**

**Figure 6-1. CA-IS2092W/CA-IS2092VW SOIC16 Top View**
**Table 6-1. CA-IS2092W/CA-IS2092VW Pin Description and Functions**

Name	PIN Number		Type	Description
	CA-IS2092W	CA-IS2092VW		
V <sub>CC</sub>	1	1	Power Supply	Logic-Side Power Input and DC-DC converter supply input. Bypass V <sub>CC</sub> to GNDA with both 0.1μF and at least 10μF capacitors as close to the device as possible.
GNDA	2, 8	2, 8	GND	Logic-Side Ground. GNDA is the ground reference for digital signals of logic side.
RO	3	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver R <sub>x</sub> . With $\overline{RE}$ low, RO is high when (V <sub>A</sub> - V <sub>B</sub> ) > -20mV and is low when (V <sub>A</sub> - V <sub>B</sub> ) < -200mV. RO is high impedance when $\overline{RE}$ is high.
$\overline{RE}$	4	4	Digital I/O	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable R <sub>x</sub> . Drive $\overline{RE}$ high to disable R <sub>x</sub> . RO is high-impedance when $\overline{RE}$ is high.
DE	5	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
V <sub>CCL</sub> <sup>1</sup>	---	7	Power Supply	Logic-supply input. V <sub>CCL</sub> is the logic supply voltage for logic-side input/output. Bypass to GNDA with a 1μF capacitor.
NC	7	---	---	No internal connection on logic side.
GNDB	9, 15	9, 15	GND	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
SEL <sup>2</sup>	10	10	Digital I/O	Output voltage V <sub>ISO</sub> select pin: V <sub>ISO</sub> = 5.0 V when SEL is shorted to V <sub>ISO</sub> ; V <sub>ISO</sub> = 3.3 V when SEL is shorted to GNDB or floating;
NC	11, 14	11	---	No internal connection on cable side.
A	12	12	Bus I/O	Non-inverting RS-485/RS-422 receiver input and driver output.
B	13	13	Bus I/O	Inverting RS-485/RS-422 receiver input and driver output.
V <sub>ISOIN</sub>	---	14	Power Supply	Cable side power supply input. Bypass V <sub>ISOIN</sub> to GNDB with at least 1μF capacitor as close to the device as possible.
V <sub>ISO</sub>	16	16	Power Supply	Isolated DC-DC power supply output. Cable Side Power supply. Bypass V <sub>ISO</sub> to GNDB with both 0.1μF and at least 10μF capacitors as close to the device as possible.

**Notes:**

- Logic-Supply Input. V<sub>CCL</sub> can be different voltage from V<sub>CC</sub> supply, which allows fully compatible +2.7V to +5.5V logic for digital input/output.
- V<sub>ISO</sub> ≤ V<sub>CC</sub>, this means if V<sub>CC</sub> = 3.3V, SEL pin must be floating or connected to GNDB and set the V<sub>IOs</sub> output to 3.3V; if V<sub>CC</sub> = 5.0V, there is no connection limit for SEL pin.

## 7. Specifications

### 7.1. Absolute Maximum Ratings<sup>1</sup>

PARAMETER	MIN	MAX	UNIT
$V_{CC}, V_{CCL}$	-0.5	6.0	V
$V_{ISO}, V_{ISOIN}$	-0.5	6.0	V
$V_{IO1}$	-0.5	$V_{CC}/V_{CCL} + 0.5^3$	V
$V_{IO2}$	-0.5	$V_{ISO}/V_{ISOIN} + 0.5^3$	V
$V_{BUS}$	-8	13	V
$I_O$	-20	20	mA
$T_J$		150	°C
$T_{STG}$	-65	150	°C

**Notes:**

- The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 6V.

### 7.2. ESD Ratings

PARAMETER	VALUE	UNIT
$V_{ESD}$ Electrostatic discharge	Bus pins to GNDB	±20
	Other pins on cable-side to GNDB	±6
	All pins on logic-side to GNDA	±6
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>2</sup>	±2	kV

**Notes:**

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

### 7.3. Recommended Operating Conditions

PARAMETER	Min	Typ.	Max	Unit
$V_{CC}^1$	3.15	3.3 or 5	5.5	V
$V_{CCL}$	2.375	3.3 or 5	5.5	V
$V_{OC}$	-7		12	V
$V_{ID}$	-12		12	V
RL	54			Ω
$V_{IH}$	2.0		$V_{CC}/V_{CCL} + 0.3$	V
$V_{IL}$	-0.3		0.8	V
$V_{IH}$	$0.7 \times V_{CC}/V_{CCL}$		$V_{CC}/V_{CCL} + 0.3$	V
$V_{IL}$	-0.3		$0.3 \times V_{CC}/V_{CCL}$	V
DR			0.5	Mbps
$T_A$	-40		125	°C

**Note:**

- $V_{ISO} \leq V_{CC}$ , this means if  $V_{CC} = 3.3V$ , SEL pin must be floating or connected to GNDB and set the  $V_{IOs}$  output to 3.3V; if  $V_{CC} = 5.0V$ , there is no connection limit for SEL pin.

### 7.4. Thermal Information

THERMAL METRIC	CA-IS2092x	Unit
	SOIC16-WB(W)	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	68.5	°C/W

**7.5. Insulation Specifications**

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			W/T	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 300 V_{RMS}$	I-IV	
		Rated mains voltage $\leq 400 V_{RMS}$	I-IV	
		Rated mains voltage $\leq 600 V_{RMS}$	I-III	
<b>DIN V VDE V 0884-11:2017-01<sup>1</sup></b>				
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	$V_{PK}$
$V_{IOWM}$	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	$V_{RMS}$
		DC voltage	849	$V_{DC}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , $t=60$ s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ , $t=1$ s (100% product test)	3535	$V_{PK}$
$V_{IOSM}$	Maximum surge isolation voltage <sup>2</sup>	Test method per IEC 60065, 1.2/50μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	4000	$V_{PK}$
$q_{pd}$	Apparent charge <sup>3</sup>	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10$ s	$\leq 5$	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10$ s	$\leq 5$	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1$ s; $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1$ s	$\leq 5$	
$C_{IO}$	Barrier capacitance, input to output <sup>4</sup>	$V_{IO} = 0.4 \times \sin(2\pi ft)$ , $f = 1$ MHz	~0.5	pF
$R_{IO}$	Isolation resistance, input to output <sup>4</sup>	$V_{IO} = 500V$ , $T_A = 25^\circ C$	$>10^{12}$	$\Omega$
		$V_{IO} = 500V$ , $100^\circ C \leq T_A \leq 125^\circ C$	$>10^{11}$	
		$V_{IO} = 500V$ at $T_S = 150^\circ C$	$>10^9$	
	Pollution degree		2	
<b>UL 1577</b>				
$V_{ISO}$	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1$ s (100% production)	2500	$V_{RMS}$
<b>Notes:</b>				
1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.				
2. Devices are immersed in oil during surge characterization.				
3. The characterization charge is discharging charge (pd) caused by partial discharge.				
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

**7.6. Safety-Related Certifications**

VDE(Pending)	UL	TUV(Pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Certification number: pending	Certification number: E511334-20210507	Certification number: pending

## 7.7. Electrical Characteristics

### 7.7.1. Driver

All typical specs are at  $V_{CC} = 5V$ ,  $V_{CCL} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter	Test Condition	Min	Typ.	Max	Unit
V <sub>OD1</sub>	Driver differential output voltage I <sub>O</sub> = 0mA, unloaded bus. SEL = LOW or float	2.9		3.7	V
		4.6			
V <sub>OD2</sub>	Driver differential output voltage R <sub>L</sub> =54Ω, see Figure 8-1, SEL = LOW or float	1.5		2.1	V
		2			
V <sub>OD3</sub>	Driver differential output voltage with bus load R <sub>L</sub> =54Ω, see Figure 8-1, SEL = HIGH	3.6		1.5	V
		2.1			
Δ V <sub>OD1</sub>	Change in differential output voltage between two states V <sub>test</sub> = -7V to 12V, see Figure 8-1	1.5		0.2	V
V <sub>OC</sub>	Common-mode output voltage R <sub>L</sub> =54Ω, or R <sub>L</sub> =100Ω, see Figure 8-1	1	V <sub>ISO</sub> /2	3	V
ΔV <sub>OC</sub>	Change in steady-state common-mode output voltage between two states R <sub>L</sub> =54Ω, or R <sub>L</sub> =100Ω, see Figure 8-1	-0.2		0.2	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current DI, DE = low or high	-20		20	μA
I <sub>OS</sub>	Short-circuit output current (V <sub>O</sub> = HIGH) DE = V <sub>CC</sub> , DI = 0V or V <sub>CC</sub> , V <sub>A</sub> or V <sub>B</sub> = -7V	-150		150	mA
		DE = V <sub>CC</sub> , DI = 0V or V <sub>CC</sub> , V <sub>A</sub> or V <sub>B</sub> = 12V			
CMTI	Common mode transient immunity V <sub>CM</sub> = 1200V; See Figure 8-6	100	150		kV/μS

### 7.7.2. Receiver

All typical specs are at  $V_{CC} = 5V$ ,  $V_{CCL} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter	Test Condition	Min	Typ.	Max	Unit
V <sub>OH</sub>	Output logic high voltage V <sub>CC</sub> =5V, I <sub>OH</sub> =4mA	V <sub>CC</sub> -0.4		4.8	V
		V <sub>CC</sub> -0.4		3	
V <sub>OL</sub>	Output logic low voltage V <sub>CC</sub> =5V, I <sub>OL</sub> =4mA	0.2		0.4	V
		0.2		0.4	
V <sub>IT+(IN)</sub>	Positive-going input threshold voltage	-110		-50	mV
V <sub>IT-(IN)</sub>	Negative-going input threshold voltage	-200		-140	mV
V <sub>I(HYS)</sub>	Receiver input hysteresis	30			mV
I <sub>I</sub>	Bus input current V <sub>A</sub> or V <sub>B</sub> =12V, other inputs = 0V	75		125	μA
		80		125	
		-100		-40	
		-100		-40	
I <sub>IH</sub>	Input current on $\overline{RE}$ pin V <sub>IH</sub> = V <sub>CC</sub>	-20		20	μA
I <sub>IL</sub>	Input current on $\overline{RE}$ pin V <sub>IL</sub> = 0V	-20		20	μA
R <sub>ID</sub>	Differential input resistance A, B, -7V < V <sub>CM</sub> < 12V	96			KΩ

**7.8. Supply Current**

 All typical specs are at  $V_{CC} = 5V$ ,  $V_{CC} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions.

Parameter		Test Condition	Min	Typ.	Max	Unit
<b>Isolated Power Supply (without bus load across A and B, unless otherwise specified.)</b>						
$V_{ISO}$	Isolated supply output	$I_{ISO} = 0$ to 130mA, $V_{CC} = 5V$ , SEL = GNDB or $V_{ISO}$	4.75	5	5.25	V
		$I_{ISO} = 0$ to 75mA, $V_{CC} = 3.3V$ , SEL = GNDB	3.13	3.3	3.47	
$I_{ISO}$	Maximum load current <sup>1</sup>	$R_L = NC^2$	$V_{CC} = 5V$ , SEL = GNDB or $V_{ISO}$	130		mA
			$V_{CC} = 3.3V$ , SEL = GNDB	75		
		$R_L = 100\Omega$	$V_{CC} = 5V$ , SEL = $V_{ISO}$	80		
			$V_{CC} = 5V$ , SEL = GNDB	105		
			$V_{CC} = 3.3V$ , SEL = GNDB	40		
		$R_L = 54\Omega$	$V_{CC} = 5V$ , SEL = $V_{ISO}$	55		
			$V_{CC} = 5V$ , SEL = GNDB	85		
			$V_{CC} = 3.3V$ , SEL = GNDB	30		
		$V_{ISO(LINE)}$	DC line regulation	$I_{ISO} = 50mA$ , $V_{CC} = 4.5$ to 5.5V, SEL = GNDB or $V_{ISO}$	2	
$I_{ISO} = 50mA$ , $V_{CC} = 3.15$ to 3.6V, SEL = GNDB						
$V_{ISO(LOAD)}$	DC load regulation	$I_{ISO} = 0$ to 130mA, $V_{CC} = 5V$ , SEL = GNDB or $V_{ISO}$	1%			
		$I_{ISO} = 0$ to 75mA, $V_{CC} = 3.3V$ , SEL = GNDB				
EFF	Efficiency @ maximum load current	$I_{ISO} = 130mA$ , $C_{LOAD} = 0.1\mu F // 10\mu F$	$V_{CC} = 5V$ , SEL = $V_{ISO}$	53%		
			$V_{CC} = 5V$ , SEL = GNDB	42%		
		$I_{ISO} = 75mA$ , $C_{LOAD} = 0.1\mu F // 10\mu F$	$V_{CC} = 3.3V$ , SEL = GNDB	47%		
<b>Quiescent current, DE = <math>V_{CC}</math>, <math>\overline{RE} = 0V</math>, DI = 0V</b>						
$I_{CC}$	Supply current on logic side	$R_L = NC^2$	$V_{CC} = 3.3V$ , SEL = GNDB	17	28	mA
			$V_{CC} = 5.0V$ , SEL = GNDB	15	22	
			$V_{CC} = 5.0V$ , SEL = $V_{ISO}$	18	28	
		$R_L = 54\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	94	125	
			$V_{CC} = 5.0V$ , SEL = GNDB	82	120	
			$V_{CC} = 5.0V$ , SEL = $V_{ISO}$	140	200	
		$R_L = 100\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	65	95	
			$V_{CC} = 5.0V$ , SEL = GNDB	55	80	
			$V_{CC} = 5.0V$ , SEL = $V_{ISO}$	93	135	
		$R_L = 120\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	57	88	
			$V_{CC} = 5.0V$ , SEL = GNDB	50	72	
			$V_{CC} = 5.0V$ , SEL = $V_{ISO}$	83	120	
<b>Average operating current, DE = <math>V_{CC}</math>, <math>\overline{RE} = 0V</math>, DI = 250kHz square-wave, 50% duty cycle.</b>						
$I_{CC}$	Supply current on logic side	$R_L = 54\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	92	125	mA
			$V_{CC} = 5V$ , SEL = GNDB	85	120	
			$V_{CC} = 5V$ , SEL = $V_{ISO}$	145	210	
		$R_L = 100\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	65	95	
			$V_{CC} = 5V$ , SEL = GNDB	60	85	
			$V_{CC} = 5V$ , SEL = $V_{ISO}$	100	145	
		$R_L = 120\Omega$	$V_{CC} = 3.3V$ , SEL = GNDB	60	85	
			$V_{CC} = 5V$ , SEL = GNDB	55	80	
			$V_{CC} = 5V$ , SEL = $V_{ISO}$	95	140	
<b>Notes:</b>						
1. DE = $V_{CC}$ , $\overline{RE} = 0V$ , DI = 0V or $V_{CC}$ ; The available output current from $V_{ISO}$ will be reduced when $T_A > 85^\circ C$ , see 错误!未找到引用源。 , 错误!未找到引用源。 , the maximum output current of $V_{ISO}$ vs. temperature.						
2. $R_L$ is bus load across A and B, $R_L = NC$ means no-load connection between CANH and CANL.						

## 7.9. Switching Characteristics

### 7.9.1. Driver

All typical specs are at  $V_{CC} = 5V$ ,  $V_{CCL} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters	Test conditions	Minimum value	TYP	Maximum value	Unit
$t_{PLH}, t_{PHL}$	Driver Propagation Delay		100	250	ns
$t_{PWD}$	Driver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-2	5	20	ns
$t_r, t_f$	Differential output rise/full time		150	500	ns
$t_{PZH}, t_{PZL}$	Driver enable time		300	800	ns
$t_{PHZ}, t_{PLZ}$	Driver disable time	See Figure 8-3	20	50	ns

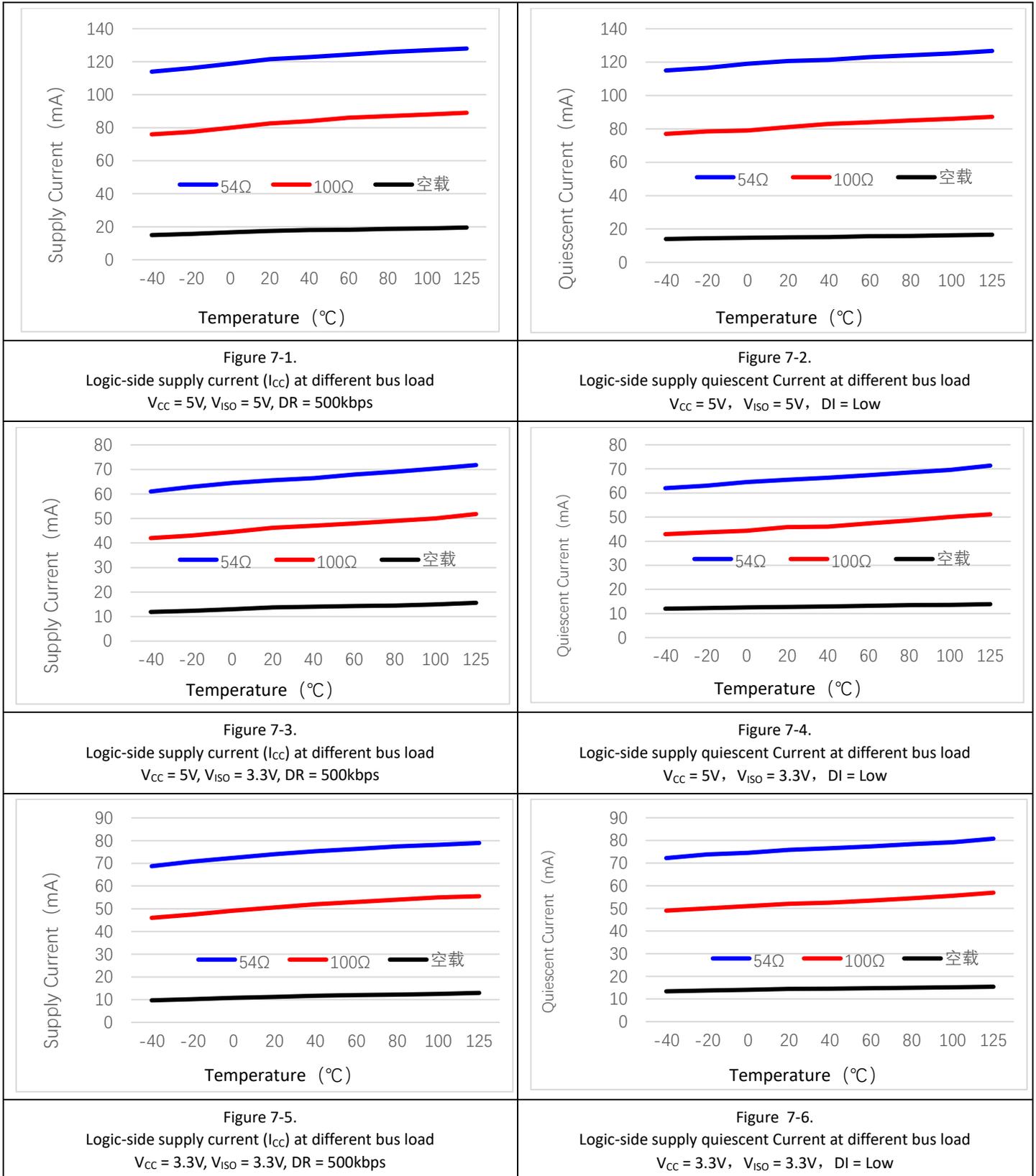
### 7.9.2. Receiver

All typical specs are at  $V_{CC} = 5V$ ,  $V_{CCL} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters	Test conditions	Minimum value	TYP	Maximum value	Unit
$t_{PLH}, t_{PHL}$	Receiver propagation delay		50	100	ns
$t_{PWD}$	Receiver output skew $ t_{PLH} - t_{PHL} $	See Figure 8-4.		12	ns
$t_r, t_f$	Receiver output rise/full time		2.5	4	ns
$t_{PHZ}, t_{PLZ}$	Receiver disable time		20	50	ns
$t_{PZH}, t_{PZL}$	Receiver enable time, $DE = 0V$	See Figure 8-5.	30	80	ns

**7.10. Typical Operating Characteristics**

All typical specs are at  $V_{CC} = 5V$ ,  $V_{CC1} = V_{CC}$ ,  $V_{ISOIN} = V_{ISO}$ ,  $T_A = 25^\circ C$ , Min/Max specs are over recommended operating conditions unless otherwise specified.



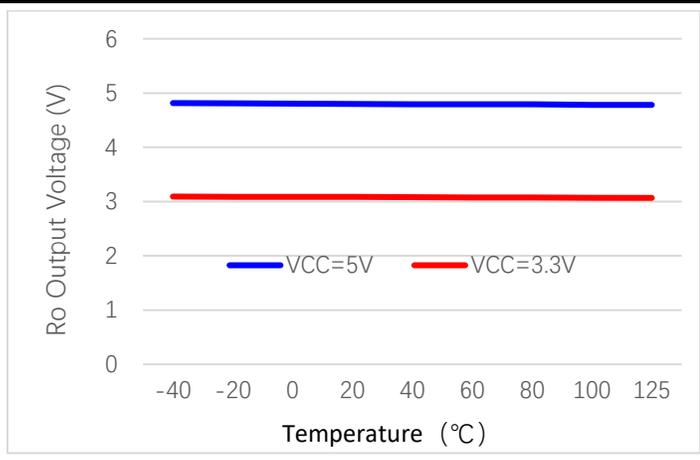


Figure 7-7.  
R<sub>O</sub> = High, R<sub>O</sub> pull-down current is 4mA

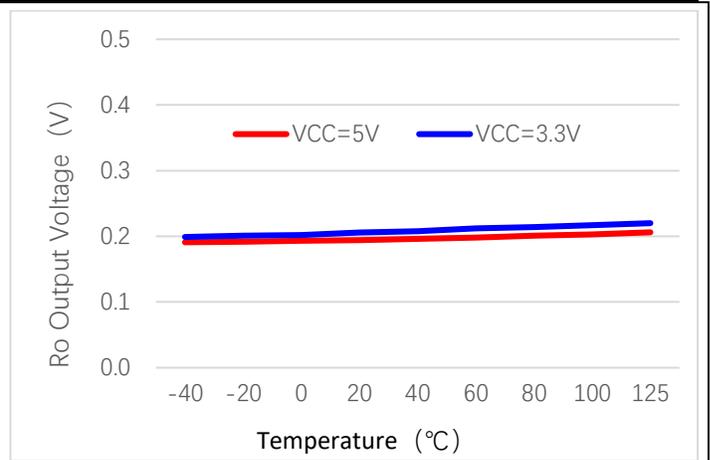


Figure 7-8.  
R<sub>O</sub> = Low, R<sub>O</sub> pull-up current = 4mA

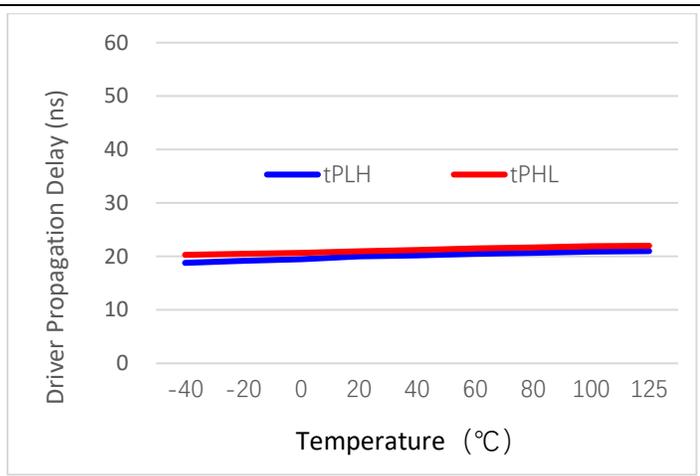


Figure 7-9. Driver propagation delay  
V<sub>CC</sub> = 3.3V, V<sub>ISO</sub> = 3.3V, R<sub>L</sub> = 54Ω

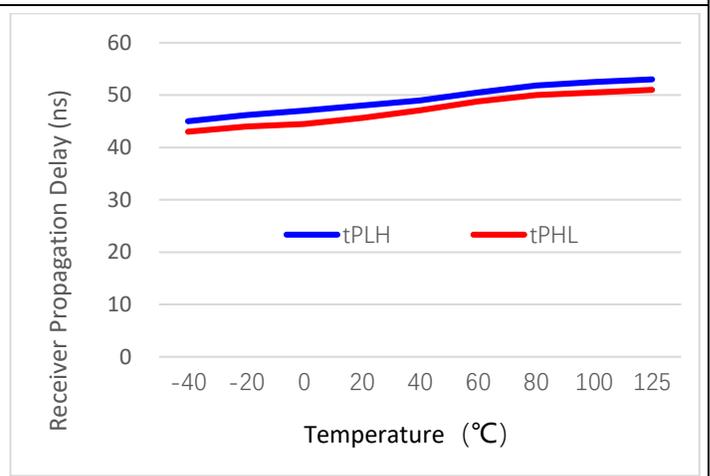


Figure 7-10. Receiver propagation delay  
V<sub>CC</sub> = 3.3V, V<sub>ISO</sub> = 3.3V, R<sub>L</sub> = 54Ω

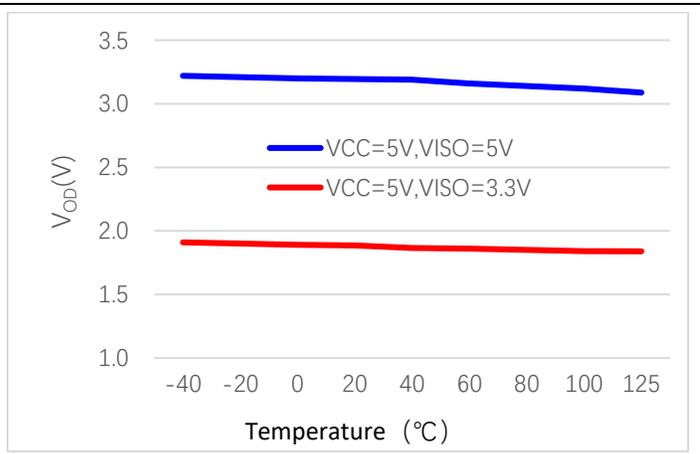


Figure 7-11.  
Differential output voltage V<sub>OD</sub>, R<sub>L</sub> = 54Ω, V<sub>CC</sub> = 5V

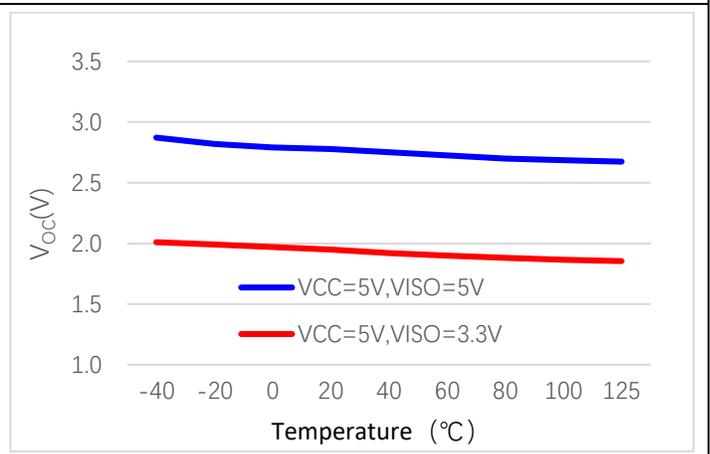


Figure 7-12.  
Common-mode output voltage V<sub>OC</sub>, R<sub>L</sub> = 54Ω, V<sub>CC</sub> = 5V

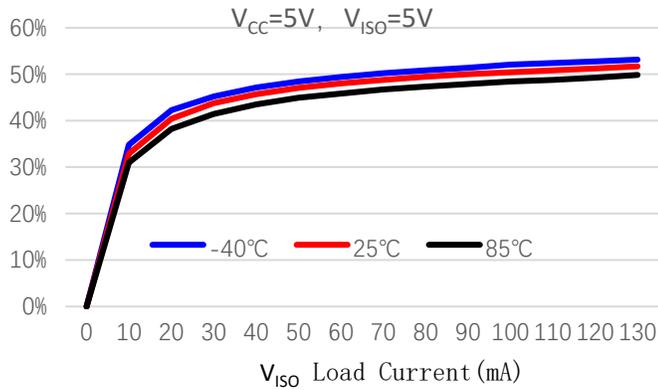


Figure 7-13.

Efficiency vs. load current ( $I_{ISO}$ ) at different ambient temperature  
 $V_{CC} = 5V, V_{ISO} = 5V, R_L = NC$

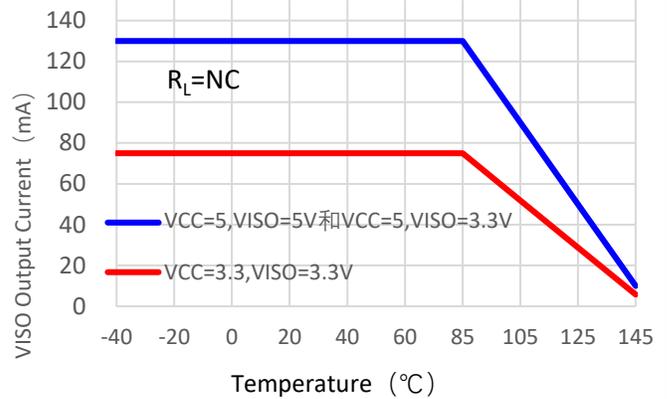


Figure 7-14.

Maximum output current from  $V_{ISO}$  vs. temperature with  $R_L = NC$   
 Without data transmission

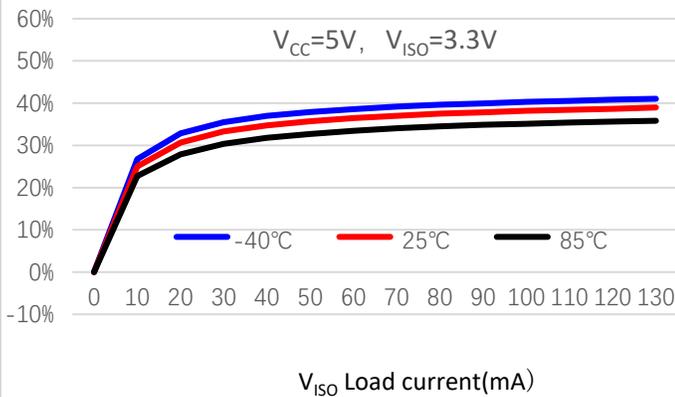


Figure 7-15.

Efficiency vs. load current ( $I_{ISO}$ ) at different ambient temperature  
 $V_{CC} = 5V, V_{ISO} = 3.3V, R_L = NC$

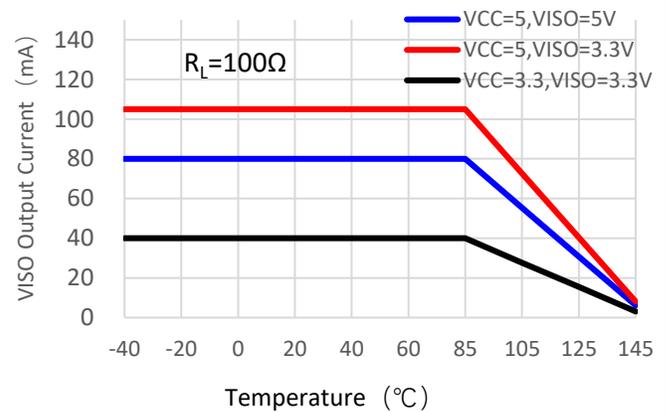


Figure 7-16.

Maximum output current from  $V_{ISO}$  vs. temperature with  $R_L = 100\Omega$   
 CA-IS2092x: DR = 500kbps,  $C_L = 2nF$

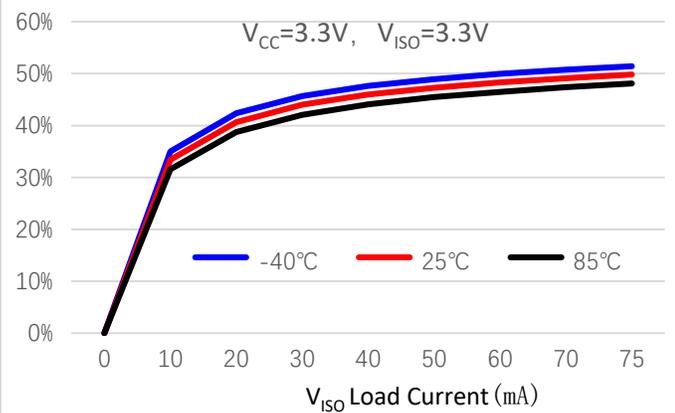


Figure 7-17.

Efficiency vs. load current ( $I_{ISO}$ ) at different ambient temperature  
 $V_{CC} = 3.3V, V_{ISO} = 3.3V, R_L = NC$

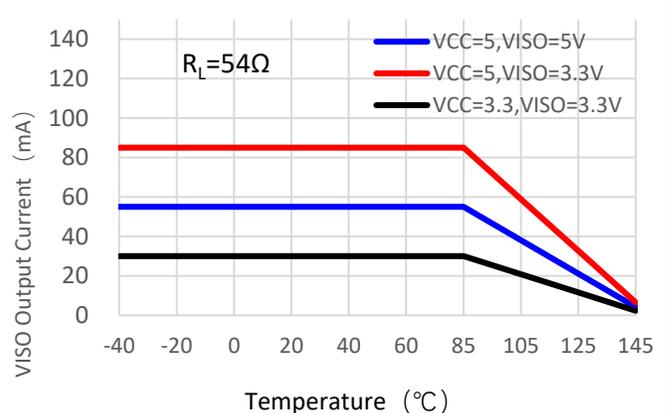
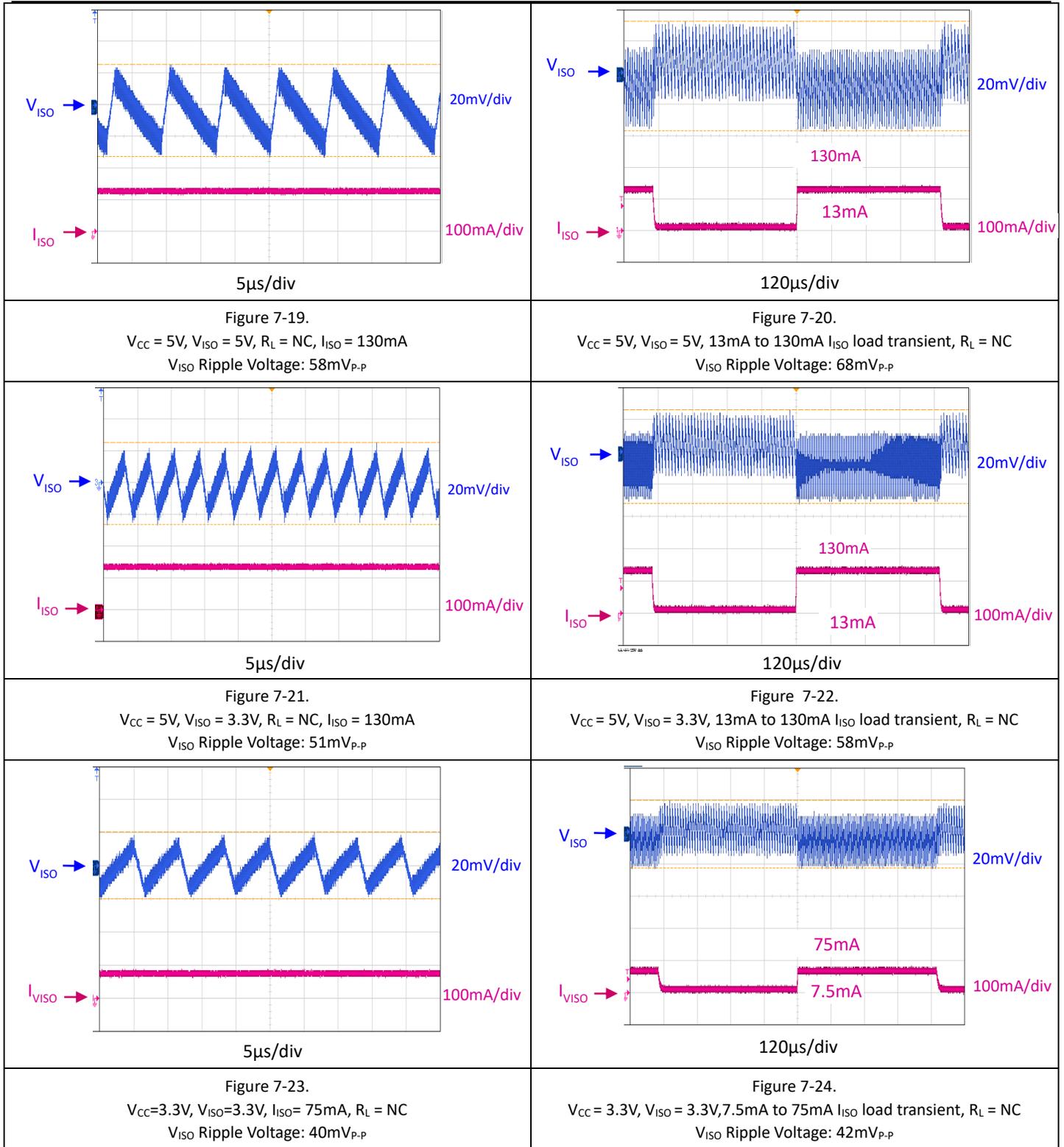


Figure 7-18.

Maximum output current from  $V_{ISO}$  vs. temperature with  $R_L = 54\Omega$   
 CA-IS2092x: DR = 500kbps,  $C_L = 2nF$



8. Parameter Measurement Information

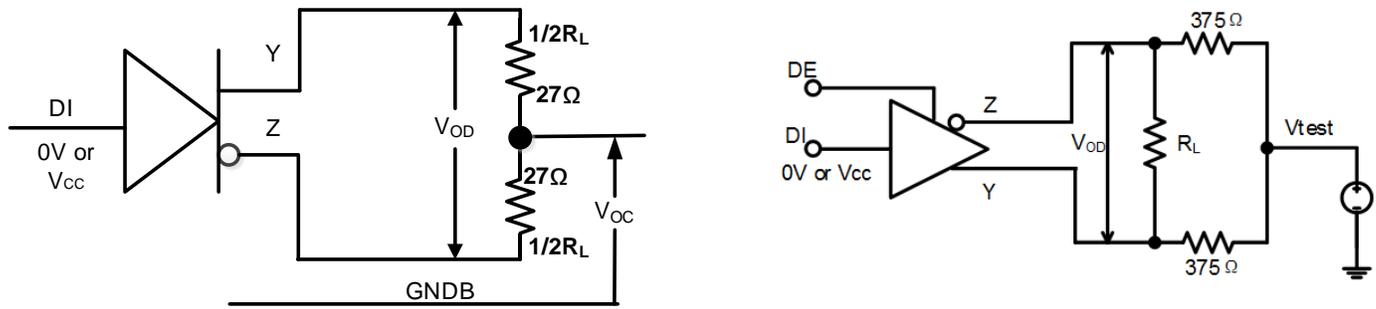


Figure 8-1. Driver DC Test Circuit

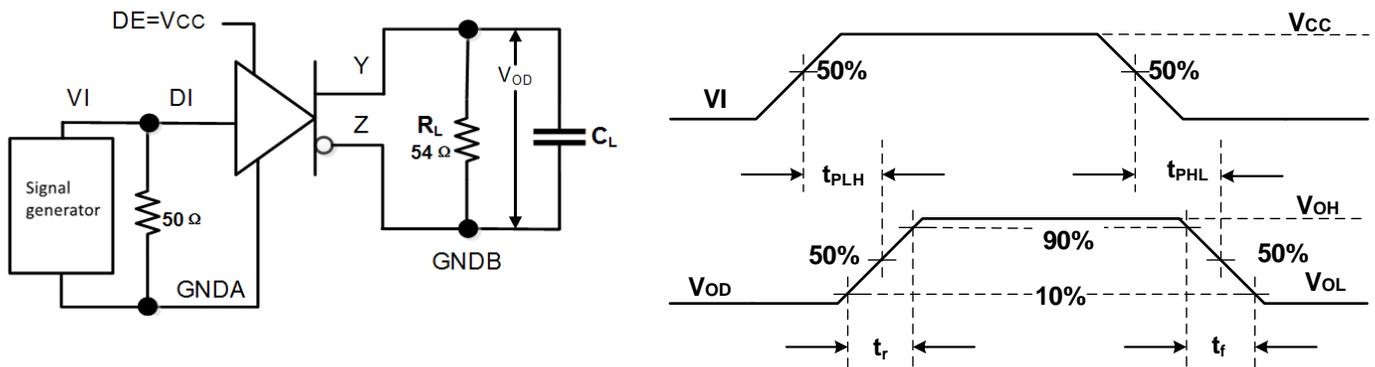


Figure 8-2. Driver Propagation Delays

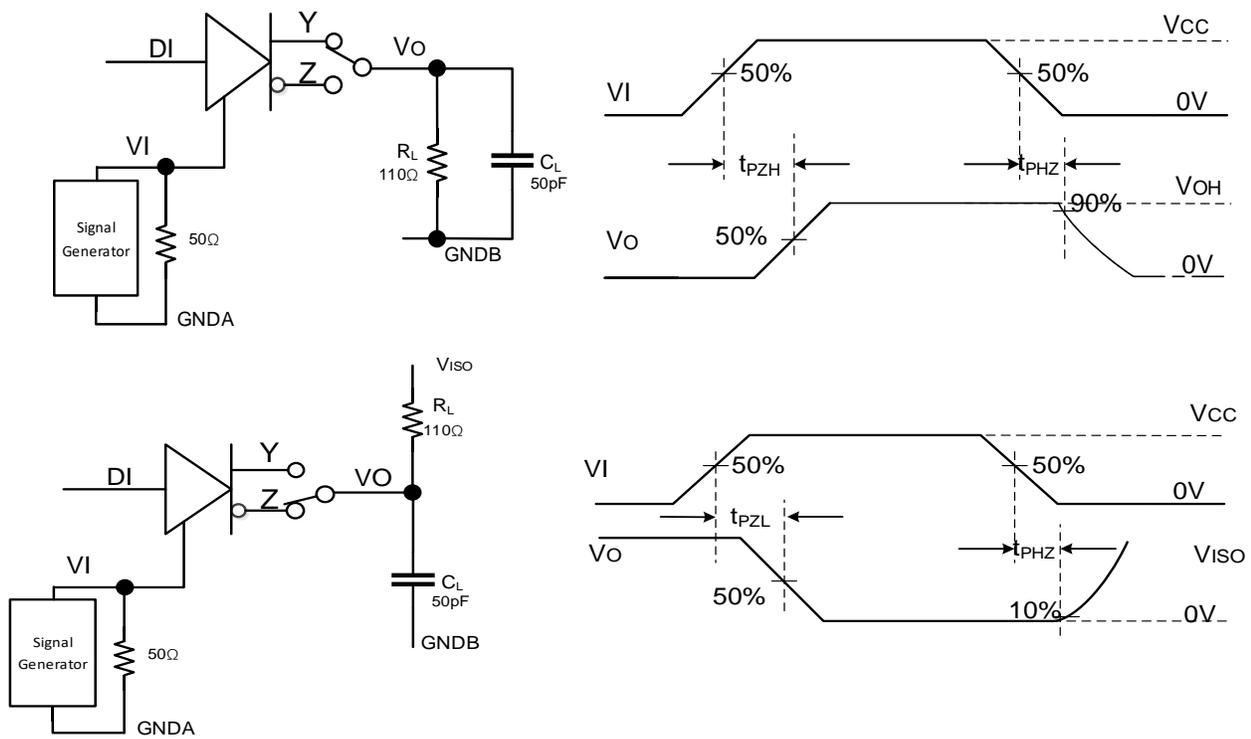


Figure 8-3. Driver Enable and Disable Times

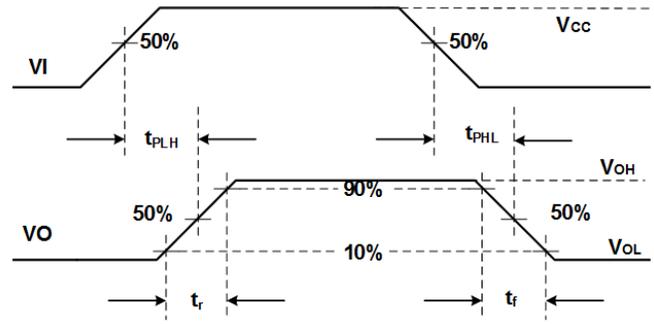
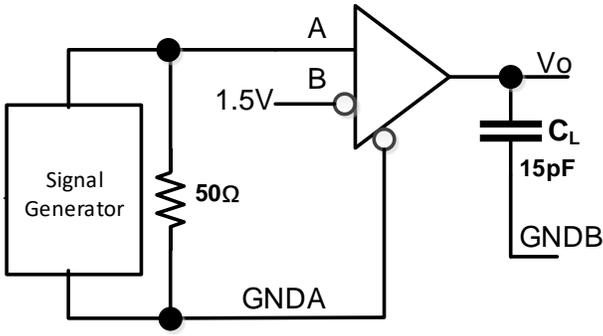


Figure 8-4. Receiver Propagation Delays

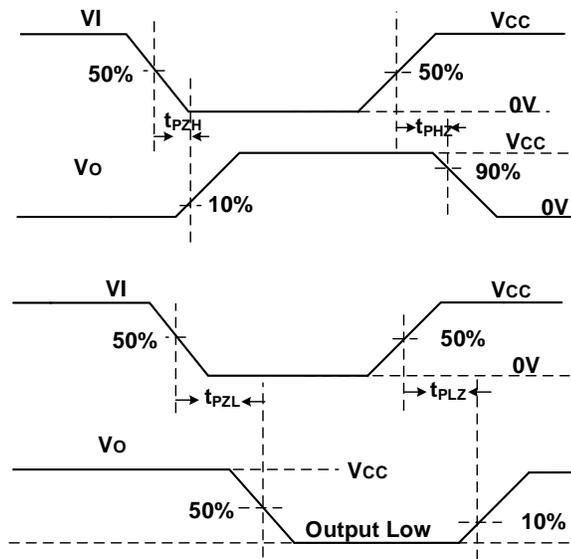
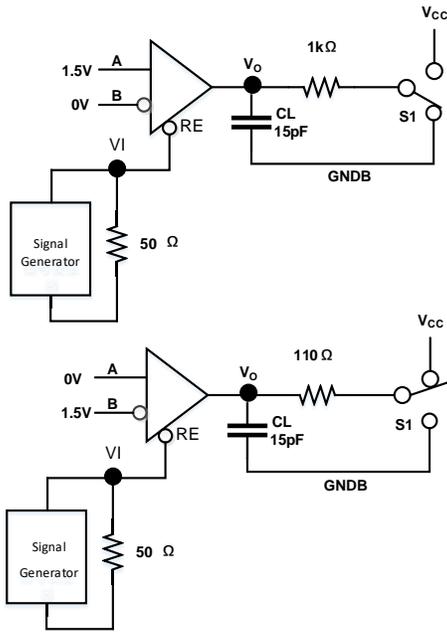


Figure 8-5. Receiver Enable and Disable Times

**Notes:**

1.  $R_L = 110 \Omega$  for RS422,  $R_L = 54 \Omega$  for RS-485
2.  $C_L$  includes external circuit (fixture and instrumentation etc.) capacitance.

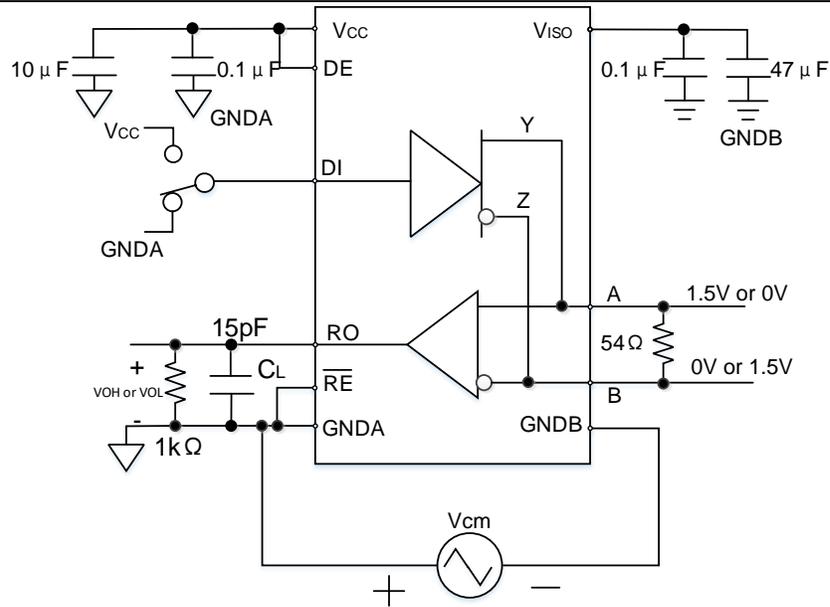


Figure 8-6. Common Mode Transient Immunity (CMTI) Test for the Half-duplex

**9. Detailed Description**

The CA-IS2092 isolated half-duplex RS-485/RS-422 transceivers provide up to 2.5kV<sub>RMS</sub> of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to 150kV/μs common mode transient immunity, allow up to 0.5Mbps communication across an isolation barrier. Power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side circuit. These devices do not require any external components other than bypass capacitors and bus termination resistors to realize an isolated RS-485/RS-422 port. Robust isolation coupled with extended ESD protection and increased speed enables efficient communication in noisy environments, making them ideal for long distance transmission and multi-drop communication in a wide range of applications such as motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs etc. systems. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state.

**9.1. Logic Input**

The CA-IS2092x devices include three logic inputs on the logic side: receiver enable, driver enable and driver digital input. The driver enable control DE pin has an internal weak pull-down to GNDA, while the digital input DI and receiver enable pins have an internal pull-up to V<sub>CC</sub>/V<sub>CCL</sub>, see Figure 9-1 the input equivalent circuit.

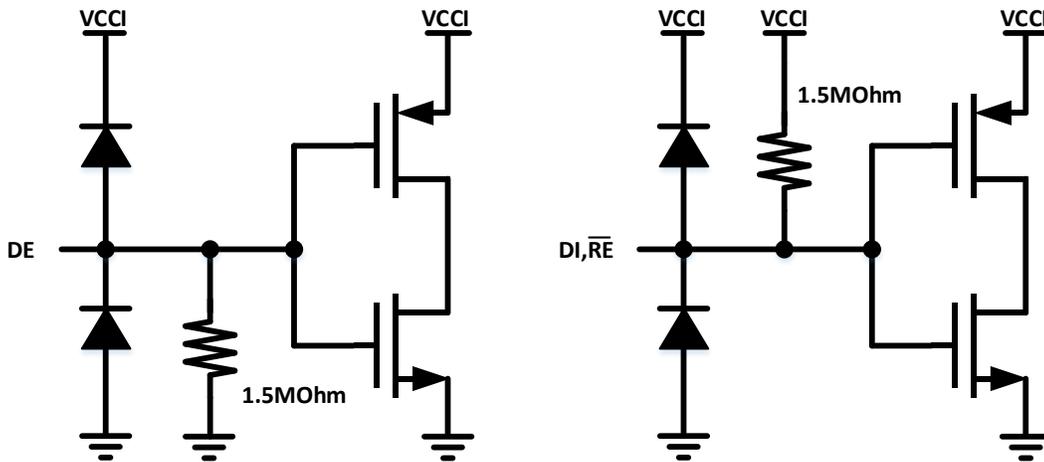


Figure 9-1. Input equivalent circuit

**9.2. Fail-Safe Receiver**

The receiver reads the differential input from the bus line (A and B) and transfers this data as a single-ended, logic-level output RO to the controller. Driving the enable input  $\overline{RE}$  low to enable the receiver. Driving  $\overline{RE}$  logic high to disable the receiver. RO is high impedance when  $\overline{RE}$  is logic high. The  $\overline{RE}$  pin has an internal pull-up resistor to V<sub>CC</sub> for CA-IS2092W or V<sub>CCL</sub> for CA-IS2092VW.

The CA-IS2092x family of RS-485/RS-422 transceivers do not require external fail-safe bias resistors because a true fail-safe feature is integrated into the devices. In true fail-safe, the receiver’s positive-going input threshold is V<sub>IT+(IN)</sub> (-110mV, typ. and -50mV, max.), if the differential receiver input voltage of V<sub>A</sub>-V<sub>B</sub> is greater than or equal to V<sub>IT+(IN)</sub>, RO is logic high when  $\overline{RE}$  is low; RO is logic low when V<sub>A</sub>-V<sub>B</sub> is less than or equal to V<sub>IT-(IN)</sub> in case the receiver is enabled; thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, see Table 9-1 the receiver truth table. Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1. Receiver Truth Table

DIFFERENTIAL INPUT: $V_{ID} = (V_A - V_B)$	ENABLE ( $\overline{RE}$ )	OUTPUT (RO)
$V_{IT+(IN)} \leq V_{ID}$	L	H
$V_{IT-(IN)} < V_{ID} < V_{IT+(IN)}$	L	Indeterminate
$V_{ID} \leq V_{IT-(IN)}$	L	L
X	H	Hi-Z
Open/Short/Idle	L	H
X	Open	Hi-Z
<b>Notes:</b>		
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.		
2. $\overline{RE}$ has an internal weak pull-up to $V_{CC}$ .		

### 9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs on the bus lines A and B. The truth table for the transmitter is provided in Table 9-2, the driver enable control DE pin has an internal weak pull-down to GNDA, see Figure 9-1 the input equivalent circuit; while the digital input DI pin has an internal pull-up to  $V_{CC}$  for CA-IS2092W or  $V_{CCL}$  for CA-IS2092VW. The driver outputs and receiver inputs on the bus side are protected from  $\pm 20kV$  electrostatic discharge (ESD) to GNDB, as specified by the Human Body Model (HBM). The driver outputs also feature short-circuit protection and thermal shutdown.

Table 9-2. Transmitter Truth Table

T <sub>x</sub> INPUT	ENABLE INPUT	OUTPUT	
(DI)	(DE)	A	B
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z
X	OPEN	Hi-Z	Hi-Z
OPEN	H	H	L
<b>Notes:</b>			
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.			
2. DE pin has an internal weak pull-down to GNDA, and DI pin has an internal pull-up to $V_{CC}/V_{CCL}$ .			

### 9.4. Protection Functions

#### 9.4.1. Signal Isolation and Power Isolation

The CA-IS2092x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. Also, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side.

#### 9.4.2. Undervoltage Lockout

Both CA-IS2092V and CA-IS2092VW have undervoltage detection on  $V_{CC}$  supply terminal, the CA-IS2092VW also features undervoltage detection on  $V_{CCL}$  supply terminal, that place the device in protected mode during an undervoltage event on  $V_{CCL}$  or/and  $V_{CC}$ , see Table 9-3 and Table 9-4. Once the undervoltage condition is cleared and the supply voltage has returned to a valid level, the devices transition to normal mode. The host controller should not attempt to send or receive messages until the device enters normal operation.

**Table 9-3. CA-IS2092W Undervoltage Lockout**

V <sub>CC</sub>	DEVICE STATE	BUS OUTPUT	RXD
> V <sub>CC(UVLO+)</sub>	Normal	Per TXD	Mirrors Bus
< V <sub>CC(UVLO-)</sub>	Protected mode	High Impedance	High Impedance

**Table 9-4. CA-IS2092VW Undervoltage Lockout**

V <sub>CC</sub>	V <sub>CCL</sub>	DEVICE STATE	BUS OUTPUT	RXD
> V <sub>CC(UVLO+)</sub>	> V <sub>CCL(UVLO+)</sub>	Normal	Per TXD	Mirrors Bus
< V <sub>CC(UVLO-)</sub>	> V <sub>CCL(UVLO+)</sub>	Protected mode	High Impedance	High Impedance
> V <sub>CC(UVLO+)</sub>	< V <sub>CCL(UVLO-)</sub>	Protected mode	High Impedance	High Impedance
< V <sub>CC(UVLO-)</sub>	< V <sub>CCL(UVLO-)</sub>	Protected mode	High Impedance	High Impedance

### 9.4.3. Thermal Shutdown

If the junction temperature of the CA-IS2092x device exceeds the thermal shutdown threshold  $T_{J(\text{shutdown})}$  (180°C, typ.), the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device (160°C, typ.).

### 9.4.4. Current-Limit

The CA-IS2092x protect the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to 12V by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit fault. The transmitter returns to normal operation once the short is removed.

### 9.5. Isolated Supply Output

The integrated DC-DC converter provide up to 650mW of isolated power with +3.3V or +5V fixed output voltage configurations. , depending on the SEL pin status, see Table 9-5 for the supply configurations of CA-IS2092x devices. Get the SEL pin fixed (connect to V<sub>ISO</sub> or GNDB) before power on the transceivers.

**Table 9-5. Supply Configuration**

SEL INPUT	V <sub>CC</sub>	V <sub>ISO</sub>
Shorted to V <sub>ISO</sub>	5 V	5V
Shorted to GNDB or floating	5 V	3.3V
Shorted to GNDB or floating	3.3 V <sup>1</sup>	3.3V <sup>2</sup>

**Notes:**

1. V<sub>DD</sub> = 3.3 V, SEL shorted to V<sub>ISO</sub> (essentially V<sub>ISO</sub> = 5 V) is not recommended.
2. The SEL pin has a weak pull-down internally. However, for V<sub>ISO</sub> = 3.3 V, the SEL pin should be connected to the GNDB externally, especially in the noisy system.

The maximum output current from V<sub>ISO</sub> is shown as Table 9-6. Note that the I<sub>ISO</sub> value in Table 9-6 is the maximum output current at +25°C with data rate x load capacitance < 0.5Mbps x 2nF. As the increase of temperature, especially when the temperature exceeds +85°C, the maximum load current will be decreased, see more details in 错误!未找到引用源。 , 错误!未找到引用源。 , and 错误!未找到引用源。 .

Table 9-6. Maximum Output Current of  $V_{ISO}$  @  $T_A = 25^\circ C$

Supply voltage $V_{CC}$ (V)	$V_{ISO}$ (V)	$R_L$ ( $\Omega$ ) between CANH and CANL	$I_{ISO}$ (mA)
4.5~5.5	5	NC <sup>1</sup>	130
4.5~5.5	3.3		130
3.15~3.6	3.3		75
4.5~5.5	5	100	80
4.5~5.5	3.3		105
3.15~3.6	3.3		40
4.5~5.5	5	54	55
4.5~5.5	3.3		85
3.15~3.6	3.3		30

**Note:**

1. NC means no-load connection between CANH and CANL.

## 10. Applications Information

### 10.1. Overview

The CA-IS2092 family of half-duplex RS-485/RS-422 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Because of high peak currents flowing through  $V_{CC}$  and  $V_{ISO}$  supplies, bulk capacitance of typical  $10\mu F$  (or at least  $4.7\mu F$ ) is recommended on both pins. Higher values of bulk capacitors are helpful to reduce noise and ripple further and enhance performance, see Figure 10-1 the typical application circuit. Make sure there is no data transmission during the CA-IS2092X power up.

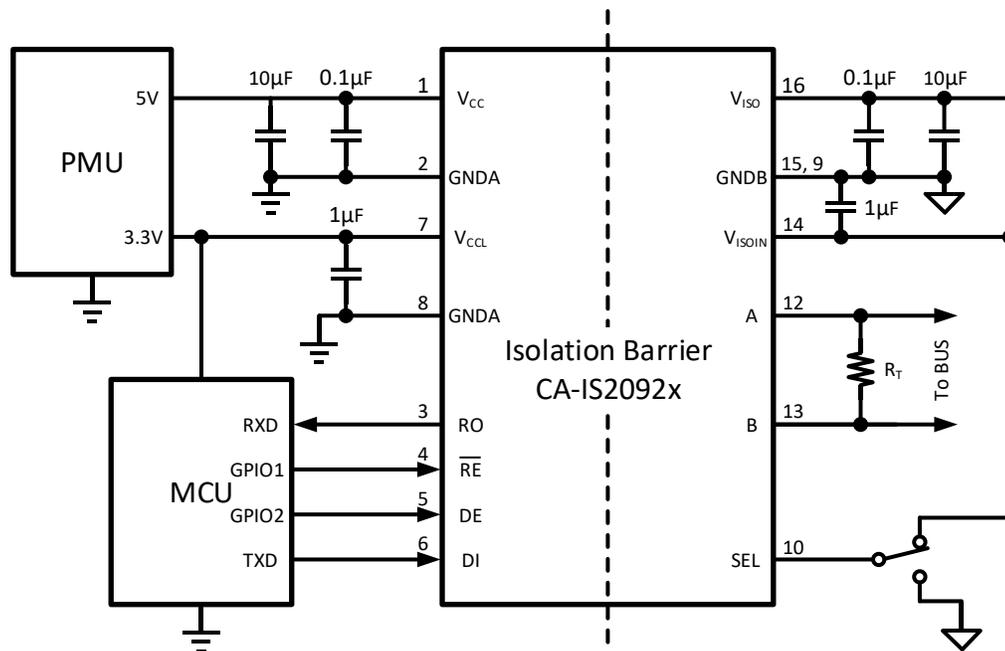


Figure 10-1. Typical application circuit

### 10.2. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, Figure 10-2. The maximum recommended data rate in the RS-485/RS422 network is 10Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original RS-485 standard, new RS-485/RS-422 transceivers and cables are pushing the limit of RS-485 far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor ( $120\Omega$  in the typical application circuits), whose value matches the characteristic impedance( $Z_0$ ) of the cable, and keep stub lengths off the main line as short as possible. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

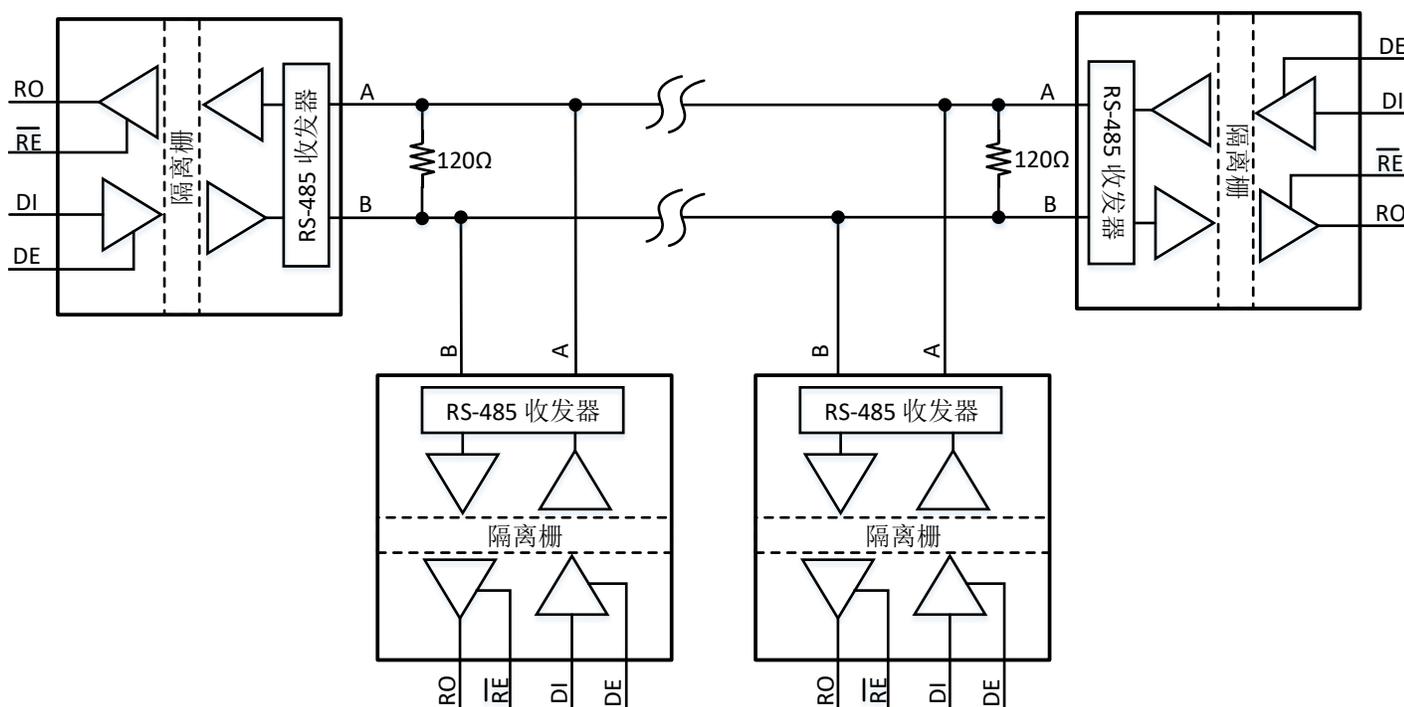


Figure 10-2. Typical isolated half-duple RS-485 application circuit

### 10.3. 256 transceivers on the bus

The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of  $120\Omega$  or more, is 32 ( $375\Omega$ ). The CA-IS2092x transceivers have a  $1/8$ -unit load ( $96k\Omega$ ) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line.

### 10.4. PCB Layout

Careful PCB layout is critical to achieve clean and stable communication operation. It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the minimum  $0.1\mu\text{F}/10\mu\text{F}$  decoupling capacitors between  $V_{CC}$  and  $\text{GNDA}$ , between  $V_{ISO}$  and  $\text{GNDB}$  are recommended. For the individual logic supply input  $V_{CCL}$  and  $V_{ISOIN}$ , we recommend to use a  $1\mu\text{F}$  ceramic capacitors with X5R or X7R between  $V_{CCL}$  pin and  $\text{GNDA}$ ,  $V_{ISOIN}$  and  $\text{GNDB}$ . Place the bypass capacitors, and the CA-IS2092x IC on the same PCB layer. Place decoupling capacitors as close as possible to the CA-IS2092x device pins, see Figure 10-3 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths.

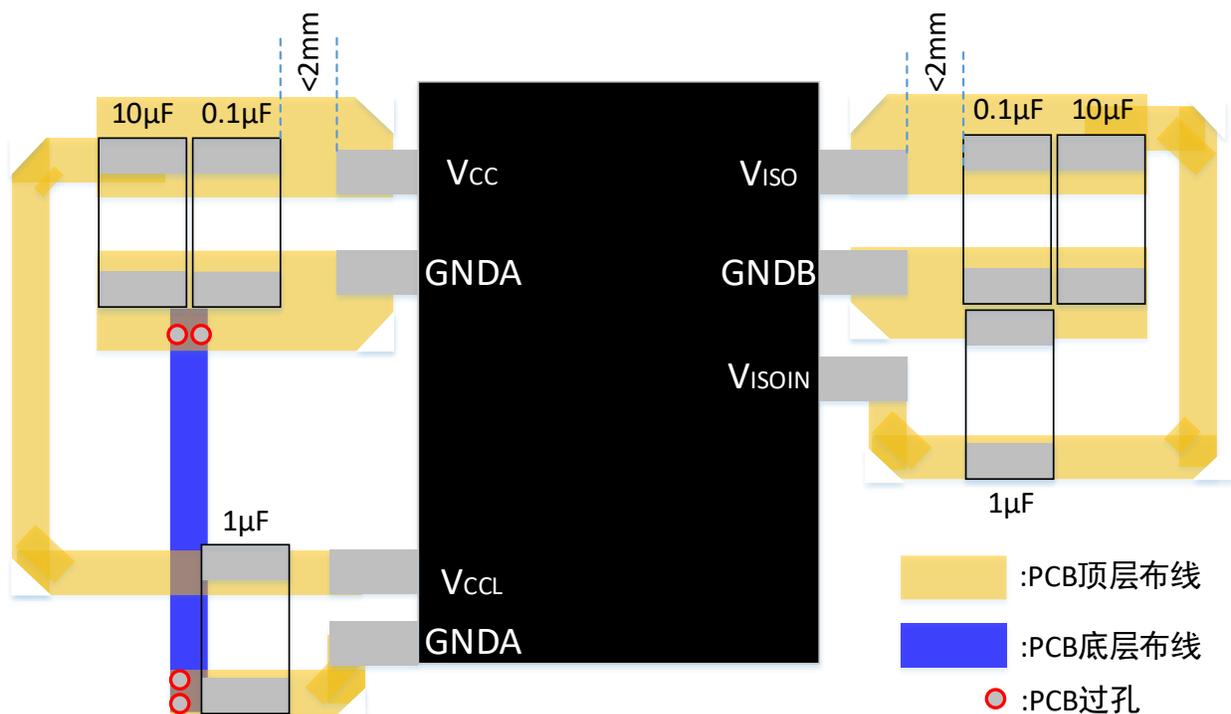
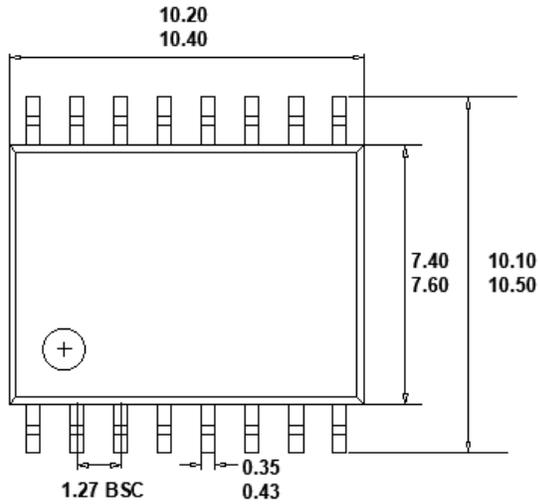


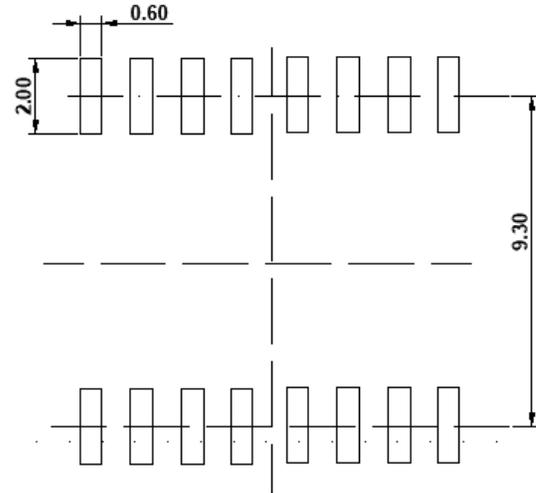
Figure 10-3. Recommended PCB Layout

**11. Package Information**

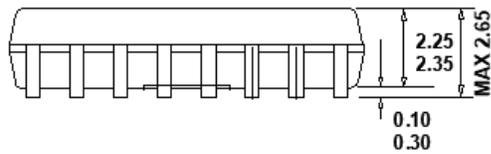
**16-Pin Wide Body SOIC Package Outline**



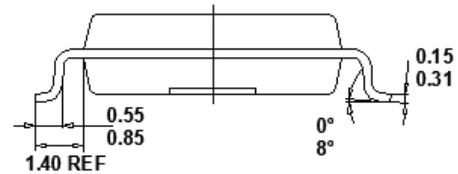
**TOP VIEW**



**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**LEFT SIDE VIEW**

**Note:**

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

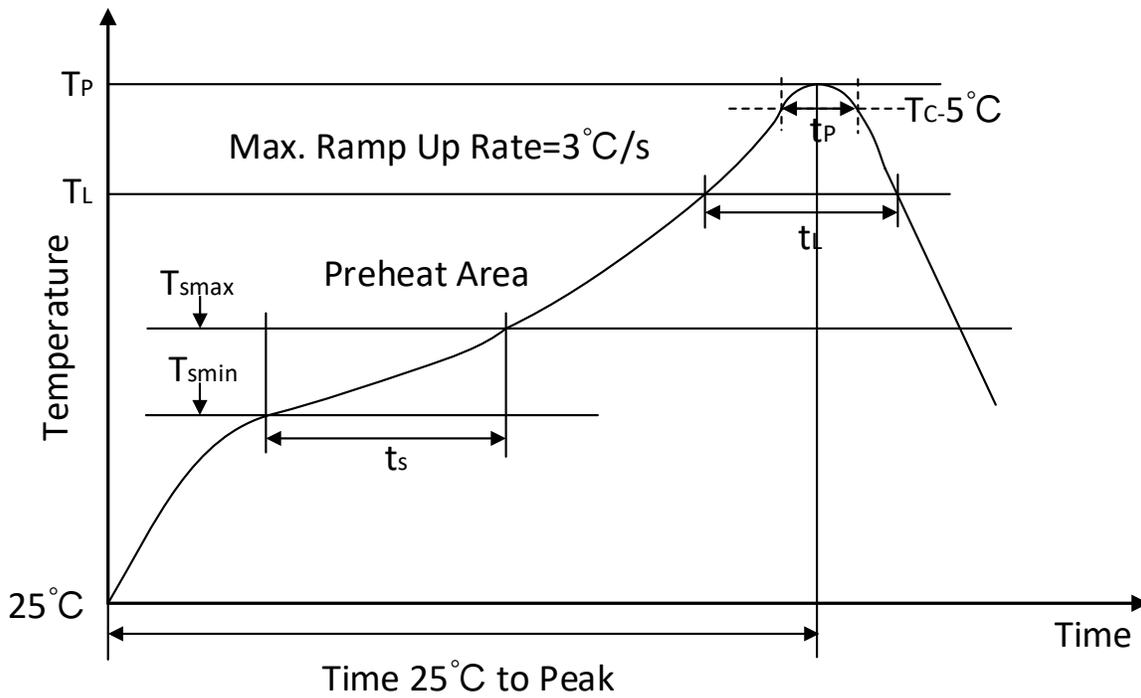
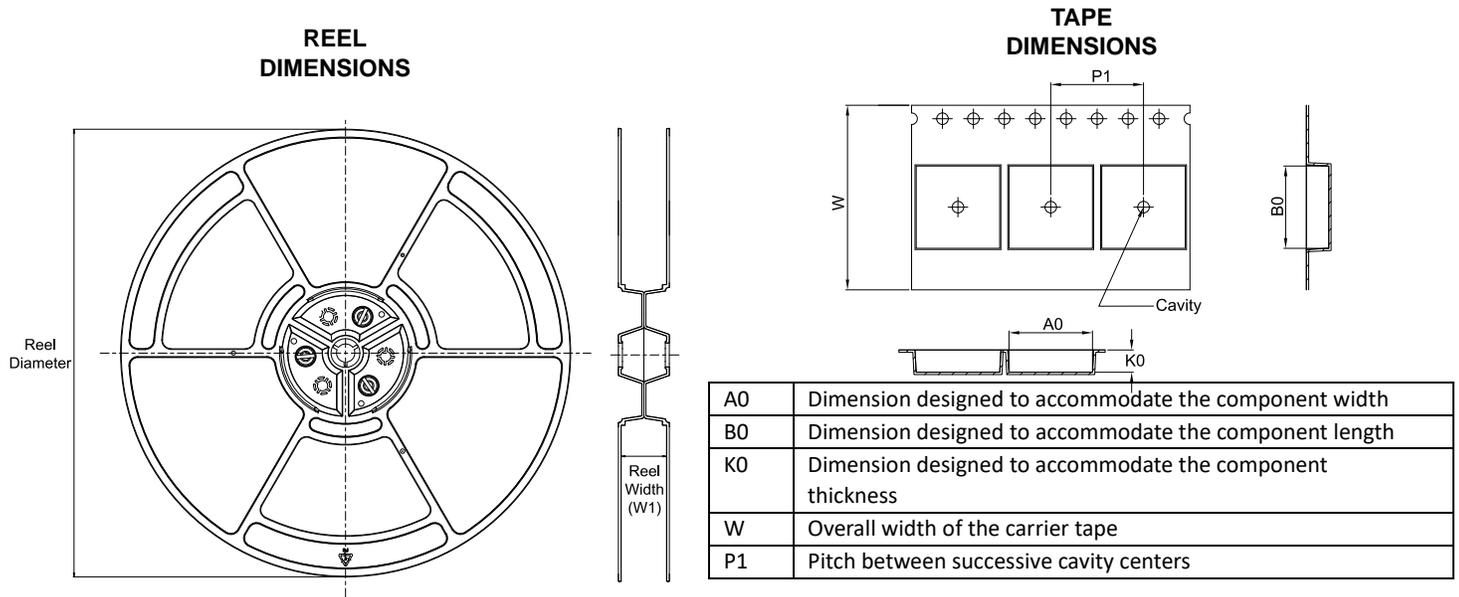


Figure. 12-1 Soldering Temperature (reflow) Profile

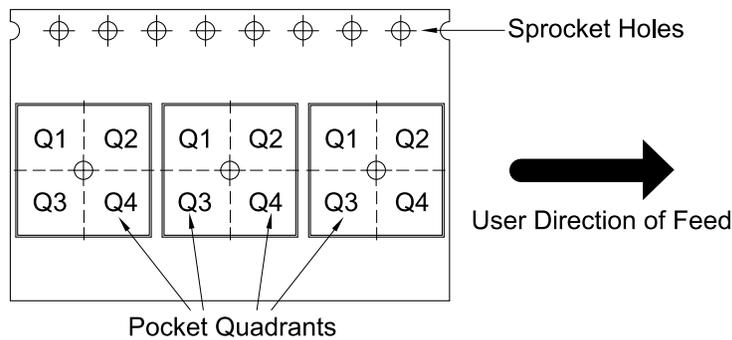
Table. 12-1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 °C to Peak)	3°C /second max
Time of Preheat temp(from 150 °C to 200 °C )	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25 °C to peak temp	8 minutes max

### 13. Tape And Reel Information



#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2092W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS2092VW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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