OMMIC Innovating with III-V's

PRELIMINARY DATASHEET

CGY2128UH/C1

24-34 GHz Ka-band Low Noise Amplifier

DESCRIPTION

The CGY2128UH/C1 is a high performance Ka band Low Noise Amplifier. This device is a key component for high frequencies (25-31 GHz) systems.

The CGY2128UH/C1 is a three stage Low Noise Amplifier with a low power consumption (Vdd=3.5V, total Drain current = 45mA).

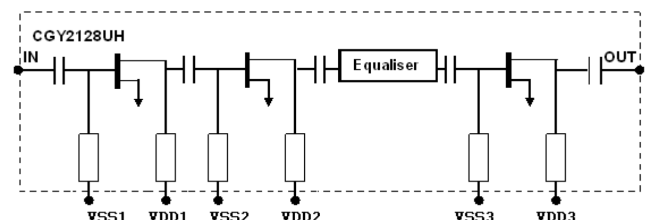
The MMIC is manufactured using OMMIC's proprietary 0.13 µm MHEMT D01MH technology.

FEATURES

- Suitable for Ka band applications
- Wide frequency range : 24 – 34 GHz
- 24 dB small signal gain
- Low power consumption (157mW)
- Mid-band NF= 1.3 dB at 29GHz
- Output P1dB = 11dBm at 29GHz
- Chip size = 2640 x 2000 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Space and MIL-STD Available

APPLICATIONS

- Ka band applications
- Instrumentation
- General purpose amplifier
- Ka-band communications



Block Diagram of the CGY2128UH Low Noise Ampliifier

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LIMITING VALUES

Tamb = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}, V_{DD3}	Drain voltage		0	5	V
I_D total	Total Drain current			55	mA
V_{SS1}, V_{SS2}, V_{SS3}	Gate supply voltage	V_{DD} open-circuited	-2	0.6	V
T_{stg}	Storage temperature		-55	+150	° C
T_j	Junction temperature			+150	° C
T_{amb}	Ambient temperature		-40	+85	° C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th(j-a)}$	Thermal resistance from junction to ambient (T_a = 25 °C)	TBD	° C/W

DC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}, V_{DD3}	Drain voltage			3.5	+ 4.5	V
I_{D1}	Stage 1 drain current			8		mA
I_{D2}	Stage 2 drain current			14		mA
I_{D3}	Stage 3 drain current			25		mA
V_{SS1}, V_{SS2}, V_{SS3}	Gates supply voltages		-1.5	0.0	0.5	V

NOTE

V_{SS1} determines the typical drain current I_{DD1}, V_{SS2} determines the typical drain current I_{DD2}, V_{SS3} determines the typical drain current I_{DD3}.

RF CHARACTERISTICS

T_{amb} = 25 °C, V_{DD1}= V_{DD2}= V_{DD3} =3.5V, I_{D1} = 8 mA, I_{D2} = 14mA, I_{D3} = 26mA.
The specifications mentioned below are measured on-wafer, using 50 Ω RF probes unless stated otherwise.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
BW	Useful bandwith		24		34	GHz
Gain	Reference Gain	F = 28 GHz		24.5		dB
S11	Input return loss	F = 28GHz		-16	-10	dB
S22	Output return loss	F = 28GHz		-17	-10	dB
S12	Isolation	F = 28GHz		-48		dB
NF	Noise Figure	F = 28GHz		1.3		dB
P1dB	Output 1dB compression point	F = 28GHz		11		dBm
OIP3	Output third intercept point	With two carriers F1=27.95GHz, F2=28.05GHz		21		dBm
K	Microwave stability factor. T_{amb} = -40˚C to +85˚C	F = 0.1 MHz to 50 GHz	1.1			

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

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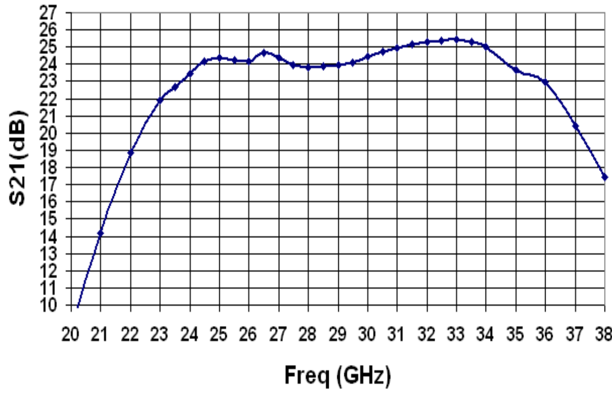
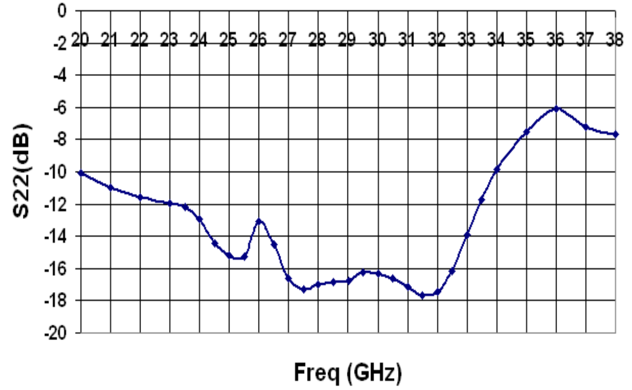
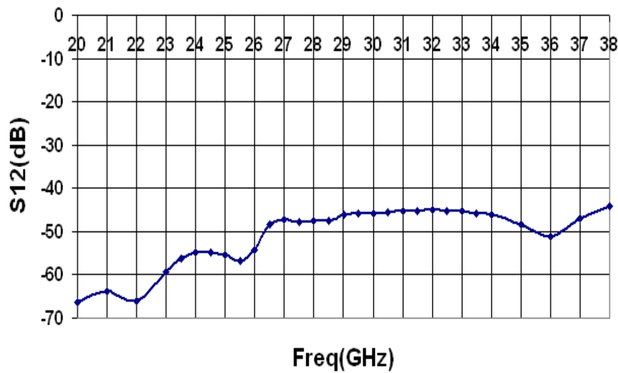
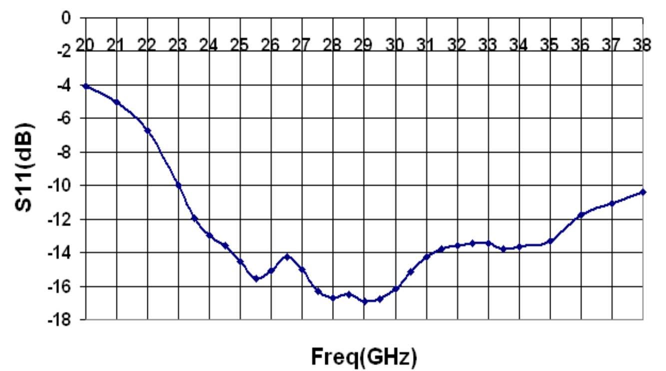
MEASURED PERFORMANCE

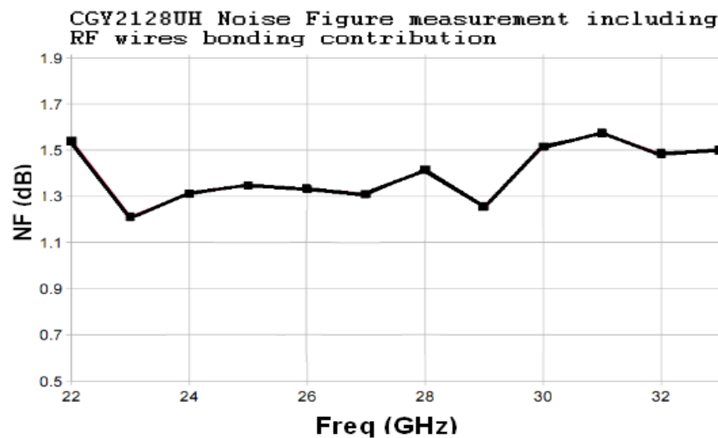
T_{amb} = 25 °C, V_{DD1} =V_{DD2} = V_{DD3} = 3.5V, on wafer.











CGY2128UH/C1 TYPICAL SCATTERING PARAMETERS

T_{amb} = 25 °C, V_{DD1}= V_{DD2}= V_{DD3} =3.5V, I_{D1} = 8 mA, I_{D2} = 14mA, I_{D3} = 26mA.

Freq (GHz)	S11(dB)	Ang S11 (°)	S12(dB)	Ang S12 (°)	S21(dB)	Ang S21 (°)	S22(dB)	Ang S22 (°)
20.0	-4.1	43.7	-66.5	53.7	8.6	-174.6	-10.1	141.3
21.0	-5.0	17.8	-63.8	19.4	14.2	147.2	-10.9	122.1
22.0	-6.7	-14.0	-66.1	-17.1	18.8	101.4	-11.6	100.9
23.0	-10.0	-47.2	-59.3	-76.7	21.9	49.5	-12.0	76.3
23.5	-12.0	-58.5	-56.2	-109.7	22.7	25.0	-12.2	60.4
24.0	-12.9	-68.1	-54.7	-140.2	23.5	2.7	-12.9	43.0
24.5	-13.6	-82.3	-54.9	-167.1	24.2	-21.5	-14.4	30.1
25.0	-14.5	-95.6	-55.5	-177.6	24.4	-45.1	-15.2	21.7
25.5	-15.6	-108.2	-56.9	172.3	24.2	-66.9	-15.3	17.0
26.0	-15.1	-113.4	-54.1	-149.5	24.2	-83.3	-13.1	2.8
26.5	-14.3	-133.7	-48.4	-179.9	24.7	-104.7	-14.5	-27.4
27.0	-15.0	-149.5	-47.3	157.1	24.4	-124.9	-16.6	-37.7
27.5	-16.3	-158.9	-47.7	138.2	24.0	-142.4	-17.3	-40.7
28.0	-16.7	-164.6	-47.6	128.3	23.8	-158.0	-17.0	-46.8
28.5	-16.5	-169.3	-47.4	122.1	23.9	-173.5	-16.8	-55.7
29.0	-16.9	-173.8	-46.1	112.9	23.9	171.4	-16.8	-63.8
29.5	-16.8	-173.8	-45.9	97.9	24.1	156.8	-16.2	-74.0
30.0	-16.2	-178.8	-45.9	93.5	24.4	141.4	-16.3	-85.0
30.5	-15.2	175.6	-45.6	84.0	24.7	124.6	-16.6	-93.3
31.0	-14.2	168.7	-45.4	75.6	25.0	107.4	-17.1	-99.0
31.5	-13.8	159.1	-45.1	65.2	25.2	89.5	-17.6	-99.5
32.0	-13.6	147.7	-44.9	59.1	25.3	70.9	-17.5	-95.7
32.5	-13.4	135.0	-45.2	49.2	25.4	52.7	-16.1	-90.5
33.0	-13.4	123.2	-45.3	40.1	25.4	34.5	-13.9	-90.7
33.5	-13.8	110.1	-45.8	34.4	25.3	15.3	-11.8	-97.2
34.0	-13.7	95.2	-46.2	23.1	25.0	-5.0	-9.8	-108.1
35.0	-13.3	56.6	-48.3	-4.0	23.7	-43.2	-7.6	-133.8
36.0	-11.7	8.9	-51.3	80.7	23.0	-81.5	-6.1	-163.9
37.0	-11.0	-38.6	-46.9	49.5	20.4	-120.9	-7.2	175.6
38.0	-10.4	-71.0	-44.1	46.9	17.5	-155.8	-7.7	163.5

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APPLICATION INFORMATION

Typical application scheme

A reference module layout is proposed in figure 1. In this figure 1, RF input and output microstrip transmission lines are used, but coplanar transmission lines with similar performance may also be used. All path lengths and physical sizes of the components should be minimized.

All RF input and output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as small as possible to reduce parasitic inductance. Higher RF input / output inductance may result in a degradation of gain and match. Ribbon bonding technique can also be used.

All others bonding inductances (pads V_{D1}, V_{D2}, V_{D3} and V_{ss1}, V_{ss2}, V_{ss3}) should be kept as short as possible.

Decoupling 47 pF chip capacitors (close to the chip) and 100 nF SMD* capacitors (positioned at around 4mm from the chip) are used to improve the power supply rejection.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn or silver conductive epoxy material can be used for die attachment.

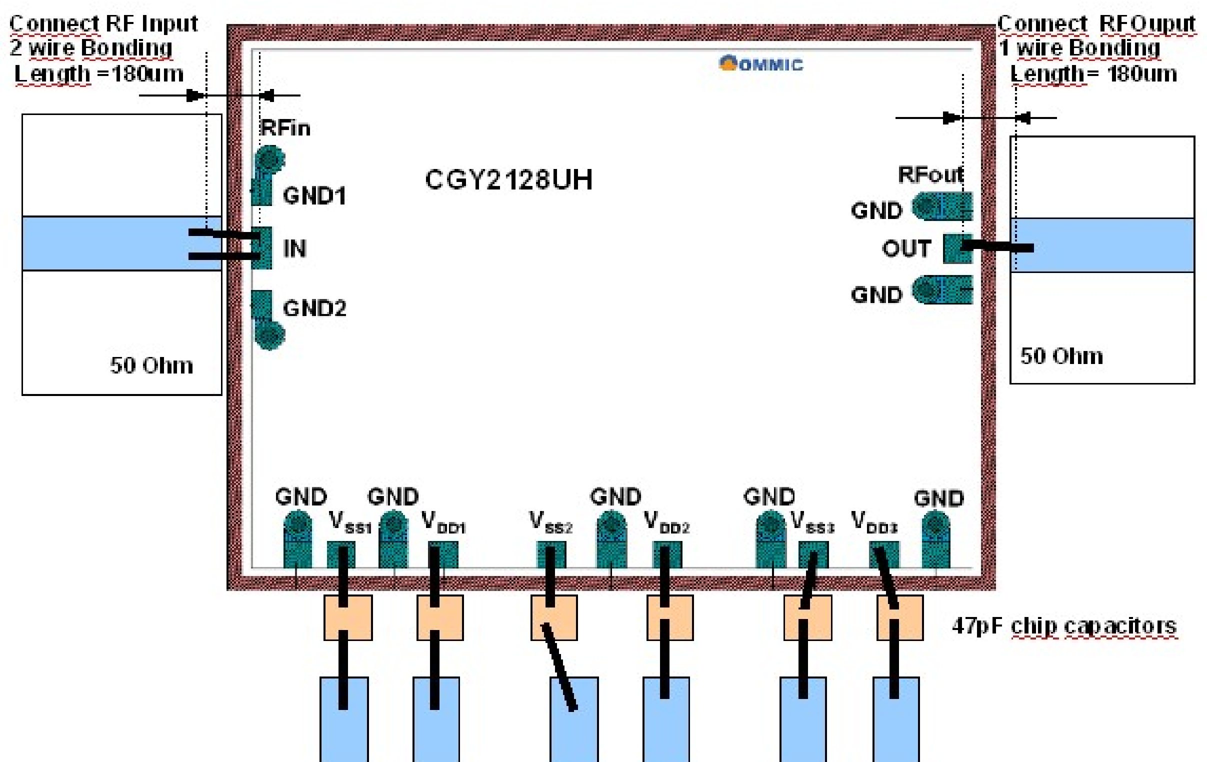

Figure 1: *CGY2128UH/C1 module layout : Microstrip assembly*

*Surface Mount Devices

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OPERATING AND HANDLING INSTRUCTIONS

The CGY2128UH/C1 is a very high performance MHEMT device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

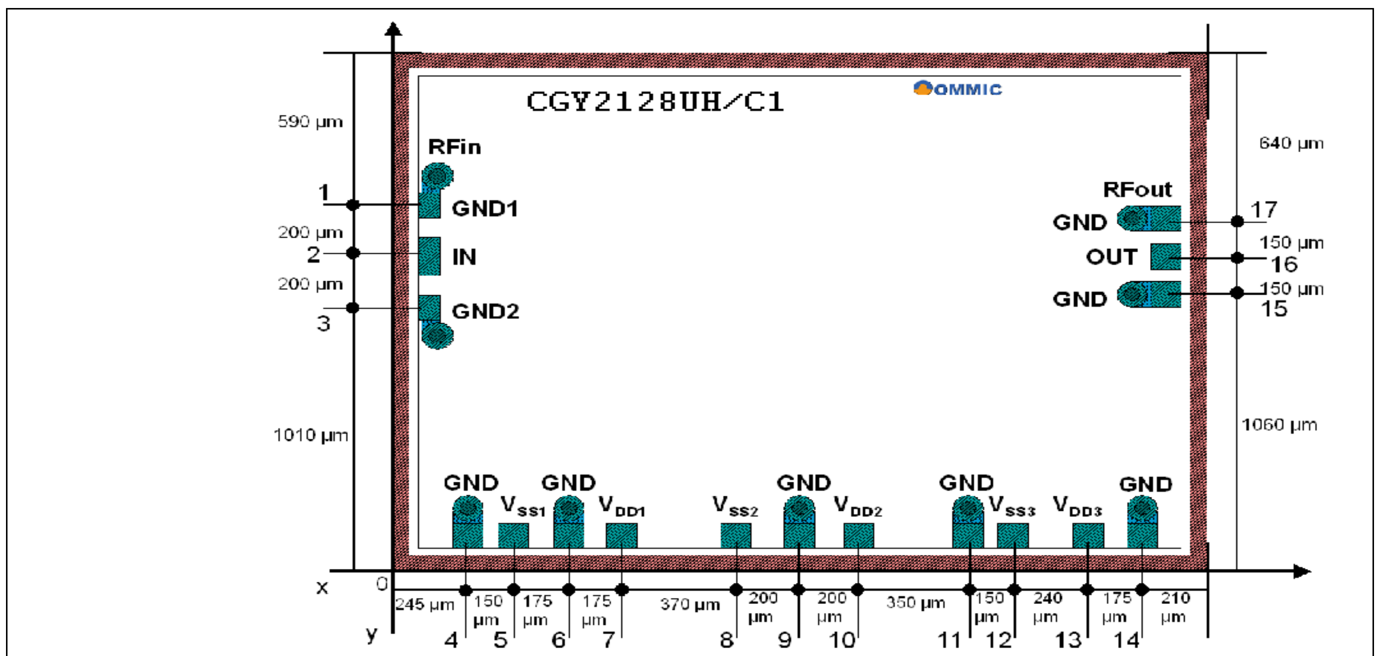
The following power supply sequence is recommended.

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting V_{ss1}, V_{ss2}, V_{ss3} to –1 V.
c) Increase V_{DD1} ,V_{DD2} and V_{DD3} to 3.5V
d) Increase the gate voltages V_{SS1}, V_{SS2} and V_{SS3} slowly from –1 V until the three drains current stages reaches respectively to 8mA, 13mA and 25mA.
e) Apply the RF input signal.

2- Mounting and ESD handling precautions

For high performance Integrated Circuits, such as the CGY2128UH/C1, care must be taken when mounting GaAs MMICs so as to correctly mount, bond and subsequently seal the packages and hence obtain the most reliable long-term operation. The temperature, duration, material and sealing techniques compatible with GaAs MMICs and the precautions to be taken are described in OMMIC's document "OM-CI-MV/001/PG", entitled, "Precautions for III-V users".

PAD CONFIGURATION



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PAD POSITION

SYMBOL	PAD	COORDINATES (1)		DESCRIPTION
		Y	X	
GND	1	120	1412	Connected to ground with on-chip via hole
IN	2	120	1212	RF input
GND	3	120	1012	Connected to ground with on-chip via hole
GND	4	130	245	Connected to ground with on-chip via hole
V_{SS1}	5	130	395	Gate supply voltage 1, must be decoupled to ground using external capacitor(s)
GND	6	130	575	Connected to ground with on-chip via hole
V_{DD1}	7	130	745	Drain supply voltage 1, must be decoupled to ground using external capacitor(s)
V_{SS2}	8	130	1115	Gate supply voltage 2, must be decoupled to ground using external capacitor(s)
GND	9	130	1315	Connected to ground with on-chip via hole
V_{DD2}	10	130	1515	Drain supply voltage 2, must be decoupled to ground using external capacitor(s)
GND	11	130	1865	Connected to ground with on-chip via hole
V_{SS3}	12	130	2015	Gate supply voltage 3, must be decoupled to ground using external capacitor(s)
V_{DD3}	10	130	2255	Drain supply voltage 3, must be decoupled to ground using external capacitor(s)
GND	14	130	2430	Connected to ground with on-chip via hole
GND	15	2510	1062	Connected to ground with on-chip via hole
OUT	16	2510	1212	RF Output
GND	17	2510	1062	Connected to ground with on-chip via hole

MECHANICAL INFORMATION

PARAMETER		VALUE
Size		2640 x 2000 µm
Thickness		100 µm
Backside material		TiAu
Passivation		PECVD deposited Si_3N_4
Bonding pad dimensions	GND	100 x 100 µm
	OUT, V_{SS1}, V_{DD1}, V_{SS2}, V_{DD2}, V_{SS3}, V_{DD3}, GND	100 x 100 µm
	IN	150 x 80 µm

NOTE

The die size and all pad positions refer to the mask layout, with (X=0, Y=0) at the bottom left corner of the layout.For each pad, the (X,Y) coordinates refer to the center of the pad.
Wafers are diced by sawing, with a sawline width of 35 µm (± 5 µm). A misalignment of the sawline with the middle of the dicing street (± 20 µm on all sides) may also result in a variation of ± 20 µm of the actual positions of the pads on the diced chip and an additional tolerance of ± 40 µm on the die size.

DEFINITIONS

Limiting values definition

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

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ORDERING INFORMATION

Generic type	Package type	Version	Description
CGY2128UH	Bare Die	C1	24-34 GHz Ka-band Low Noise Amplifier

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