PRELIMINARY DATASHEET

CGY2135UH/C1

18-23 GHz 33dBm Power Amplifier

DESCRIPTION

The CGY2135UH/C1 is a high performance dual line-up 3 stages GaAs Power Amplifier MMIC designed to operate in the K band from 18 to 23 GHz.

The CGY2135UH/C1 has an output power of 31.2 dBm at the 1 dB compression point and operates with a 4 V power supply. The small signal gain is 25.4 dB at 20.5GHz and it exhibits a 20.2% PAE at 1dB compression point. It can be used in Radar, Telecommunication and Instrumentation applications.

The die is manufactured using OMMIC's High Performance 0.13 µm gate length PHEMT Power Technology D01PH. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

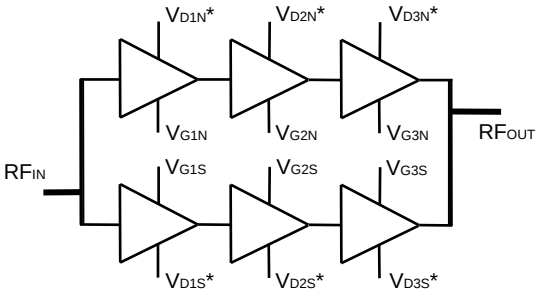
APPLICATIONS

- Radar
- Telecommunications
- Instrumentation

FEATURES

- Operating Range : 18 GHz to 23 GHz
- P_{1dB} : 31.2 dBm @ 20.5GHz
- Psat : 32 .3 dBm @ 20.5GHz
- PAE : 20.2 % @ 20.5Ghz @ P_{1dB}
- Gain : 25.4 dB @ 20.5 GHz
- Power Supply : 4.0 V
- 50 Ohms Input and Output matched
- Input Return Loss : > 12 dB
- Output Return Loss : > 12 dB
- Chip size = 3.65 x 3.14 x 0.1 mm
- Device Availability (Q3 2012):
  - Tested, Inspected Known Good Die (KGD)
  - Demonstration Boards
  - Space and MIL-STD MMICs

V_{D1N}, V_{D2N}, V_{D3N} are available externally but are internally interconnected



V_{D1S}, V_{D2S}, V_{D3S} are available externally but are internally interconnected

CGY2135UH/C1 Power Amplifier Block diagram

RoHS Compliant

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MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{GXN}, V_{GXS} (X = 1..3)	Gate voltage		- 2,5	0	V
V_{DN}, V_{DS}	Drain voltage		0	+ 5.5	V
I_{DN}, I_{DS}	Drain current			750	mA
$I_{GXN, S}$ (all gates)	Gate Current		- 1	+ 1	mA
P_{IN}	RF Input power			+ 20	dBm
T_{amb}	Ambient temperature		- 40	+ 85	°C
T_j	Junction temperature			+ 175	°C
T_{stg}	Storage temperature		- 55	+ 85	°C

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j\ -\ amb)}$	Thermal resistance from junction to ambient (DC power at T_{amb} max)	TBD	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, $I_{DN} = I_{DS}$ = 600mA,

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RFin	Input frequency		18		23	GHz
V_{DN}, V_{DS}	Drain Supply voltage			+ 4.0		V
V_{GXN}, V_{GXS} (X = 1..3)	Gate Supply voltage	$I_{DN} + I_{DS}$ = 1200 mA		-0.39		V
$I_{DN} + I_{DS}$	Total supply current @ Psat			1200		mA
G	Gain	@ 18 GHz @ 20.5GHz @ 23GHz		23.9 25.4 26.6		dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point	@ 18 GHz @ 20.5 GHz @ 23 GHz		+30.5 +31.2 +32.3		dBm
Psat	Saturated power	@ 18 GHz @ 20.5 GHz @ 23 GHz		+31.8 +32.3 +33.1		dBm
PAE	Power Added Efficiency			20.2		%
OIP3	Output third order intercept point			TBD		dBm
IMD3	2 Carriers 3 dB below P1dB			TBD		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT}/RF_{IN}		-40		dB
S_{11}	Input reflection coefficient			12		dB
S_{22}	Output reflection coefficient			12		dB
P_{OFF}	Leakage when HPA off All gates			TBD		dBm

(*) Measurement reference planes are the INPUT and OUTPUT plans of the CGY2135UH/C1 MMIC.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

GAIN CURVE

Conditions : V_{DN} = V_{DS} = 4.0V, V_{GXN} = V_{GXS} = -0.4V (I_{DN} + I_{DS} = 1200mA), T_{amb} = + 25°C (On Wafer measurements)

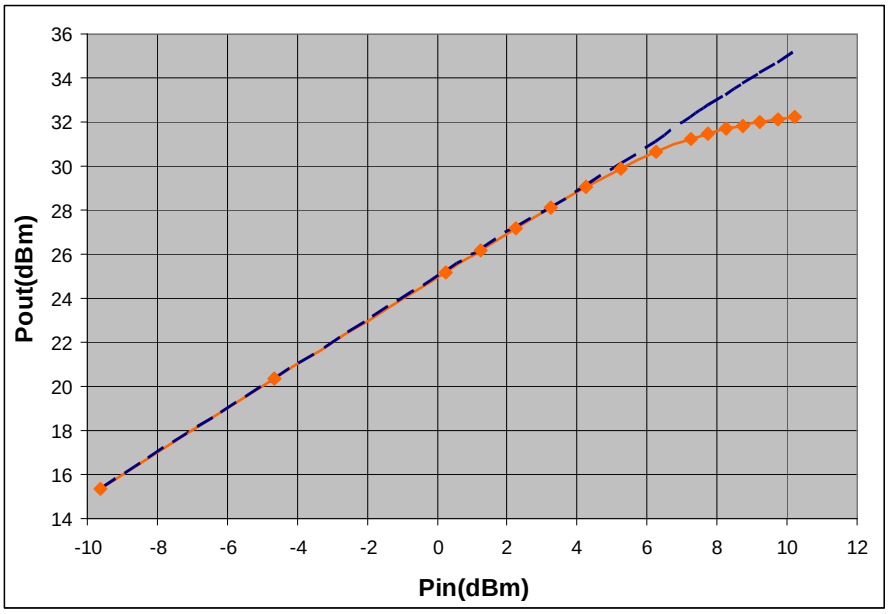

Figure 1 Pout vs Pin @20.5GHz

COMPRESSION AND PAE

Conditions : V_{DN} = V_{DS} = 4.0V, V_{GXN} = V_{GXS} = -0.4V (I_{DN} + I_{DS} = 1200mA), T_{amb} = + 25°C (On Wafer measurements)

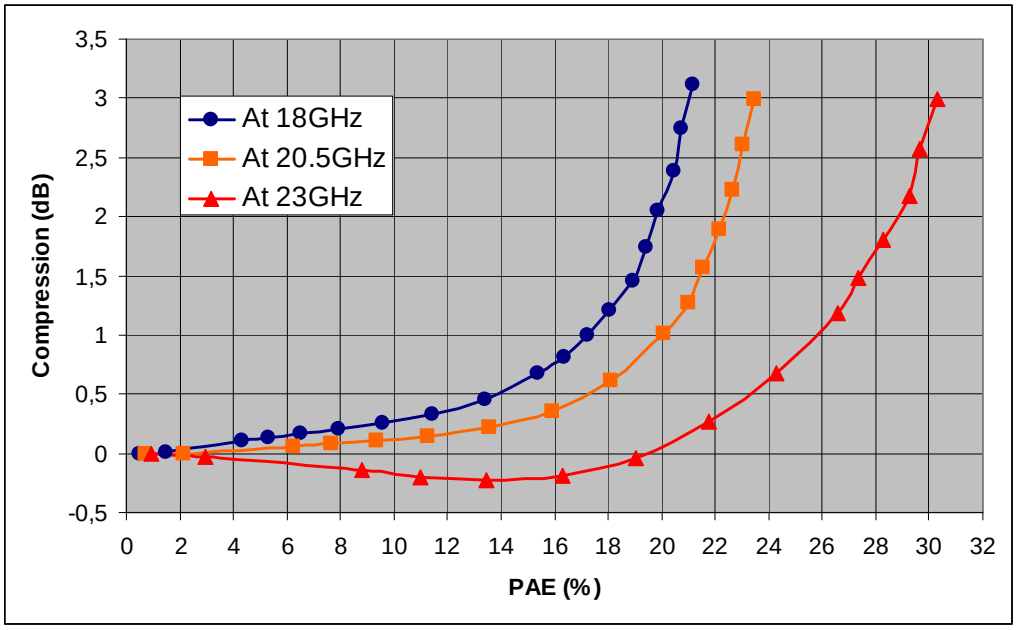

Figure 2 PAE vs compression

APPLICATION SCHEMATIC

To prevent unstability of the customer design it is hightly recommended to place a 47pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionnaly, a 10nF capacitor can be added on a drain connection. In the gate circuitry, a 500 Ω resistor have been added in serie with each gate introducing some low pass filtering in case of fast power switching.

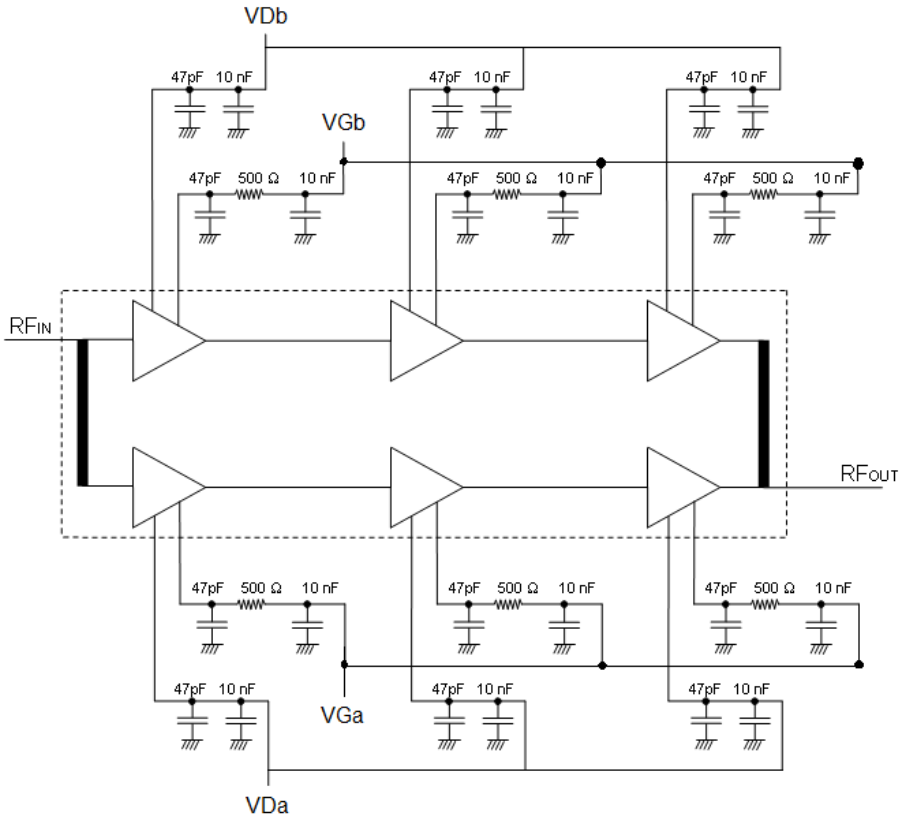

Figure 3 : Application schematics

Component NAME	Value	Type	Comment
All 47pF capacitors	47pF	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die with bonding as short as possible
All 500 Ω resistors	500Ω	Chip Resistor	Chip resistor US MICROWAVES RG1421-500-1% soldered close to the 47pF chip capacitor with bonding as short as possible
All 10nF capacitors	10nF	Chip Capacitor	MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520

Due to the highly symmetrical design of the component and the requirements of the power combiner, it is recommended to keep drain current I_{DN} equal to I_{DS}, for the same reason, it is recommended to keep drain voltage V_{DN} equal the V_{DS}.

In order to validate each stage of the amplifier with respect to the DC, it is recommended to set firstly all gate voltage $V_{GXN, XS}$ to -2.0V, then to set the corresponding drain voltage V_{DN}, V_{DS} to +1V and check that the corresponding drain current I_{DS}, I_{DS} stay at a very low level, after that verification, V_{DN}, V_{DS} can be set to 4V. When $V_{GXN, XS}$ is changed from -2.5 to roughly -0.4V, the corresponding drain current increases slowly in a controlled manner to reach the typical targeted value.

DIE LAYOUT AND PIN CONFIGURATION

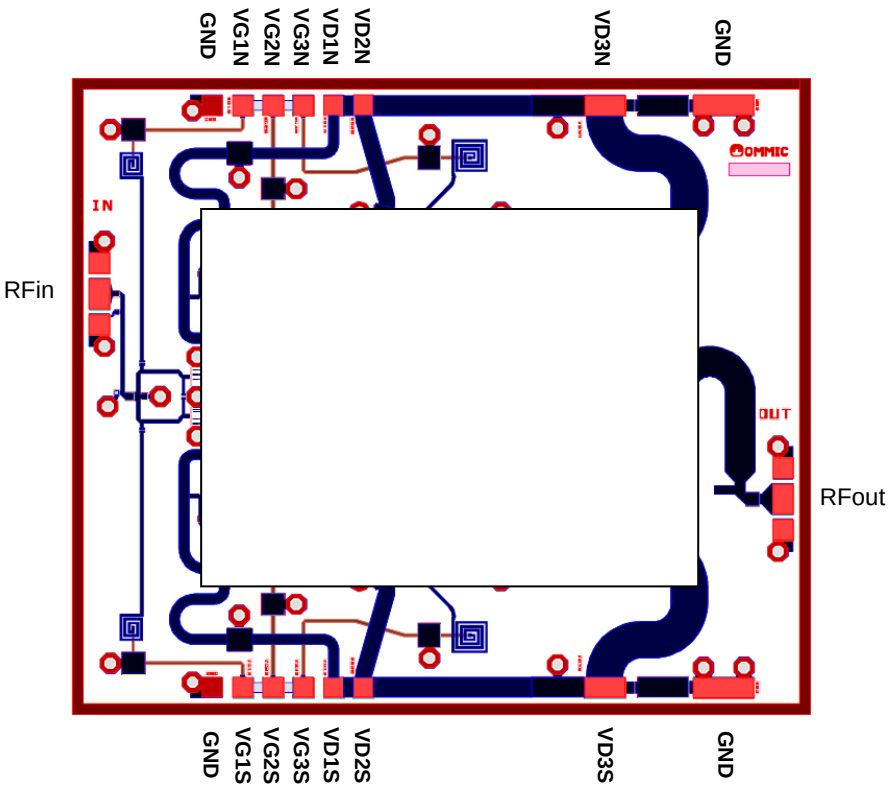

Figure 4 CGY2135UH/C1 pads function

PINOUT

The amplifier has a "NORTH" and a "SOUTH" face, North face is on the top when RF input is on the left and RF output on the right

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD3N	VD3b	Drain 3 supply voltage North
VD2N	VD2b	Drain 2 supply voltage North
VD1N	VD1b	Drain 1 supply voltage North
VG3N	VG3b	Gate 3 supply voltage North
VG2N	VG2b	Gate 2 supply voltage North
VG1N	VG1b	Gate 1 supply voltage North
VD3S	VD3a	Drain 3 supply voltage South
VD2S	VD2a	Drain 2 supply voltage South

VD1S	VD1a	Drain 1 supply voltage South
VG3S	VG3a	Gate 3 supply voltage South
VG2S	VG2a	Gate 2 supply voltage South
VG1S	VG1a	Gate 1 supply voltage South
GND	GND	Ground

Note :

In order to ensure good RF performances and stability It is key to connected to the ground the pad available on the backside of the die.

BONDINGS PAD COORDINATES

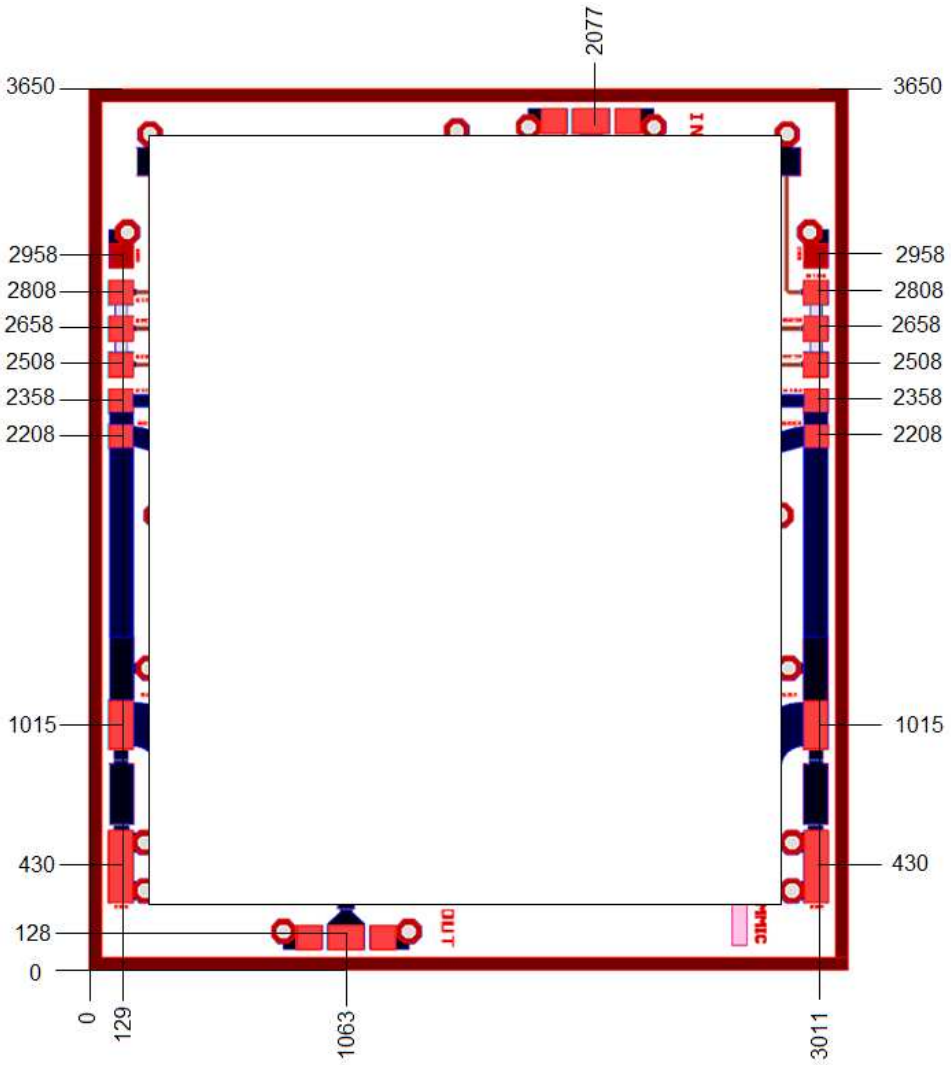

Figure 5 Bondings pad coordinates

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on-wafer tested	32	-	3.65 x 3.14 x 0.1

SOLDERING

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330°C.
Temperature in excess of 300°C should not be applie d to the die longer than 1mn
Toxic fumes will be generated at temperatures higher than 400°C

ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2135	UH	C1	-	On-Wafer measured Die

RoHS Compliant

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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