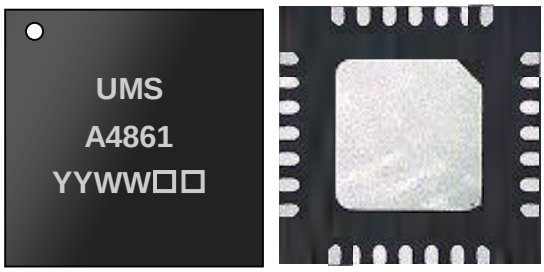
6-11 GHz Variable Gain Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

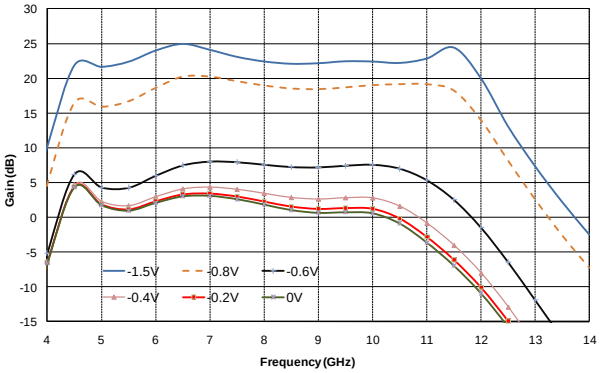
The CHA4861-QGG is a variable gain broadband four stage monolithic amplifier.
It is designed for a wide range of applications, typically commercial communication systems.
The circuit is manufactured with a power pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 6-11GHz
- 23dB gain
- 29dBm Output IP3
- 20dB Gain control range
- DC bias: Vd=4.5V @ Id=160mA
- 28L-QFN5x5

Linear gain versus gain control



Main Electrical Characteristics

Tamb.= +25°C, Vd = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		11	GHz
Gain	Linear Gain		23		dB
ΔG	Gain control range		20		dB
OIP3	3rd order intercept point		29		dBm

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Electrical Characteristics

Tamb.= +25°C, Vd = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		11	GHz
Gain	Linear Gain without control		23		dB
NF	Noise Figure at maximum gain		9		dB
RLin	Input return loss		-10		dB
RLout	Output return loss		-12		dB
OIP3	Output 3rd order intercept point @ max. gain		29		dBm
OIP3	Output 3rd order intercept point @ min. gain		26		dBm
P1dB	Power at 1dB compression @ all gain		24		dBm
ΔG	Gain control range		20		dB
VG12, VG3	DC gate voltage stage 1,2, 3		-1.3		V
GC	DC gain control voltage (GC1 & GC2)	-2.0		0	V
Vd	DC drain voltage		4.5		V
Id	Quiescent drain current (1)		160		mA

These values are representative of onboard measurements.

(1) Id not affected by GC

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5V	V
Id	Drain bias current	230	mA
VG12-VG3	Gate bias voltage	-2 to +0.4	V
GC1-GC2	Gain control voltage	-2.5 to +0.6	V
Pin	Maximum peak input power overdrive (2)	+7	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

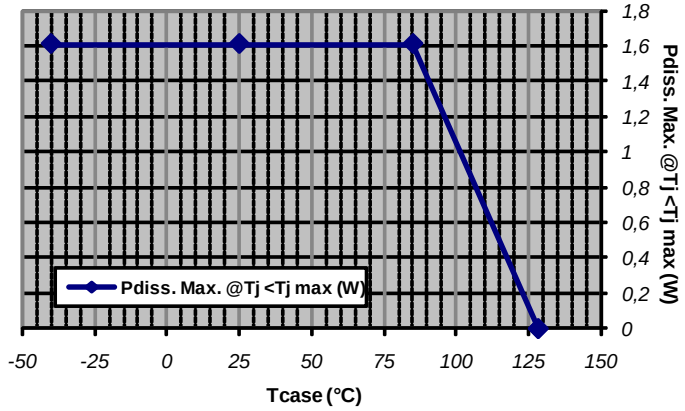
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

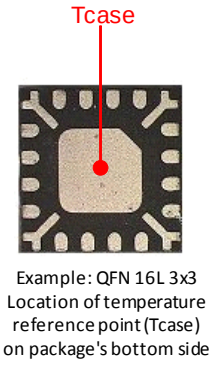
DEVICE THERMAL SPECIFICATION : CHA4861-QGG			
Recommended max. junction temperature (Tj max)	:	128	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	1,6	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	37	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<26	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Typical Package Sij parameters

Tamb.= +25°C, Vd = +4.5V, Id = 160 mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.2	92	-79.1	36	-35.5	146	-1.3	96
3.0	-1.4	45	-81.8	14	-19.1	-177	-1.9	43
4.0	-1.5	-4	-72.3	22	9.9	1	-3.6	-27
5.0	-2.3	-66	-84.7	-109	21.9	128	-12.2	-60
6.0	-7.3	-149	-71.7	61	23.9	-17	-20.5	-136
7.0	-19.6	78	-68	-6	24.9	-163	-18.4	-99
8.0	-14	-38	-73.6	-90	23.2	77	-18.9	-133
9.0	-11.4	-81	-78.6	-26	23.1	30	-15	-157
10.0	-10.8	-114	-68.6	-116	23.7	-150	-11.9	140
11.0	-11.1	-150	-59.9	-173	23.9	93	-13.3	76
12.0	-12.2	-96	-61.1	125	22.2	-84	-15.5	2
13.0	-8.3	-157	-61.3	111	9	153	-17.2	-36
14.0	-9.1	170	-56.1	114	-0.5	60	-15.9	-69
15.0	-10.9	144	-50.5	70	-8.8	-34	-14.9	-96
16.0	-13.7	77	-50.2	-15	-18.5	-177	-14.1	-164
17.0	-16.6	68	-52.3	-69	-29.8	95	-13	177
18.0	-17.6	69	-57.6	-15	-39.6	21	-12.2	156
19.0	-16.8	64	-50.9	-45	-45.5	-36	-11.8	134
20.0	-15	48	-51.7	-85	-49.7	-78	-11.9	109
21.0	-13.4	-157	-56.3	-78	-54.5	-76	-12.4	-100
22.0	-11.9	170	-51.7	-84	-51.6	-84	-13.4	-134
23.0	-10.1	136	-50.8	-82	-50.8	-77	-14.6	-179
24.0	-8.6	99	-46.4	-79	-45.6	-76	-14	125
25.0	-6.9	61	-43.4	-108	-41.5	-118	-11.4	75
26.0	-5.3	27	-44.3	-136	-43.7	-144	-8.6	36
27.0	-4.4	-6	-42.1	-137	-42.8	-130	-6.6	2
28.0	-2.8	-37	-38.6	-172	-39	-170	-5	-27
29.0	-2.3	-65	-39.1	169	-39.4	167	-4	-54
30.0	-1.8	-90	-36.3	143	-37.2	144	-3.3	-80
31.0	-1.6	-115	-35	111	-34.7	109	-2.9	-105
32.0	-1.5	-135	-37.5	50	-36.7	56	-2.6	-125
33.0	-1.5	-154	-39.5	33.	-39.5	38	-2.4	-145
34.0	-1.1	-171	-42	18.	-40.5	7	-1.9	-162
35.0	-1	174	-52.6	34.	-51.9	-10	-1.8	-180
36.0	-1	156	-42.5	56	-44.3	38	-1.6	165
37.0	-0.8	141	-44.1	19	-45.3	12	-1.2	152
38.0	-0.9	131	-46.4	9	-43	-27	-0.3	138
39.0	-0.8	117	-41.4	14	-42.3	0	-0.3	125
40.0	-0.5	98	-39	-54	-38.9	-59	-0.2	106

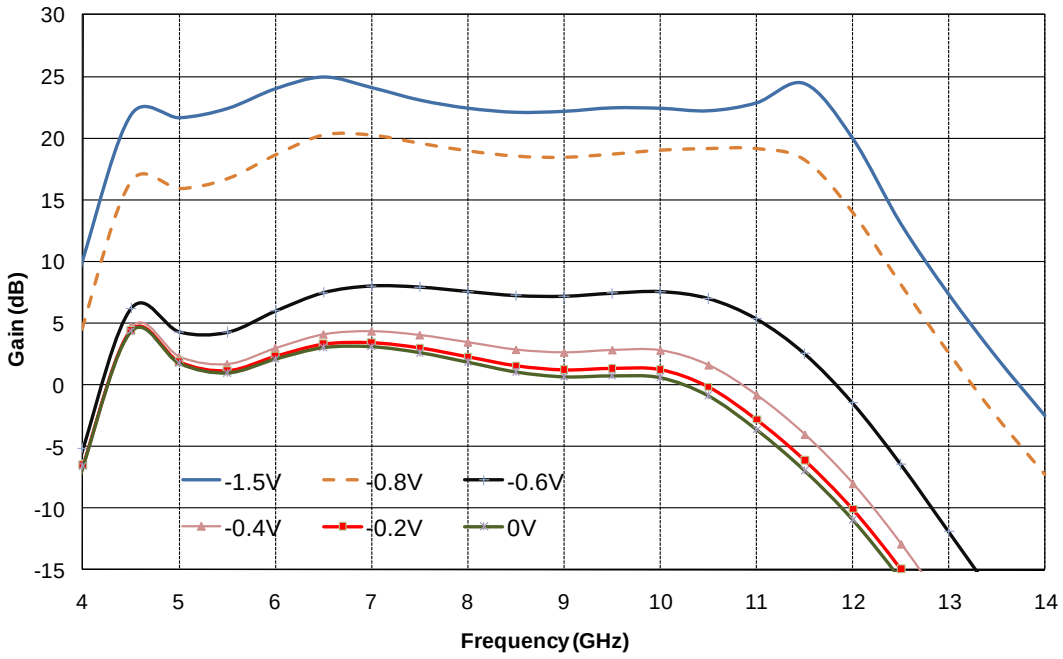
See paragraph “Definition of the Sij reference planes”

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

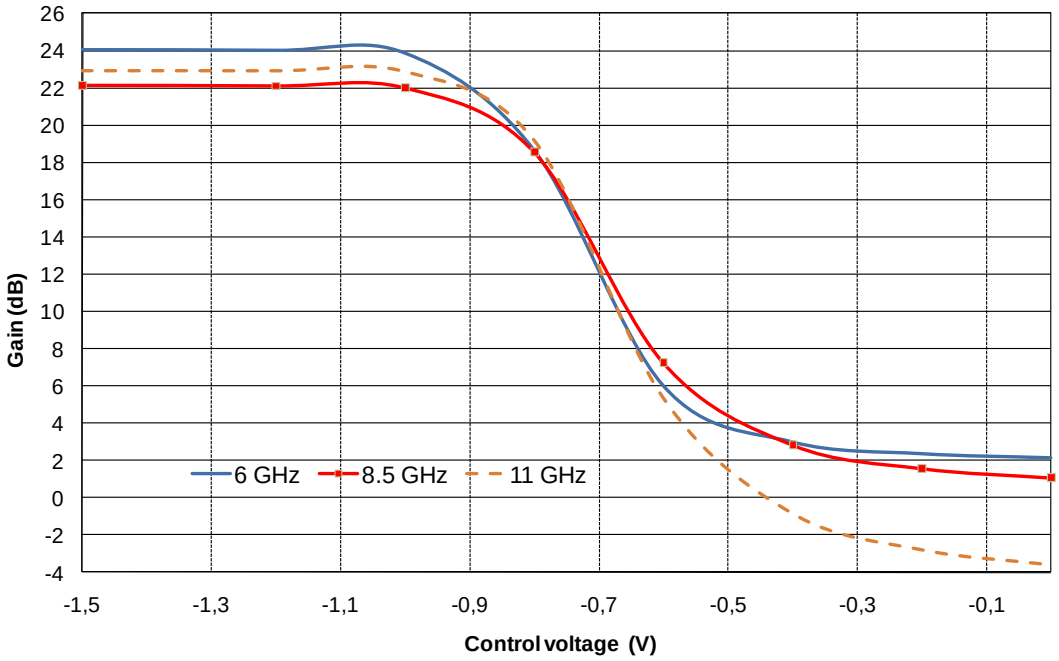
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 160mA
These measurements are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Board losses are de-embedded.

Linear Gain versus Frequency & Gain Control Voltage



Linear Gain versus Gain Control Voltage & frequency

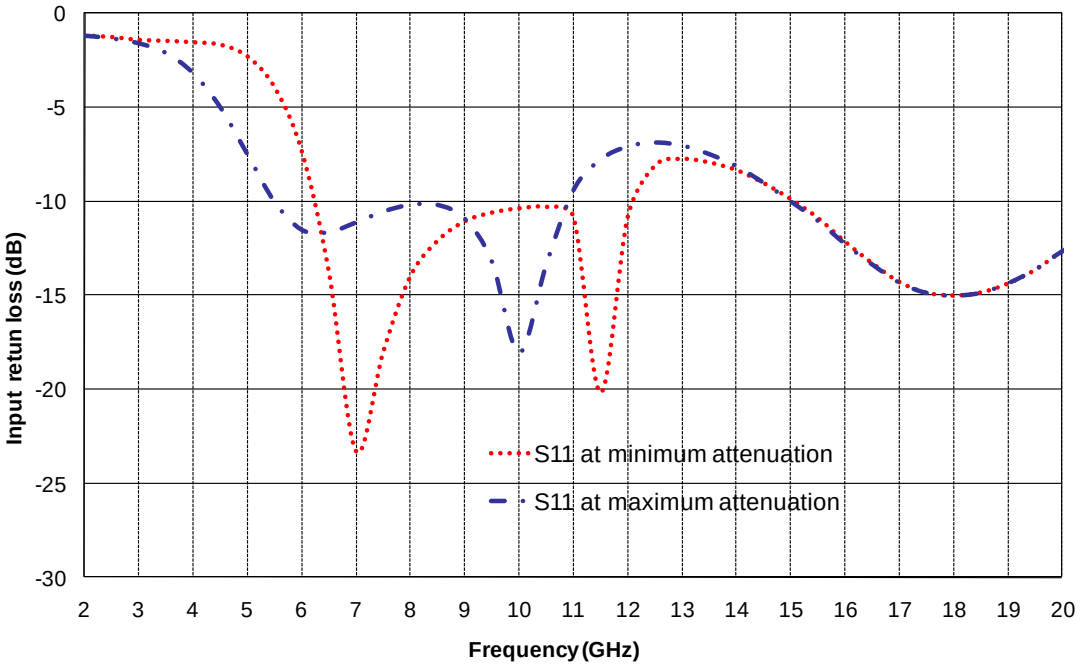


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

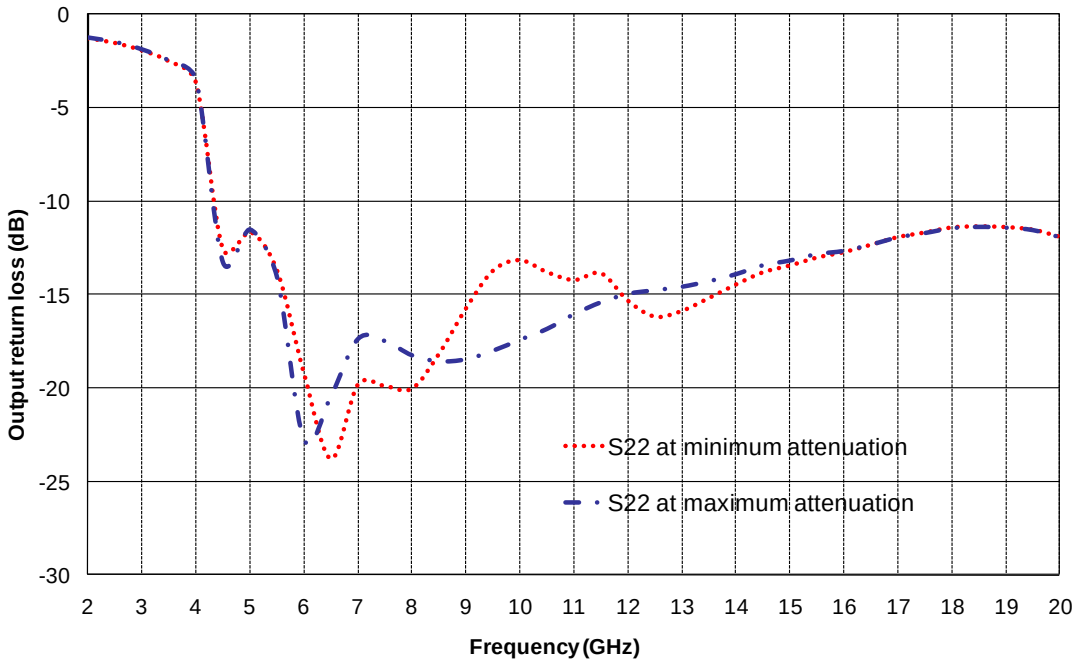
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 160mA

Input return loss at min. & max. gain



Output return loss at min & max gain

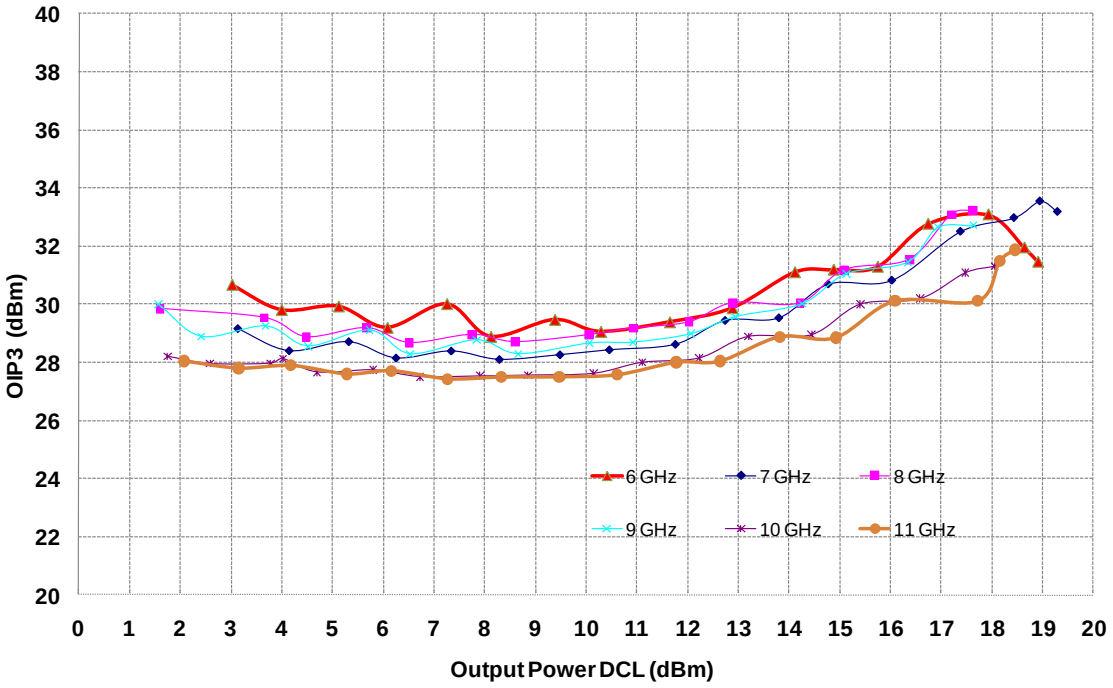


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

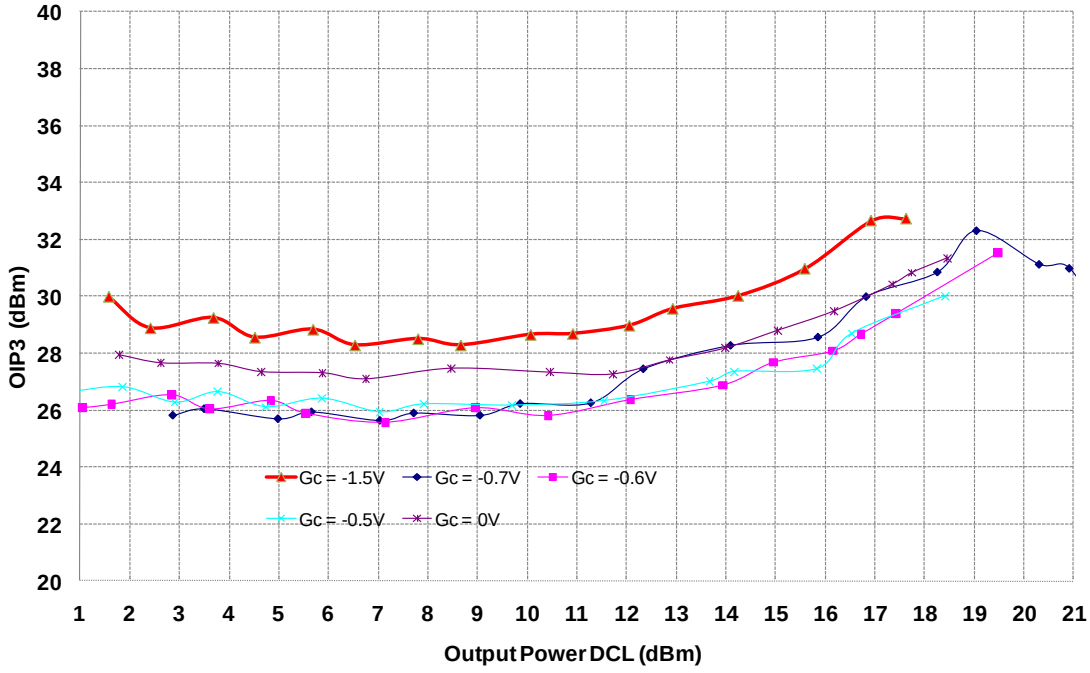
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 160mA

Output IP3 versus Output power & frequency at maximum gain (Gc1=Gc2= -1.5V)



Output IP3 at 9GHz versus Output power & gain control

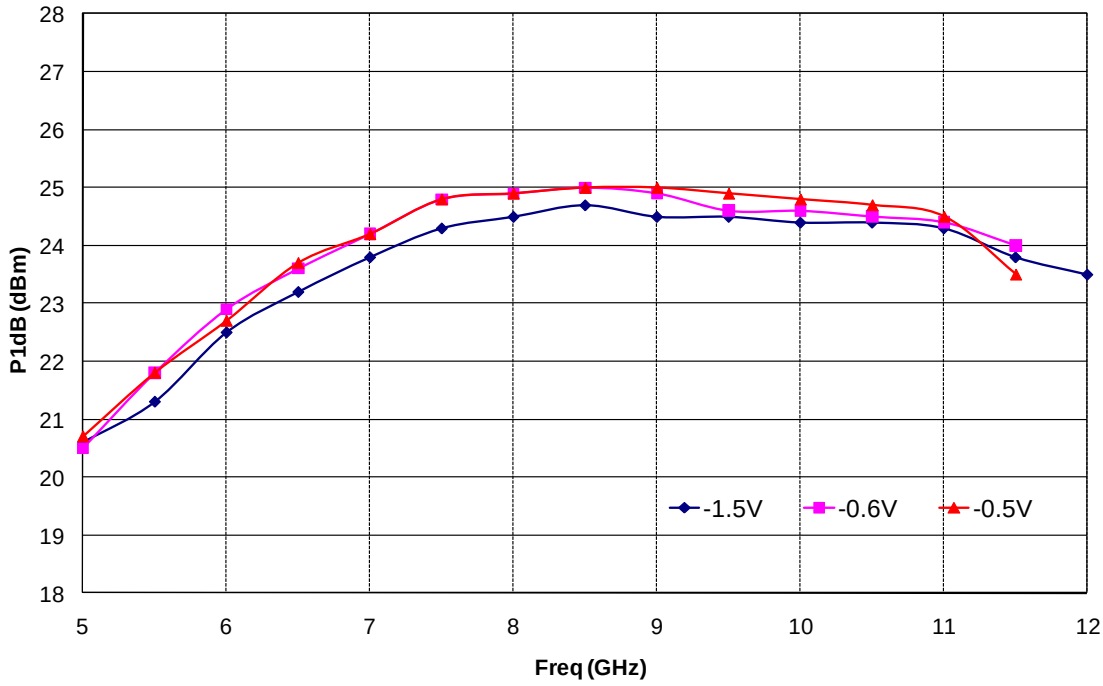


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

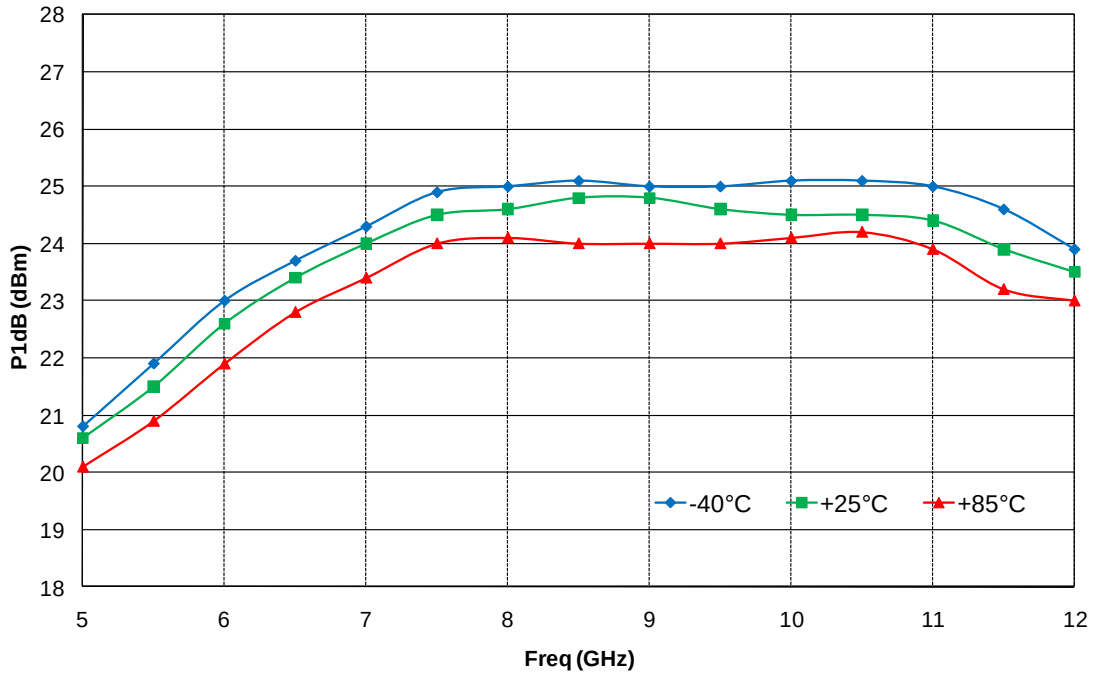
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 160mA

Output power at 1dB compression versus Frequency & gain control



Output power at 1dB compression versus Frequency & temperature at max gain

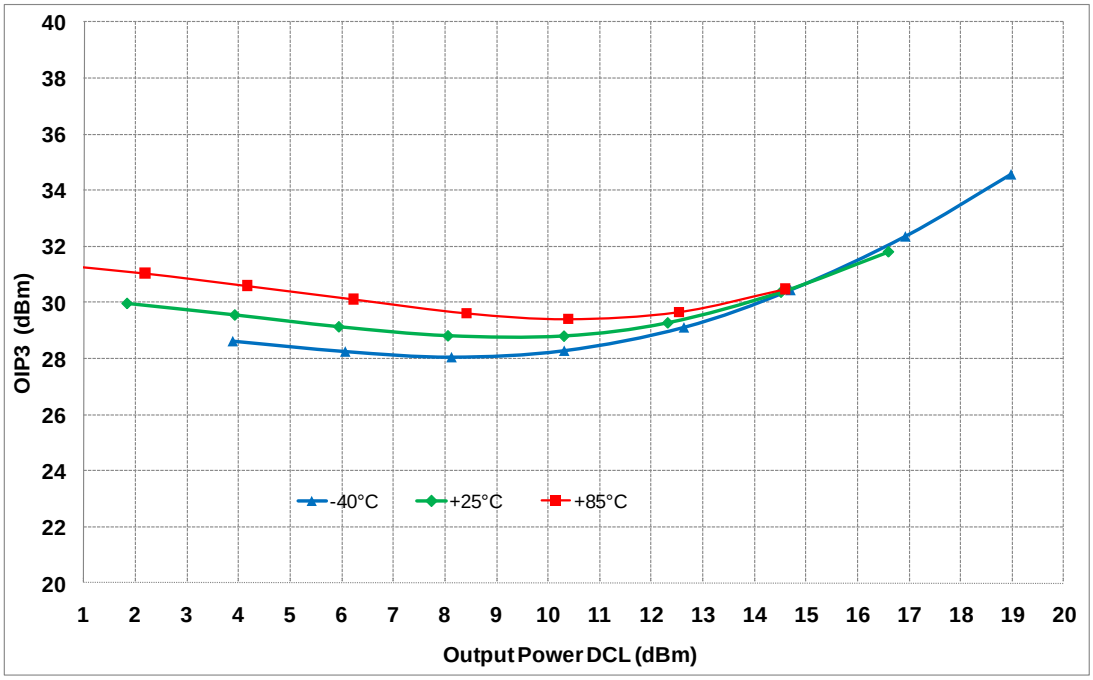


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

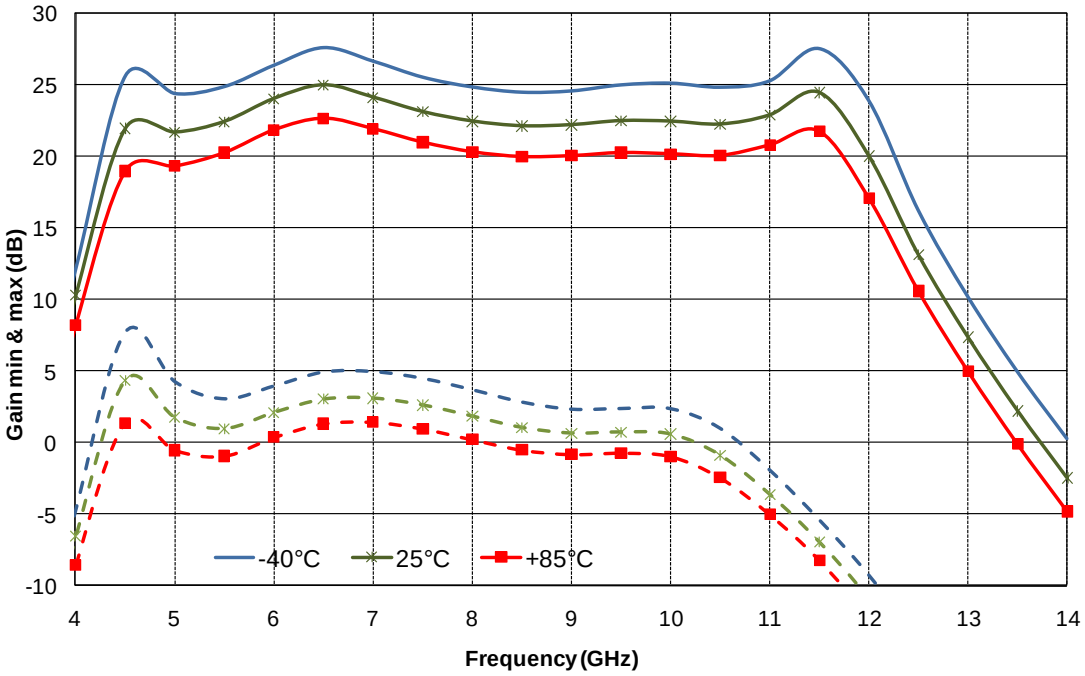
Typical Board Measurements

Tamb.= +25°C, Vd = +4.5V, Id = 160mA

Output IP3 versus Output power & temperature at 9GHz and maximum gain

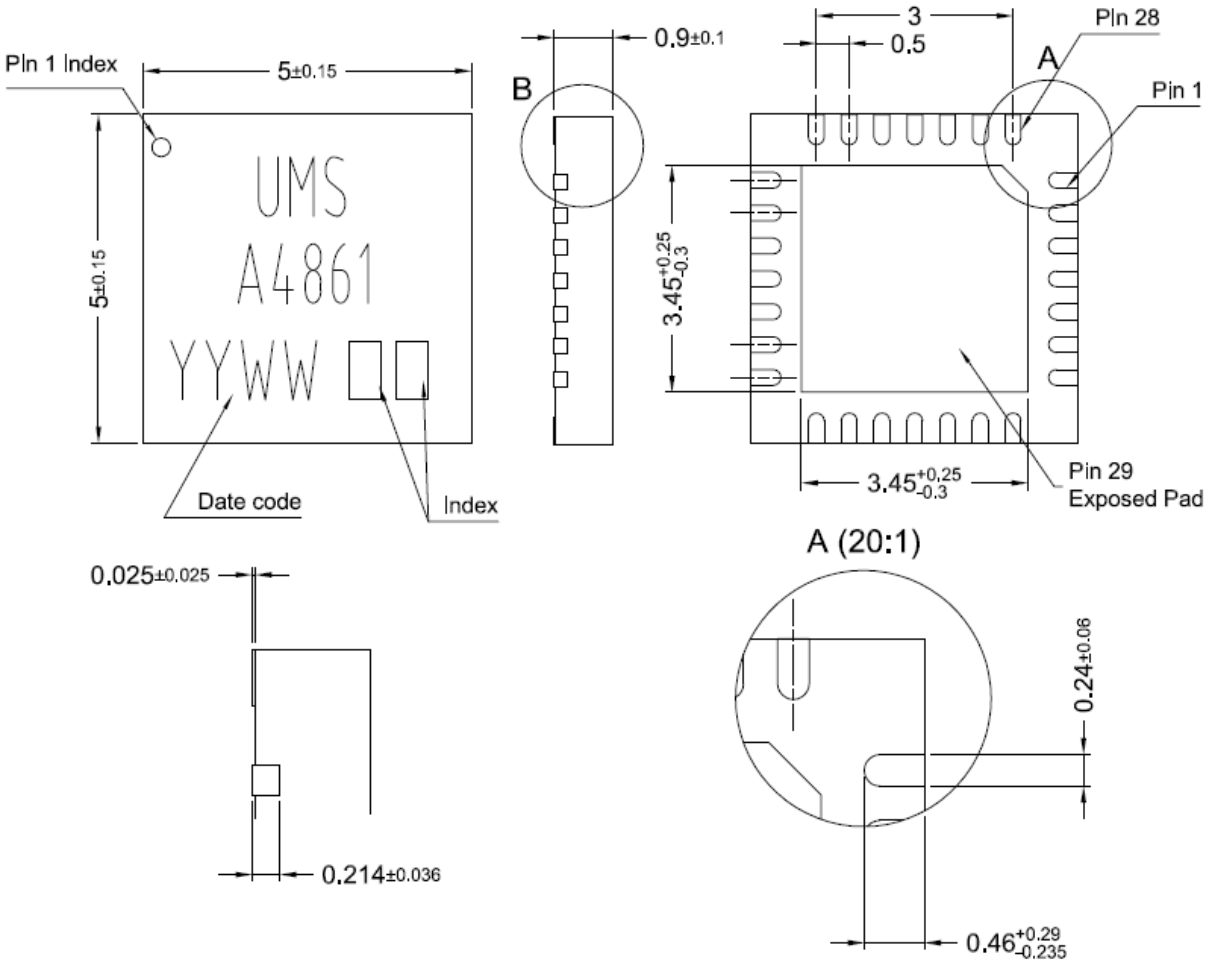


Maximum & minimum gain versus Frequency & temperature



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Package outline (1)



Matt tin, Lead Free (Green)		1- Gnd(2)	11- GC2	21- Gnd(2)
Units :	mm	2- RF IN	12- VG3	22- Nc
From the standard :	JEDEC MO-220 (VGGD)	3- Gnd(2)	13- Nc	23- Nc
		4- Gnd(2)	14- Nc	24- VD
29- GND		5- Nc	15- Gnd(2)	25- Nc
		6- Gnd(2)	16- Gnd(2)	26- Gnd(2)
		7- Gnd(2)	17- Nc	27- Nc
		8- Gnd(2)	18- Gnd(2)	28- Nc
		9- GC1	19- Gnd(2)	
		10- VG12	20- RF OUT	

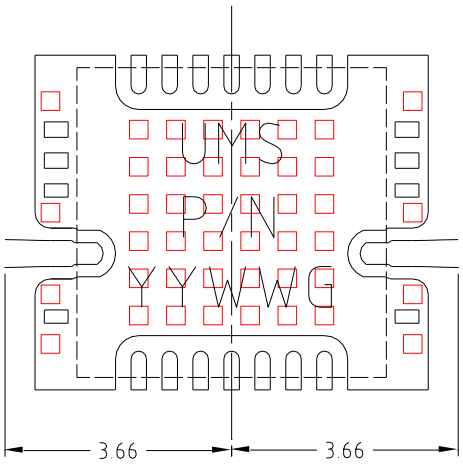
(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

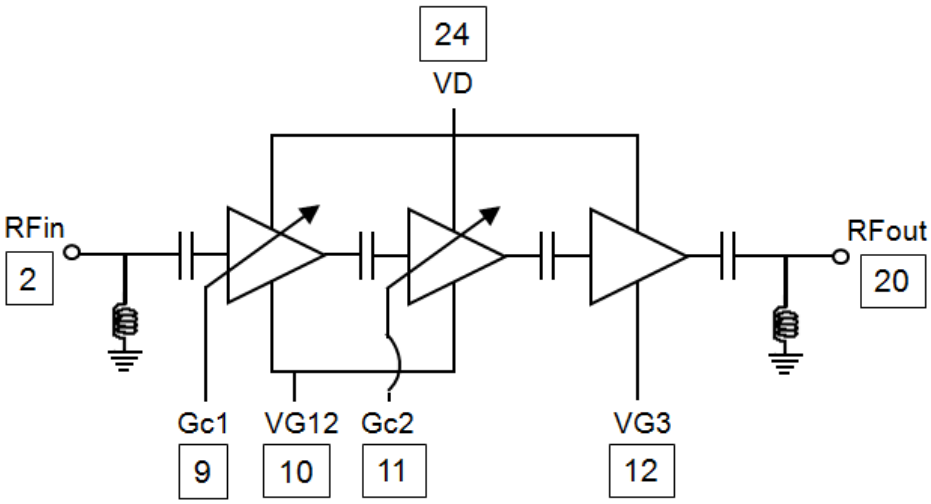
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

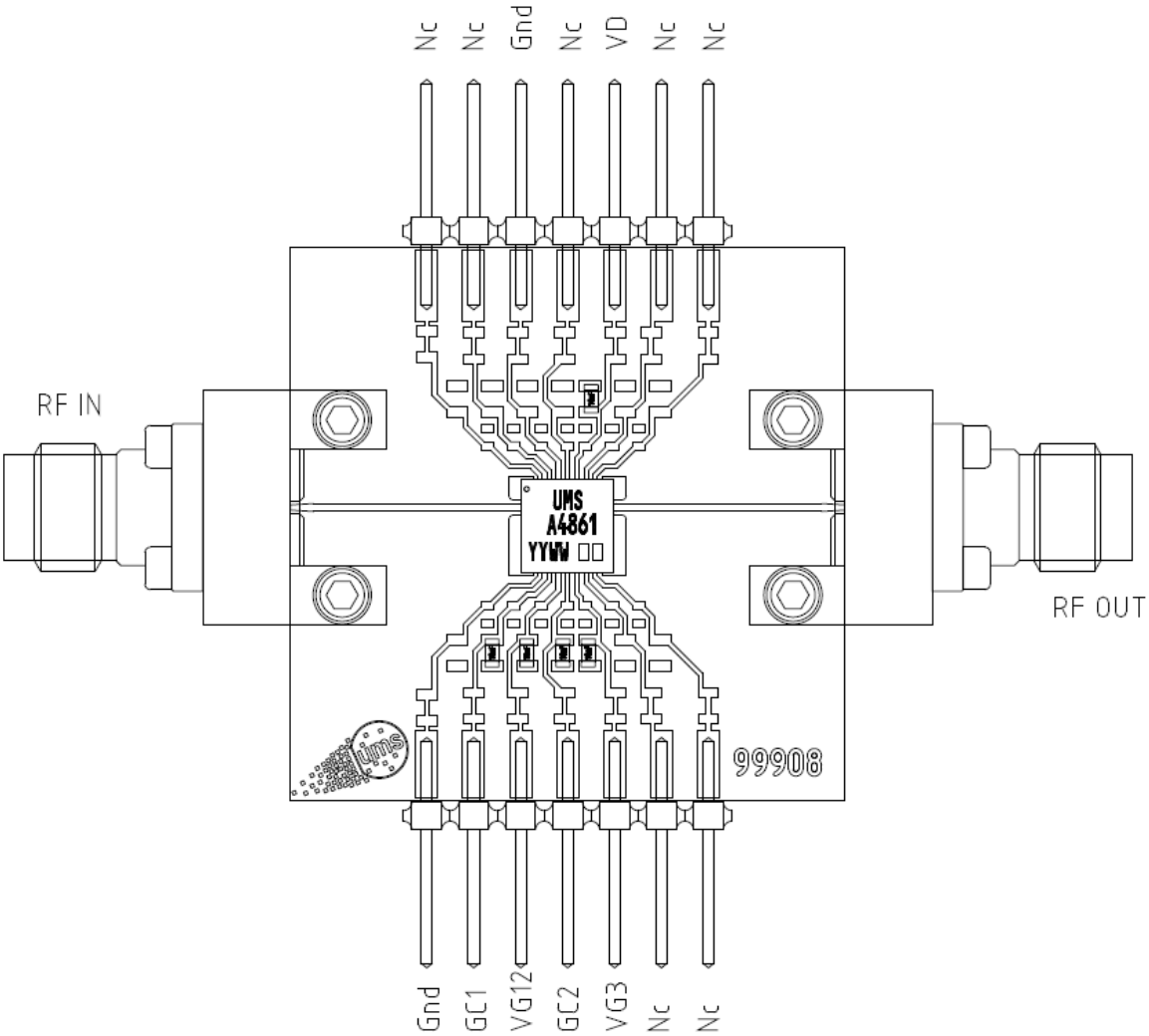


ESD protections are also implemented on gate and control accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

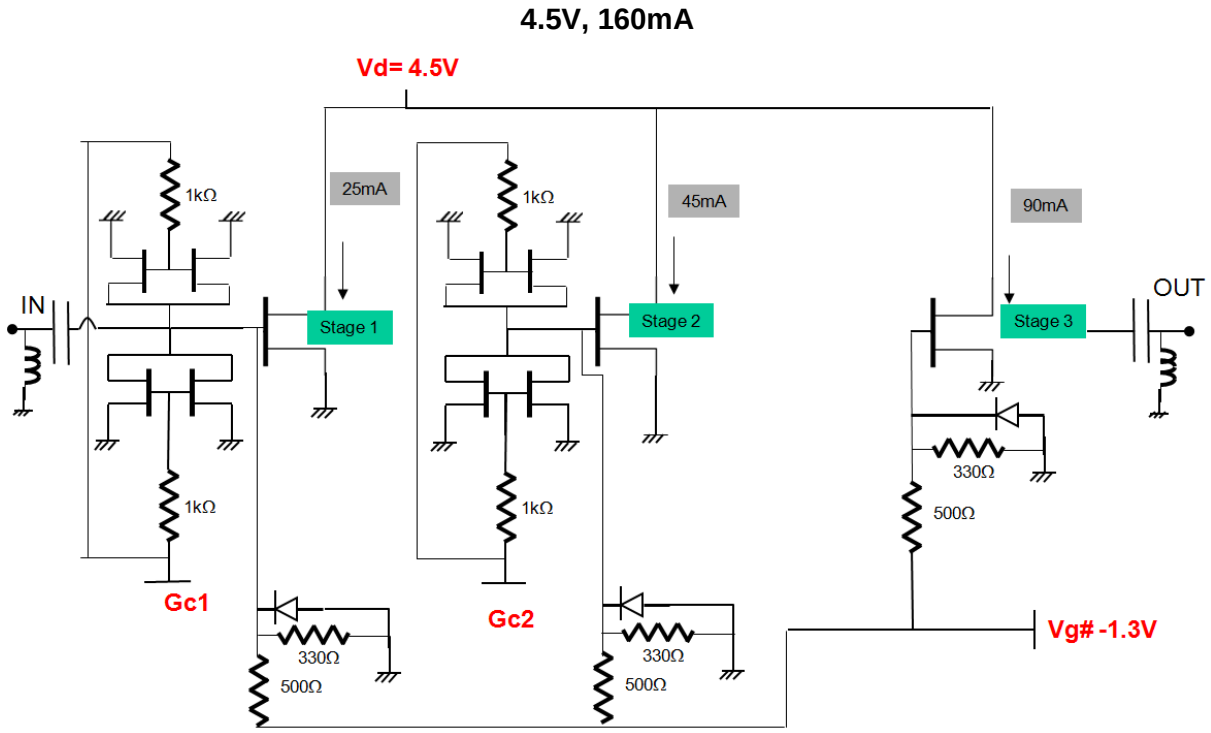
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

DC Schematic



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 package:	CHA4861-QGG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34