United Monolithic Semiconductors

CHA3666-99F

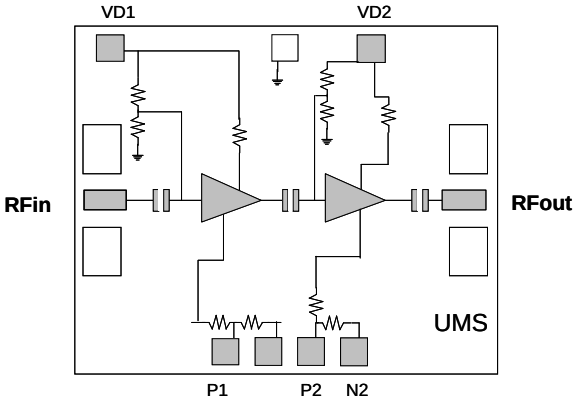
6-17GHz Low Noise Amplifier

GaAs Monolithic Microwave IC

Description

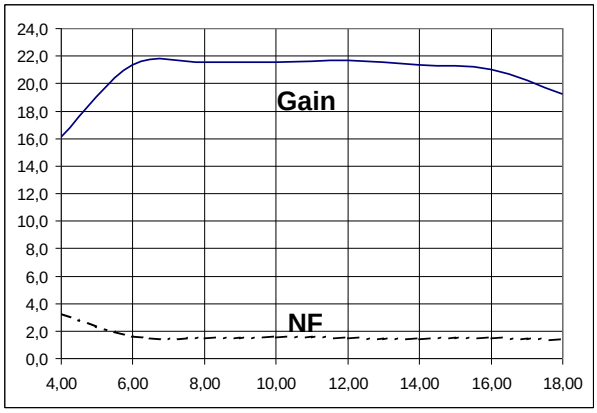
The CHA3666-99F is a two-stage self biased wide band monolithic low noise amplifier.

The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.



Main Features

- Broadband performances: 6-17GHz
- 1.8dB noise figure
- 26dBm 3rd order intercept point
- 17dBm power at 1dB compression
- 21dB gain
- Low DC power consumption
- DC bias: Vd=4.0Volt@Id=80mA
- Chip size 1.47x1.47x0.1mm



Main Electrical Characteristics

Tamb.= +25°C, Vd1=Vd2= +4V Pads: P1, N2=GND

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		17	GHz
NF	Noise figure		1.8	2	dB
G	Gain	19	21		dB
IP3	3rd order intercept point		26		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Temp = +25°C, Pads: P1, N2 = GND [1]

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		17	GHz
G	Gain [2]	19	21		dB
ΔG	Gain flatness		±0.5		dB
NF	Noise figure [2]		1.8	2	dB
IS11I	Input return loss [2]		2.5:1	2.7:1	dB
IS22I	Output return loss [2]		2.0:1	2.2:1	dB
IP3	3rd order intercept point [2]		26		dBm
P1dB	Output power at 1dB gain comp.[2] [3]	15	17		dBm
Vd	Drain bias voltage		4		V
Id	Drain bias current	60	80	100	mA
Top	Operating temperature range. [4]	-40		+85	°C

[1] The other pads are not connected.
[2] These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
[3] P1dB can be increased (+0.5dBm) when P1 & P2 are connected and N2 non-connected. In this case Id is typically 85mA.
[4] Operating temperature range refers to chip backside.

Absolute Maximum Ratings [1]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Pin	RF input power	10	dBm
Tstg	Storage temperature range	-55 to +125	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	Vd1	VD1 pad	4.0	V
Vd2	Vd2	VD2 pad	4.0	V
P1	P1	GND (connected to ground)	GND	
P2	P2	NC (not connected)	NC	
N2	N2	GND (connected to ground)	GND	

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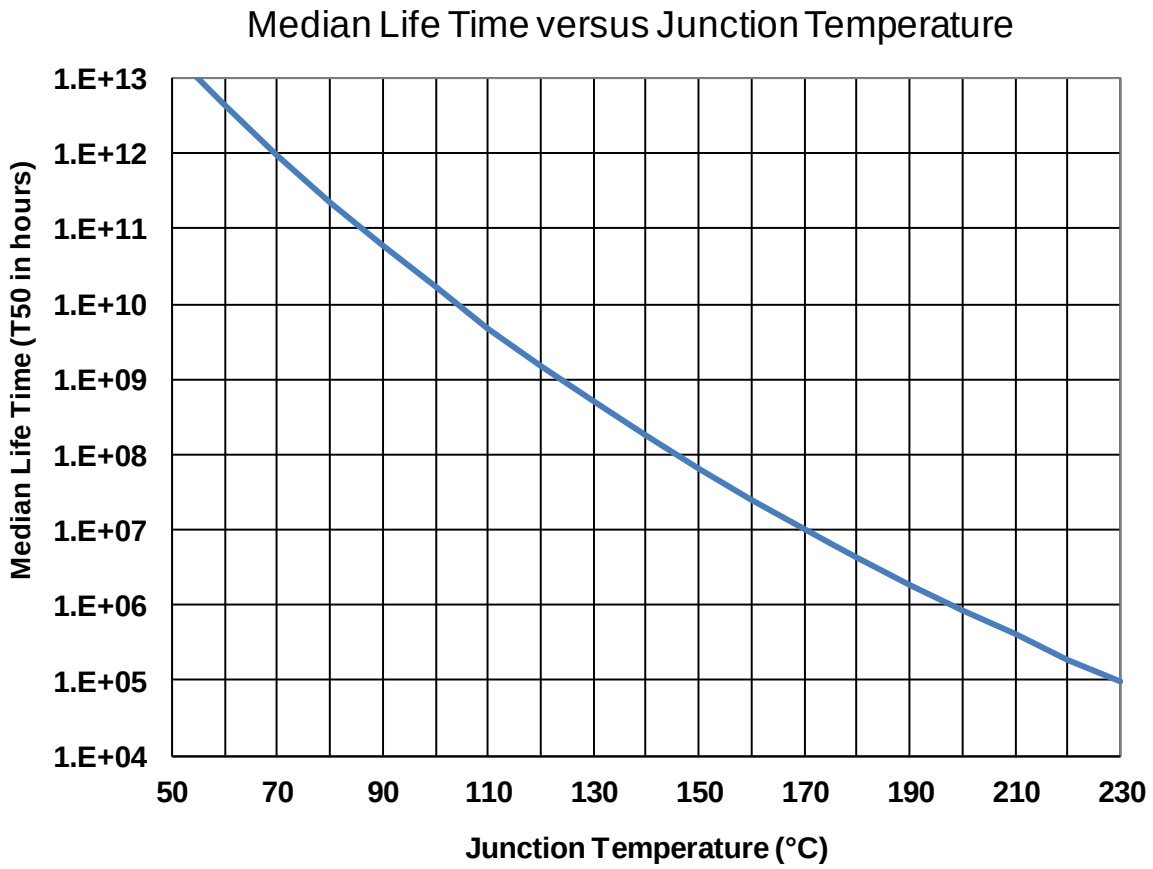
Device thermal performances

Thermal performances of the device are given below, based on the ums rules to evaluate the junction temperature.
This same procedure is the basis for the junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA3666-99F is fabricated (pHEMT 0.25µm).
The temperature Tb is defined as the chip back-side temperature.
The thermal resistance (Rth_eq) is given for the full circuit, and assume CW mode operation by default.

Parameter	Symbol	Conditions	Values	Unit
Thermal Resistance	Rth_eq	Tb = 85°C, P1: GND, N2: GND(1) 4V, 80mA, (Pdiss = 0.32W)	169	°C/W
Junction Temperature	Tj		139	°C
Median Lifetime	T50		$2.0x10^8$	Hrs
Thermal Resistance	Rth_eq	Tb = 85°C, P1: GND, P2: GND(1) 4V, 85mA, (Pdiss = 0.34W)	175	°C/W
Junction Temperature	Tj		145	°C
Median Lifetime	T50		$1.1x10^8$	Hrs

(1) Refer to “Chip Biasing options” section.



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Typical on-wafer Sij parameters

Tamb.= +25°C, Vd1=Vd2= +4V, Pads: P1, N2 = GND.

Freq GHZ	dBS11 dB	PhS11 °	dBS12 dB	PhS12 °	dBS21 dB	PhS21 °	dBS22 dB	PhS22 °
0,5	-0,12	-12,41	-58,07	-75,30	-55,39	74,95	-0,16	-11,79
1,0	-0,15	-25,18	-66,93	158,40	-59,74	86,43	-0,19	-23,89
1,5	-0,21	-38,83	-68,19	-42,37	-55,53	-2,66	-0,26	-37,09
2,0	-0,31	-54,17	-70,23	132,40	-28,46	25,79	-0,62	-51,84
2,5	-0,53	-72,61	-66,09	-174,80	-11,74	2,26	-1,03	-68,34
3,0	-0,99	-96,30	-58,45	112,50	1,55	-54,65	-2,92	-84,65
3,5	-2,07	-129,20	-57,93	51,75	9,78	-105,90	-5,03	-92,78
4,0	-4,44	179,00	-53,52	-50,92	15,92	-157,20	-7,10	-98,70
4,5	-8,15	104,20	-48,40	-119,10	19,62	149,90	-8,51	-98,52
5,0	-9,23	35,18	-45,69	-159,90	21,13	103,90	-9,15	-100,90
5,5	-9,21	-2,42	-43,80	169,70	21,84	65,87	-9,80	-104,20
6,0	-9,07	-20,75	-42,66	145,70	22,14	34,89	-10,53	-107,90
6,5	-8,93	-30,17	-40,68	125,10	22,22	6,85	-10,91	-113,20
7,0	-8,37	-38,97	-40,46	107,20	22,22	-17,33	-11,49	-119,50
7,5	-7,99	-47,52	-39,16	88,92	22,19	-39,18	-11,76	-128,70
8,0	-7,87	-56,29	-38,17	75,16	22,23	-59,70	-12,47	-141,30
8,5	-7,75	-63,59	-38,58	62,12	22,19	-79,40	-13,87	-154,90
9,0	-7,54	-71,38	-37,51	42,64	22,08	-97,96	-15,57	-168,10
9,5	-7,50	-79,76	-37,26	36,06	22,03	-115,30	-17,57	176,80
10,0	-7,55	-88,86	-36,90	26,77	21,97	-132,00	-20,19	157,60
10,5	-7,77	-97,01	-36,76	12,22	21,93	-148,40	-23,18	132,40
11,0	-8,11	-105,90	-36,05	-1,08	21,90	-164,10	-25,38	96,42
11,5	-8,53	-114,50	-35,65	-13,41	21,88	-179,90	-26,39	54,20
12,0	-8,98	-122,60	-35,55	-24,05	21,86	164,70	-24,69	16,73
12,5	-9,62	-130,10	-35,31	-35,87	21,82	149,40	-22,43	-8,28
13,0	-10,22	-135,40	-35,13	-50,20	21,75	134,30	-20,23	-25,56
13,5	-10,60	-143,40	-35,13	-60,43	21,72	119,10	-19,67	-36,11
14,0	-11,07	-153,70	-34,80	-76,43	21,74	104,00	-19,22	-45,27
14,5	-11,34	-160,80	-34,90	-81,33	21,73	88,96	-18,20	-51,93
15,0	-11,28	-175,20	-36,47	-95,20	21,84	73,08	-17,69	-63,45
15,5	-11,14	164,00	-36,88	-112,40	21,64	55,53	-18,61	-77,33
16,0	-11,46	146,10	-37,33	-119,70	21,52	41,16	-17,96	-72,90
16,5	-10,91	125,00	-38,29	-129,70	21,68	24,37	-16,63	-75,48
17,0	-10,01	100,10	-38,86	-155,40	21,60	5,25	-14,95	-83,86
17,5	-9,02	72,69	-41,04	-161,40	21,15	-14,81	-13,51	-102,40
18,0	-8,00	45,92	-42,41	-173,60	20,44	-35,47	-12,40	-120,70
18,5	-7,75	21,28	-45,21	-161,70	19,26	-51,39	-13,47	-130,90
19,0	-7,02	0,74	-47,61	-177,80	18,39	-69,18	-11,57	-142,30
19,5	-6,59	-18,52	-50,99	-127,80	17,14	-86,07	-10,58	-160,60
20,0	-6,38	-35,21	-45,57	-104,20	15,75	-101,50	-9,99	-176,80

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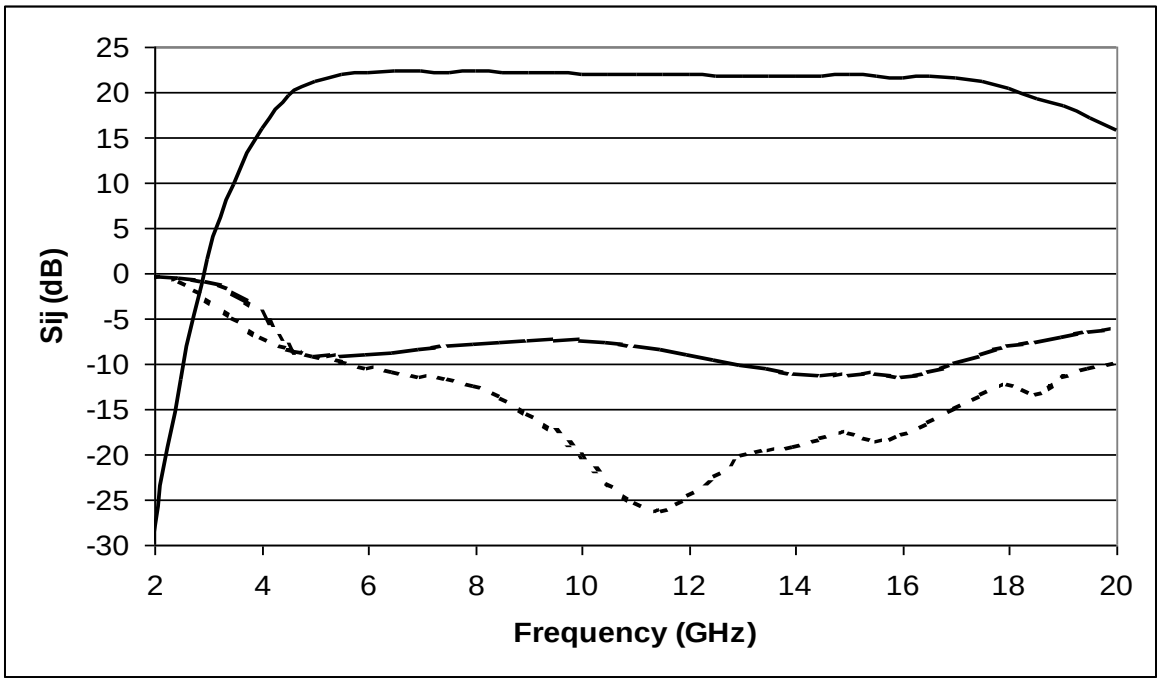
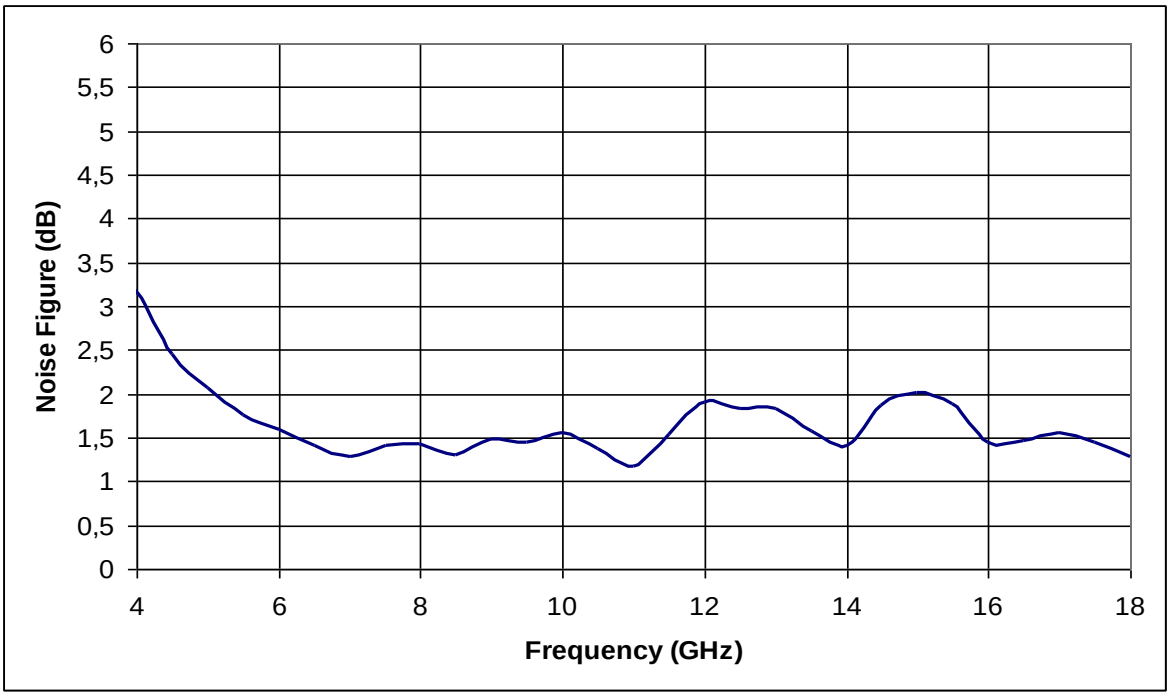
Typical on wafer Measurements

Tamb.= +25°C, Vd1=Vd2= +4V - Pads: P1, N2 = GND - Id=80mA Typical Measurements on wafer (without bonding wires at the RF ports)

S parameters versus frequency



NF versus frequency



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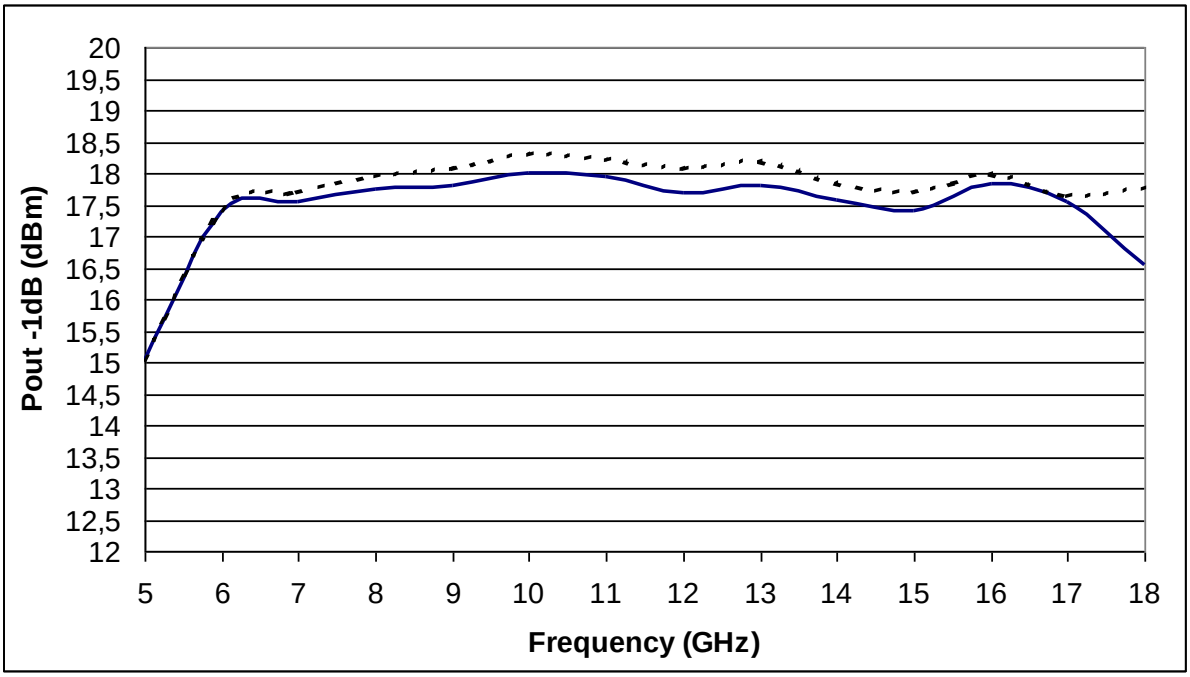
Typical on wafer Measurements

Tamb.= +25°C, Vd1=Vd2= +4V
Measurements on wafer (without bonding wires at the RF ports)

Output power at 1dB compression gain versus frequency



Plain : *Pads: P1, N2 = GND - Id=80mA Typical*
Dash : *Pads: P1, P2 = GND - Id=85mA Typical*

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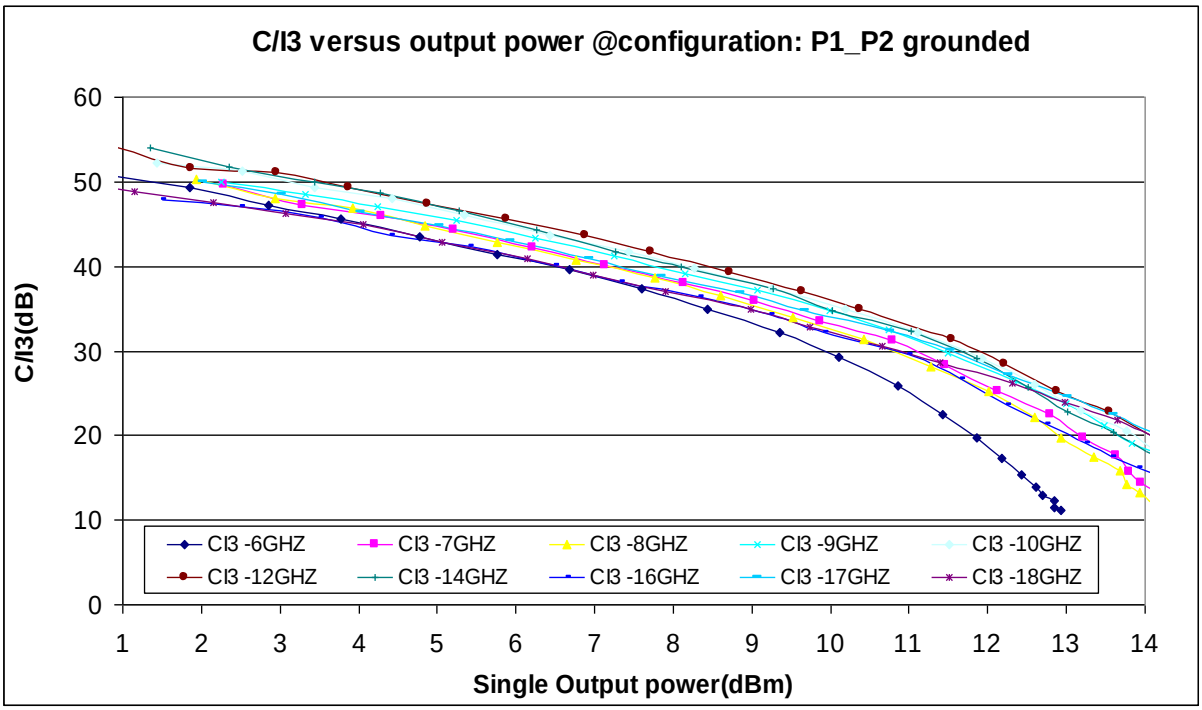
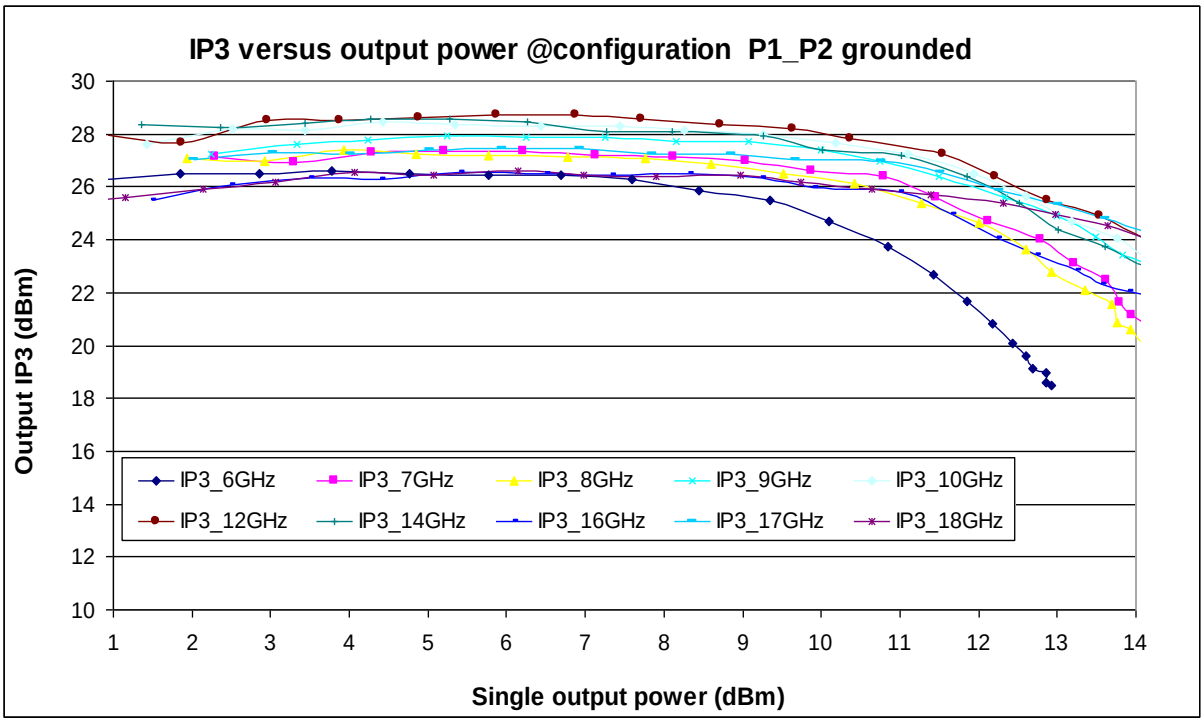
Typical on wafer Measurements

Tamb.= +25°C, Vd1=Vd2= +4V - Pads: P1, P2 = GND - Id=85mA Typical Measurements on wafer (without bonding wires at the RF ports)





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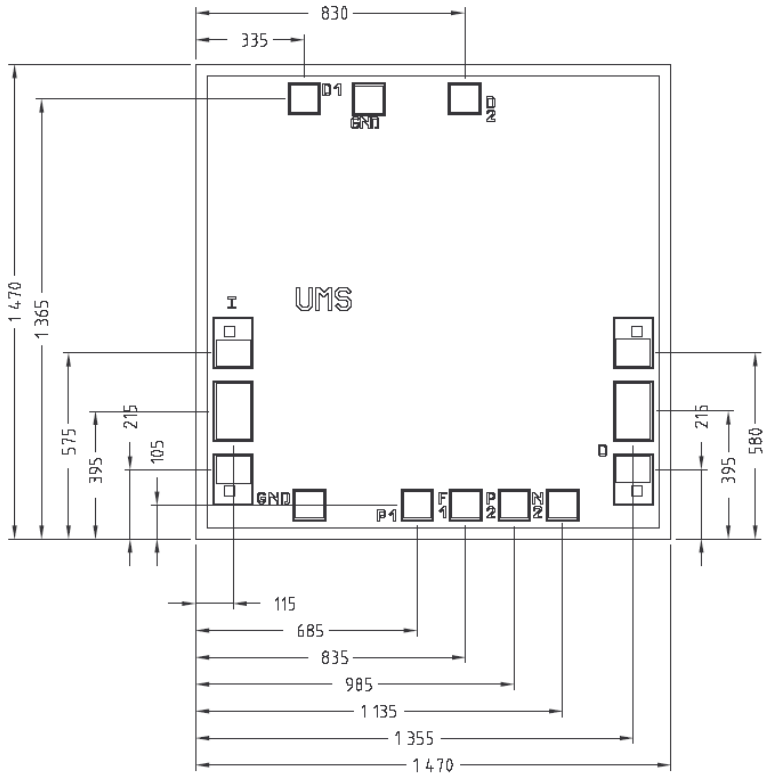
Mechanical data



Chip thickness: 100µm.
Chip size: 1.47 x 1.47 ±35µm
All dimensions are in micrometers
DC Pads size: 100x100µm.

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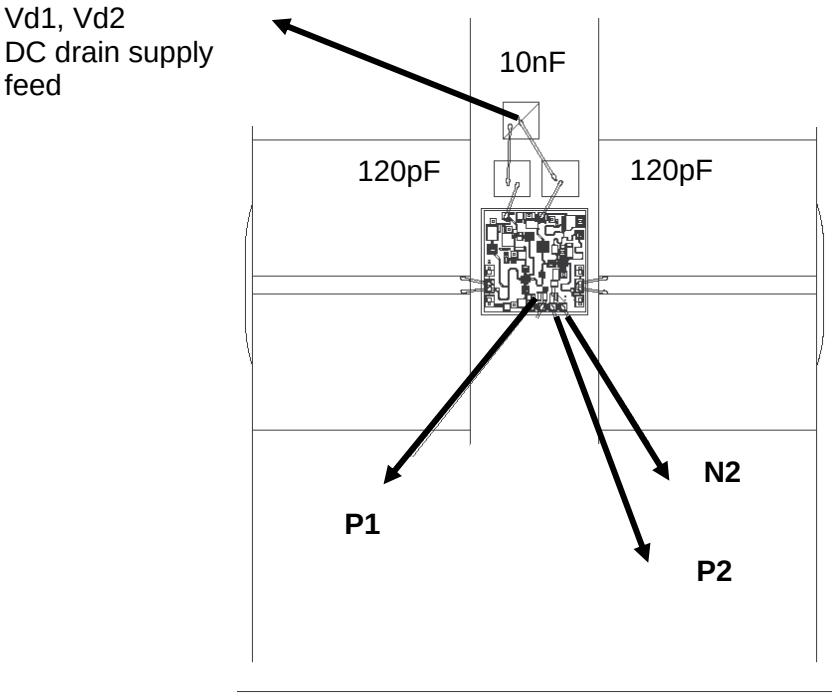
Recommended assembly plan



25µm wedge bonding is preferred

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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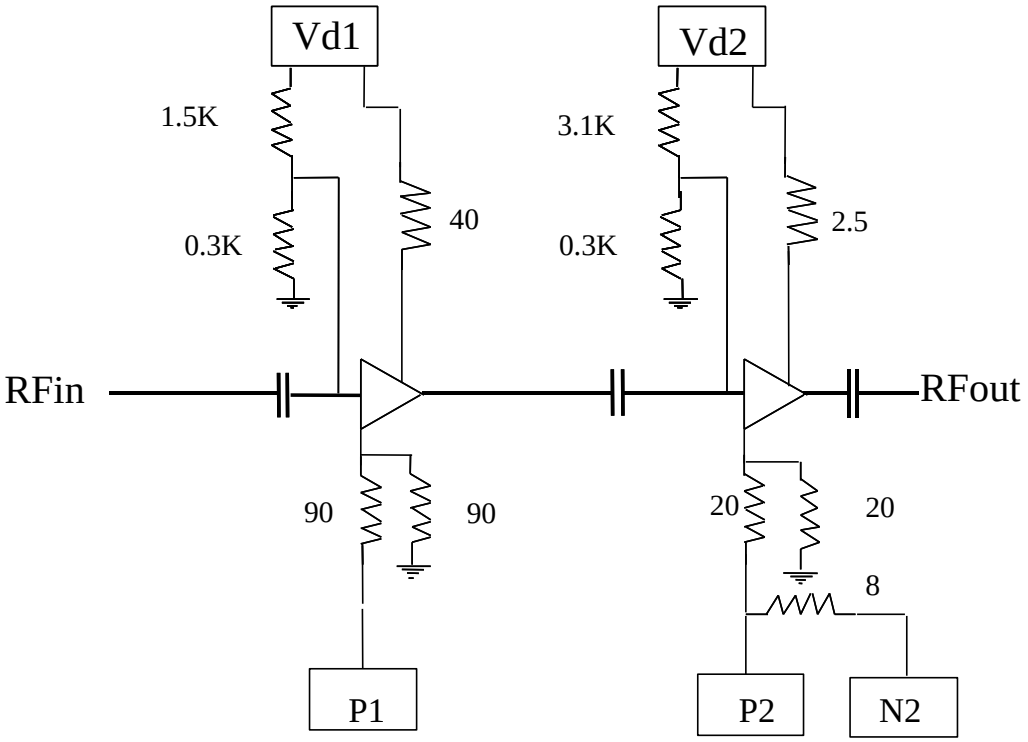
Chip Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



Two standard biasing:

Low Noise and low consumption:

Vd1=Vd2 = 4V and P1, N2 grounded.
P2 pads non connected (NC).
Idd = 80mA & Pout-1dB = 17dBm Typical.

Low Noise and higher output power:

Vd1=Vd2 = 4V and P1, P2 grounded.
N2 pads non connected (NC).
Idd = 85mA & Pout-1dB = 17.5dBm Typical.

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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA3666-99F/00

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