# SINGLE-ENDED, ANALOG-INPUT 24-BIT, 96-kHz STEREO A/D CONVERTER

Check for Samples: PCM1808-Q1

## FEATURES

- **Qualified for Automotive Applications**
- **24-Bit Delta-Sigma Stereo A/D Converter**
- **Single-Ended Voltage Input: 3 Vp-p**
- **High Performance:**
  - **THD + N: –93 dB (Typical)**
  - **SNR: 99 dB (Typical)**
  - **Dynamic Range: 99 dB (Typical)**
- **Oversampling Decimation Filter:**
  - **Oversampling Frequency: ×64**
  - **Pass-Band Ripple: ±0.05 dB**
  - **Stop-Band Attenuation: –65 dB**
  - **On-Chip High-Pass Filter: 0.91 Hz (48 kHz)**
- **Flexible PCM Audio Interface**
  - **Master/Slave Mode Selectable**
  - **Data Formats: 24-Bit I$^2$S, 24-Bit Left-Justified**
- **Power Down and Reset by Halting System Clock**
- **Analog Antialias LPF Included**
- **Sampling Rate: 8 kHz–96 kHz**
- **System Clock: 256 f$_S$, 384 f$_S$, 512 f$_S$**
- **Dual Power Supplies:**
  - **5-V for Analog**
  - **3.3-V for Digital**

- **Package: 14-Pin TSSOP**

## DESCRIPTION

The PCM1808-Q1 is high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The PCM1808-Q1 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the PCM1808-Q1 supports master and slave mode and two data formats in serial audio interface.

The PCM1808-Q1 supports the power-down and reset function by means of halting the system clock.

The PCM1808-Q1 is suitable for wide variety of cost-sensitive consumer applications where good performance and operation with a 5-V analog supply and 3.3-V digital supply is required. The PCM1808-Q1 is fabricated using a highly advanced CMOS process and is available in a small, 14-pin TSSOP package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

|  | PCM1808-Q1 |
|---|---|
| Analog supply voltage, $V_{CC}$ | −0.3 V to 6.5 V |
| Digital supply voltage, $V_{DD}$ | −0.3 V to 4 V |
| Ground voltage differences, AGND, DGND | ±0.1 V |
| Digital input voltage, LRCK, BCK, DOUT | −0.3 V to ($V_{DD}$ + 0.3 V) < 4 V |
| Digital input voltage, SCKI, MD0, MD1, FMT | −0.3 V to 6.5 V |
| Analog input voltage, $V_{IN}L$, $V_{IN}R$, $V_{REF}$ | −0.3 V to ($V_{CC}$ + 0.3 V) < 6.5 V |
| Input current (any pins except supplies) | ±10 mA |
| Ambient temperature under bias, $T_A$ | −40°C to 125°C |
| Storage temperature, $T_{stg}$ | −55°C to 150°C |
| Junction temperature, $T_J$ | 150°C |
| Lead temperature (soldering) | 260°C, 5 s |
| Package temperature (reflow, peak) | 260°C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage, $V_{CC}$ |  | 4.5 | 5 | 5.5 | V |
| Digital supply voltage, $V_{DD}$ |  | 2.7 | 3.3 | 3.6 | V |
| Analog input voltage, full scale (−0 dB) | $V_{CC}$ = 5 V | 2.93 | 3 | 3.23 | Vp-p |
| Digital input logic family |  | TTL compatible | | | |
| Digital input clock frequency, system clock |  | 2.048 | | 49.152 | MHz |
| Digital input clock frequency, sampling clock |  | 8 | | 96 | kHz |
| Digital output load capacitance |  | | | 20 | pF |
| Operating free-air temperature, $T_A$ |  | −40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Resolution | | | | 24 | | Bits |
| **DATA FORMAT** | | | | | | | |
| | Audio data interface format | | | | $I^2S$, left-justified | | |
| | Audio data bit length | | | | 24 | | Bits |
| | Audio data format | | | | MSB-first, 2s complement | | |
| $f_S$ | Sampling frequency | | | 8 | 48 | 96 | kHz |
| | System clock frequency, –40°C ≤ $T_A$ ≤ 125°C[1] | 256 $f_S$ | | 2.048 | 12.288 | 24.576 | MHz |
| | | 384 $f_S$ | | 3.072 | 18.432 | 36.864 | |
| | | 512 $f_S$ | | 4.096 | 24.576 | 49.152 | |
| **INPUT LOGIC** | | | | | | | |
| $V_{IH}$ [2] | Input logic level, –40°C ≤ $T_A$ ≤ 125°C[3] | | | 2 | | $V_{DD}$ | VDC |
| $V_{IL}$ [2] | | | | 0 | | 0.8 | |
| $V_{IH}$ [4] [5] | | | | 2 | | 5.5 | |
| $V_{IL}$ [4] [5] | | | | 0 | | 0.8 | |
| $I_{IH}$ [4] | Input logic current | $V_{IN}$ = $V_{DD}$ | | | | ±10 | µA |
| $I_{IL}$ [4] | | $V_{IN}$ = 0 V | | | | ±10 | |
| $I_{IH}$ [2] [5] | | $V_{IN}$ = $V_{DD}$ | at 25°C | | 65 | 100 | |
| | | | –40°C ≤ $T_A$ ≤ 125°C | | 65 | 150 | |
| $I_{IL}$ [2] [5] | | $V_{IN}$ = 0 V | | | | ±10 | |
| **OUTPUT LOGIC** | | | | | | | |
| $V_{OH}$ [6] | Output logic level[3] | $I_{OUT}$ = –4 mA | at 25°C | 2.8 | | | VDC |
| | | | –40°C ≤ $T_A$ ≤ 125°C | 2.7 | | | |
| $V_{OL}$ [6] | | $I_{OUT}$ = 4 mA, –40°C ≤ $T_A$ ≤ 125°C | | | | 0.5 | |
| **DC ACCURACY, –40°C ≤ $T_A$ ≤ 125°C** | | | | | | | |
| | Gain mismatch, channel-to-channel | | | | ±1 | ±3 | % of FSR |
| | Gain error | | | | ±3 | ±6 | % of FSR |
| **DYNAMIC PERFORMANCE** [7] | | | | | | | |
| THD + N | Total harmonic distortion + noise | $V_{IN}$ = –0.5 dB, $f_S$ = 48 kHz | at 25°C | | –93 | –87 | dB |
| | | | –40°C ≤ $T_A$ ≤ 125°C | | –93 | –85 | |
| | | $V_{IN}$ = –0.5 dB, $f_S$ = 96 kHz [8] | | | –87 | | |
| | | $V_{IN}$ = –60 dB, $f_S$ = 48 kHz | | | –37 | | |
| | | $V_{IN}$ = –60 dB, $f_S$ = 96 kHz [8] | | | –39 | | |
| | Dynamic range | $f_S$ = 48 kHz, A-weighted | at 25°C | 95 | 99 | | dB |
| | | | –40°C ≤ $T_A$ ≤ 125°C | 93 | 99 | | |
| | | $f_S$ = 96 kHz, A-weighted [8] | | | 101 | | |
| S/N | Signal-to-noise ratio | $f_S$ = 48 kHz, A-weighted | at 25°C | 95 | 99 | | dB |
| | | | –40°C ≤ $T_A$ ≤ 125°C | 93 | 99 | | |
| | | $f_S$ = 96 kHz, A-weighted [8] | | | 101 | | |

(1) 384 $f_s$ where $f_s$ = 96kHz, and 512 where $f_s$ = 48 kHz and 96kHz are functionally tested. Other options are specified by design.
(2) Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, in slave mode)
(3) Specified by design
(4) Pin 6: SCKI (Schmitt-trigger input, 5-V tolerant)
(5) Pins 10–12: MD0, MD1, FMT (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(6) Pins 7–9: LRCK, BCK (in master mode), DOUT
(7) Analog performance specifications are tested using a System Two™ audio measurement system by Audio Precision™ with 400-Hz HPF and 20-kHz LPF in RMS mode.
(8) $f_S$ = 96 kHz, system clock = 256 $f_S$.

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Channel separation | $f_S$ = 48 kHz | at 25°C | | 93 | 97 | | dB |
| | | −40°C ≤ $T_A$ ≤ 125°C | | 91 | 97 | | |
| | $f_S$ = 96 kHz [8] | | | | 91 | | |
| **ANALOG INPUT** | | | | | | | |
| Input voltage, −40°C ≤ $T_A$ ≤ 125°C | | | | 0.58 $V_{CC}$ | 0.6 $V_{CC}$ | 0.65 $V_{CC}$ | Vp-p |
| Center voltage input range, −40°C ≤ $T_A$ ≤ 125°C | | | | 0.2 $V_{CC}$ | 0.5 $V_{CC}$ | 0.8 $V_{CC}$ | V |
| Input impedance | | | | | 60 | | kΩ |
| Antialiasing filter frequency response | −3 dB | | | | 1.3 | | MHz |
| **DIGITAL FILTER PERFORMANCE, −40°C ≤ $T_A$ ≤ 125°C [3]** | | | | | | | |
| Pass band | | | | | | 0.454 $f_S$ | Hz |
| Stop band | | | | 0.583 $f_S$ | | | Hz |
| Pass-band ripple | | | | | | ±0.05 | dB |
| Stop-band attenuation | | | | −65 | | | dB |
| Delay time | | | | | 17.4/$f_S$ | | |
| HPF frequency response | −3 dB | | | | 0.019 $f_S$/1000 | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | |
| $V_{CC}$ | Voltage range, −40°C ≤ $T_A$ ≤ 125°C | | | 4.5 | 5 | 5.5 | VDC |
| $V_{DD}$ | | | | 2.7 | 3.3 | 3.6 | |
| $I_{CC}$ | Supply current [9] | $f_S$ = 48 kHz, 96 kHz, −40°C ≤ $T_A$ ≤ 125°C [10] | | | 8.6 | 11 | mA |
| | | Powered down [11] | | | 1 | | µA |
| $I_{DD}$ | | $f_S$ = 48 kHz | at 25°C | | 5.9 | 8 | mA |
| | | | −40°C ≤ $T_A$ ≤ 125°C | | 5.9 | 10 | |
| | | $f_S$ = 96 kHz [10] | | | 10.2 | | mA |
| | | Powered down [11] | | | 150 | | µA |
| | Power dissipation [9] | $f_S$ = 48 kHz | | | 62 | 81 | mW |
| | | $f_S$ = 96 kHz [10] | | | 77 | | |
| | | Powered down [11] | | | 500 | | µW |
| **TEMPERATURE RANGE** | | | | | | | |
| $T_A$ | Operation temperature | | | −40 | | 125 | °C |
| $θ_{JA}$ | Thermal resistance | | | | 170 | | °C/W |

(9)  Minimum load on LRCK (pin 7), BCK (pin 8), DOUT (pin 9)
(10)  $f_S$ = 96 kHz, system clock = 256 $f_S$.
(11)  Power-down and reset functions enabled by halting SCKI, BCK, LRCK.

## PIN ASSIGNMENTS

**PW PACKAGE**
**(TOP VIEW)**

```
VREF  □□ 1    14 □□ VINR
AGND  □□ 2    13 □□ VINL
VCC   □□ 3    12 □□ FMT
VDD   □□ 4    11 □□ MD1
DGND  □□ 5    10 □□ MD0
SCKI  □□ 6     9 □□ DOUT
LRCK  □□ 7     8 □□ BCK
```
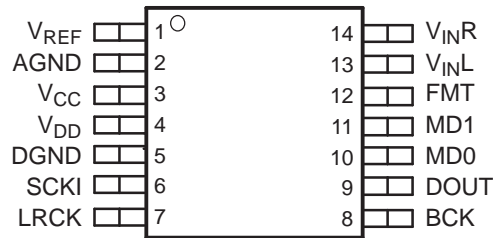
P0032-02

## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | PIN | | |
| AGND | 2 | – | Analog GND |
| BCK | 8 | I/O | Audio data bit clock input/output [1] |
| DGND | 5 | – | Digital GND |
| DOUT | 9 | O | Audio data digital output |
| FMT | 12 | I | Audio interface format select [2] |
| LRCK | 7 | I/O | Audio data latch enable input/output [1] |
| MD0 | 10 | I | Audio interface mode select 0 [2] |
| MD1 | 11 | I | Audio interface mode select 1 [2] |
| SCKI | 6 | I | System clock input; 256 $f_S$, 384 $f_S$ or 512 $f_S$ [3] |
| $V_{CC}$ | 3 | – | Analog power supply, 5-V |
| $V_{DD}$ | 4 | – | Digital power supply, 3.3-V |
| $V_{IN}L$ | 13 | I | Analog input, L-channel |
| $V_{IN}R$ | 14 | I | Analog input, R-channel |
| $V_{REF}$ | 1 | – | Reference voltage decoupling (= 0.5 $V_{CC}$) |

(1) Schmitt-trigger input with internal pulldown (50-kΩ, typical)
(2) Schmitt-trigger input with internal pulldown (50-kΩ, typical), 5-V tolerant
(3) Schmitt-trigger input, 5-V tolerant

5

# PCM1808-Q1

## Functional Block Diagram
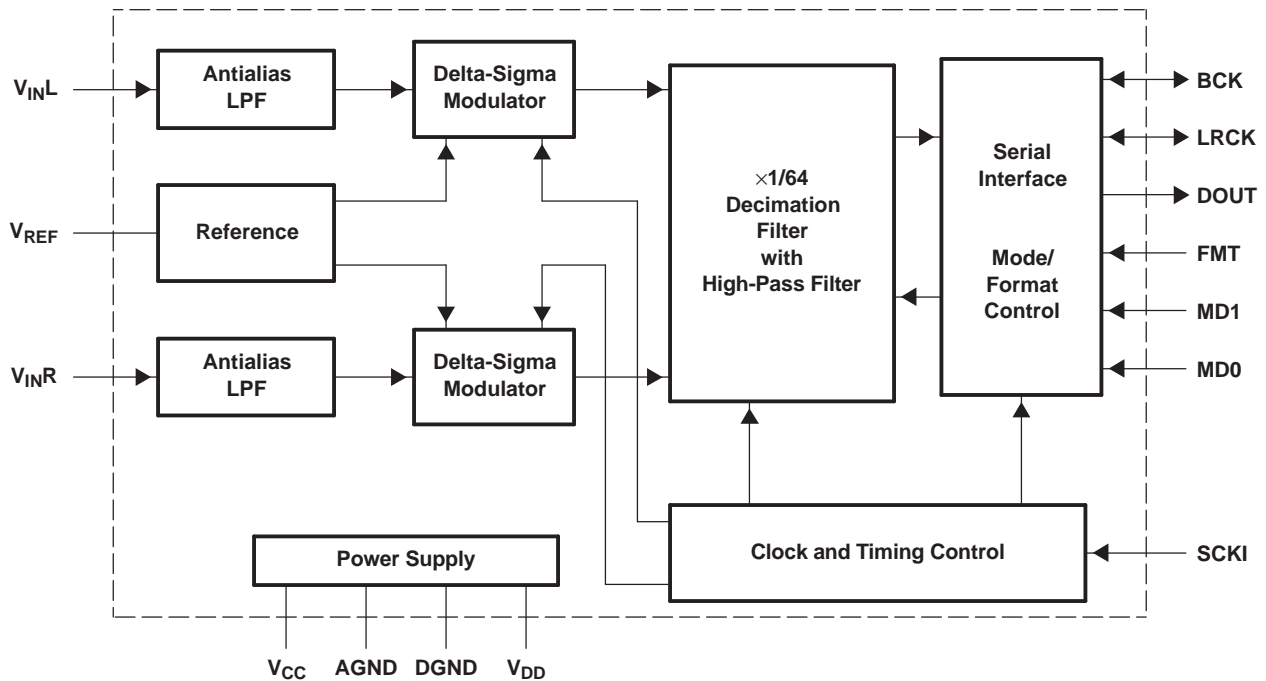


B0004-10

## TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted.
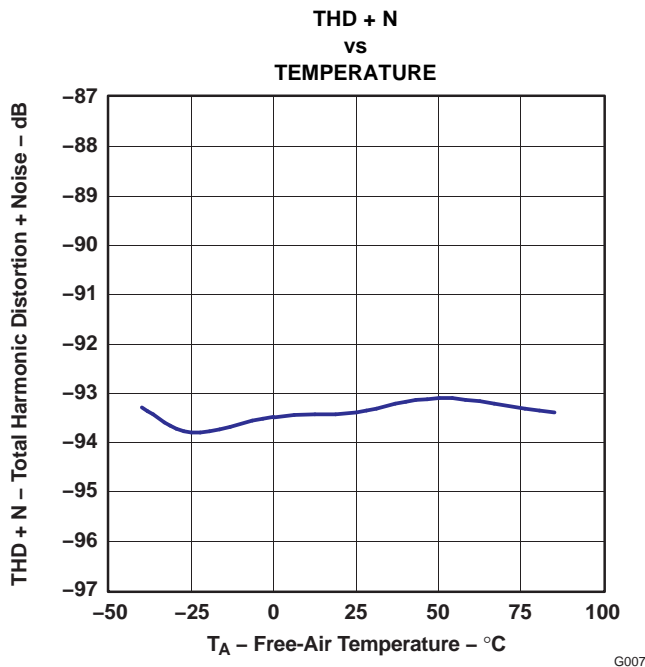
## DECIMATION FILTER FREQUENCY RESPONSE
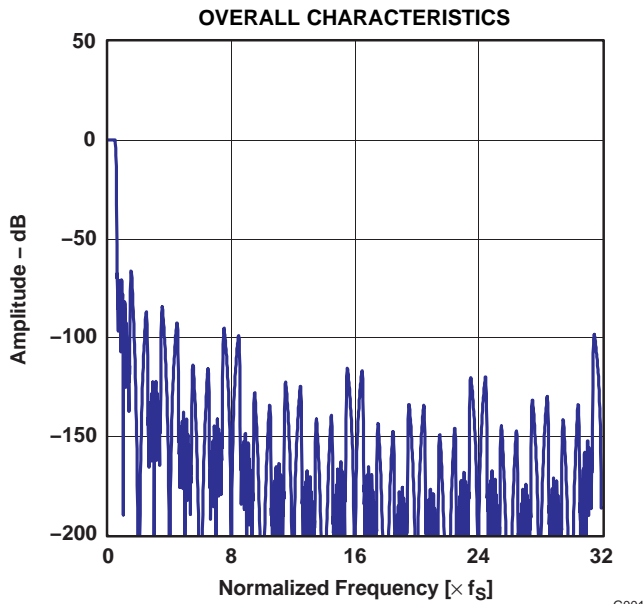


Figure 1.
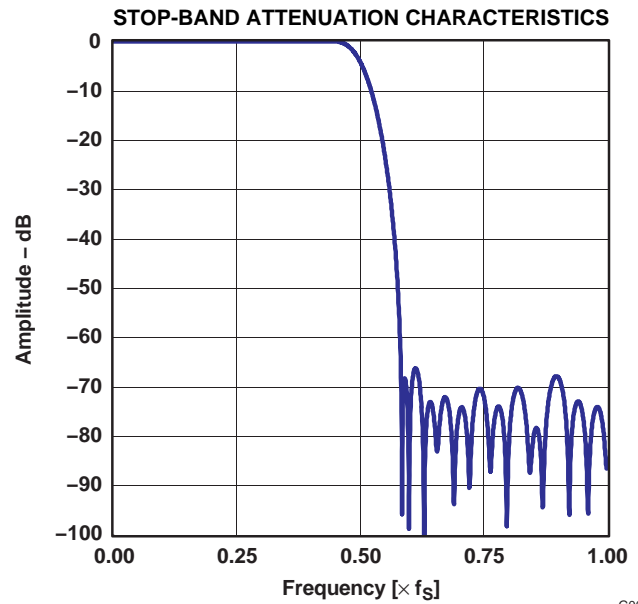


Figure 2.

## TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (Continued)

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted.

## DECIMATION FILTER FREQUENCY RESPONSE (Continued)

PASS-BAND RIPPLE CHARACTERISTICS

G003

**Figure 3.**

TRANSITION BAND CHARACTERISTICS

−4.13 dB at 0.5 $f_S$

G004
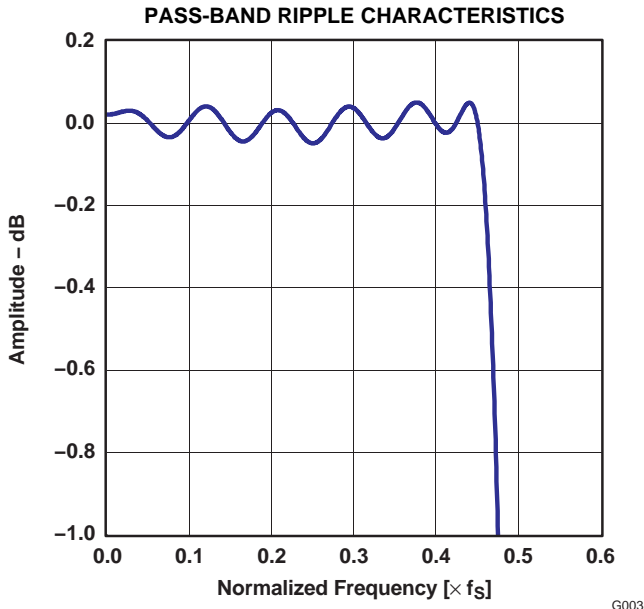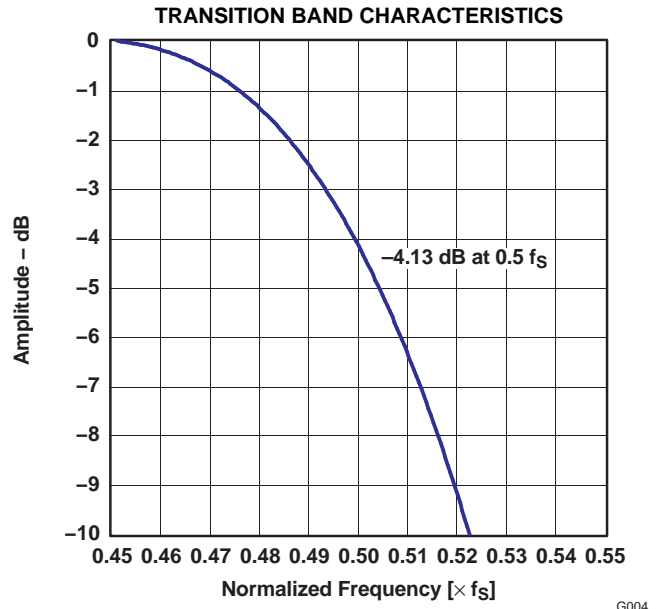
**Figure 4.**

## HIGH-PASS FILTER FREQUENCY RESPONSE

HPF STOP-BAND CHARACTERISTICS

G005

**Figure 5.**

HPF PASS-BAND CHARACTERISTICS

G006
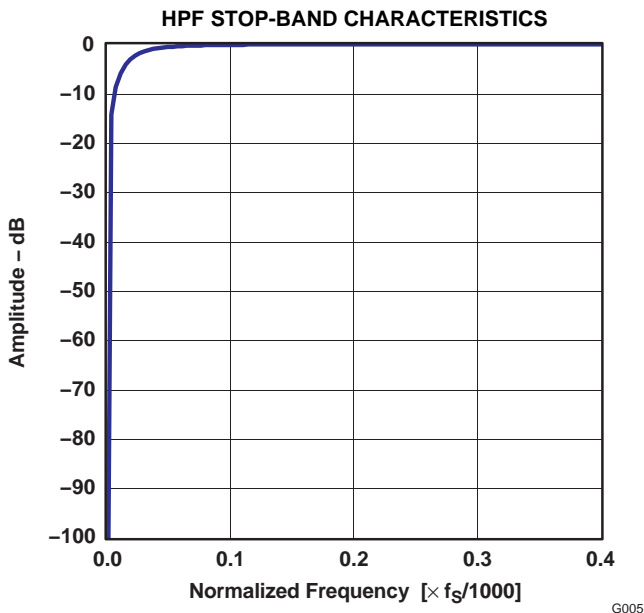
**Figure 6.**

## TYPICAL PERFORMANCE CURVES

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted.

THD + N
vs
TEMPERATURE
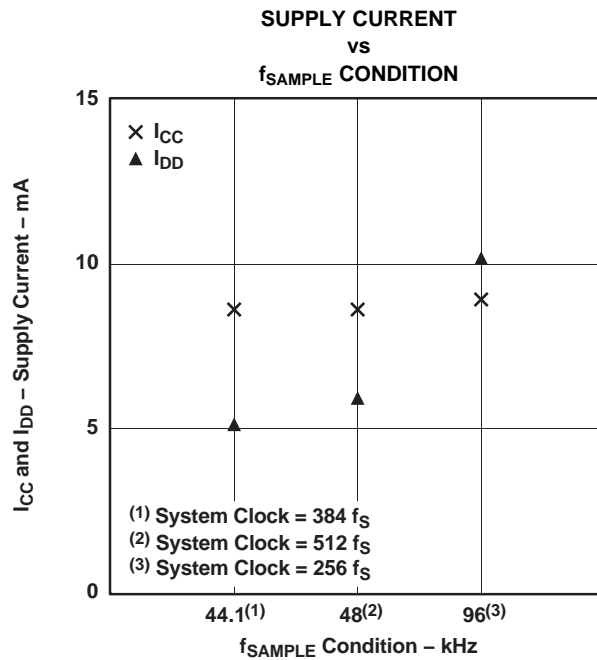


**Figure 7.**

DYNAMIC RANGE AND SNR
vs
TEMPERATURE



**Figure 8.**

THD + N
vs
SUPPLY VOLTAGE



**Figure 9.**

DYNAMIC RANGE AND SNR
vs
SUPPLY VOLTAGE



**Figure 10.**

## TYPICAL PERFORMANCE CURVES (Continued)

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted.



Figure 11.
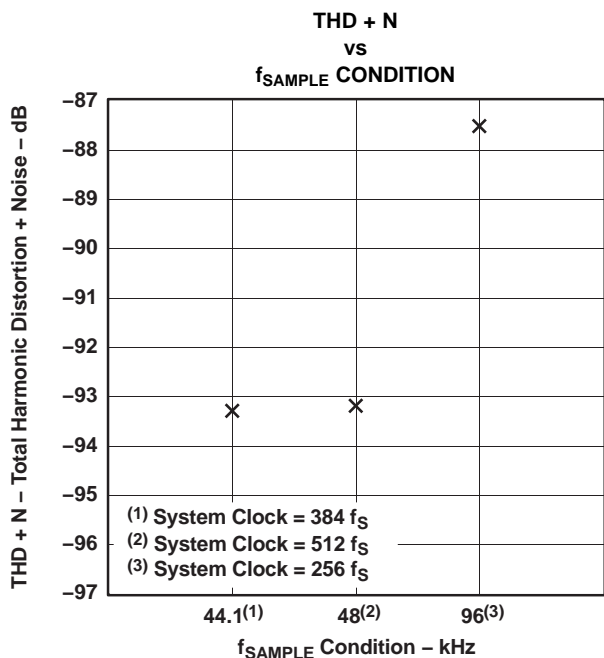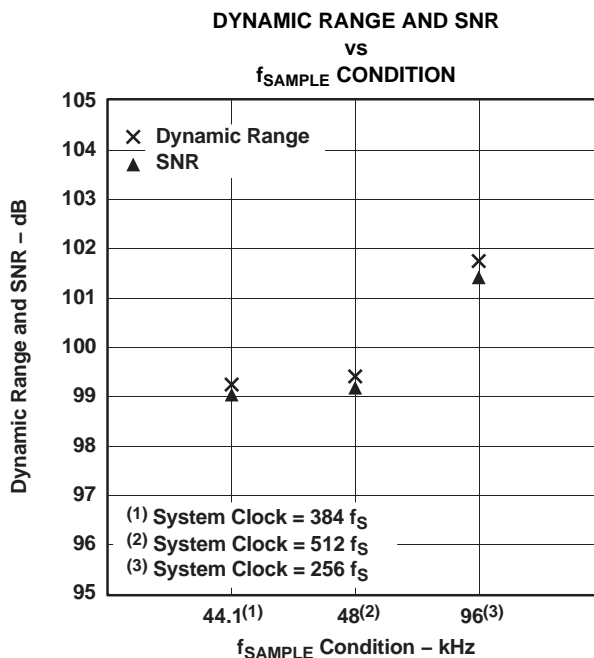


Figure 12.

## OUTPUT SPECTRUM
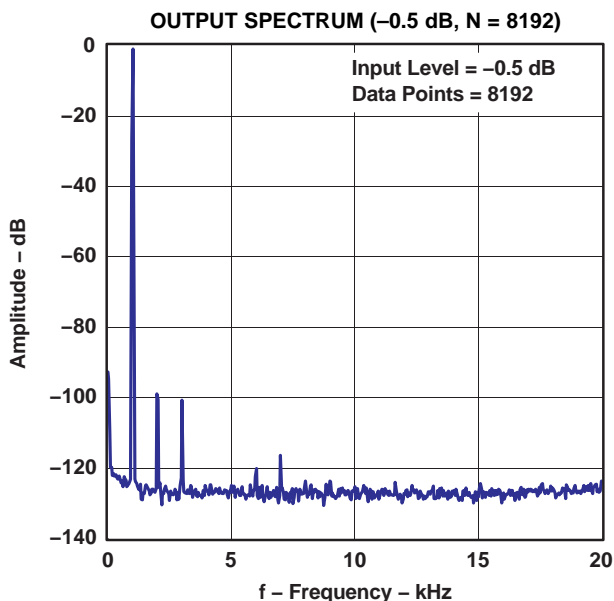


Figure 13.
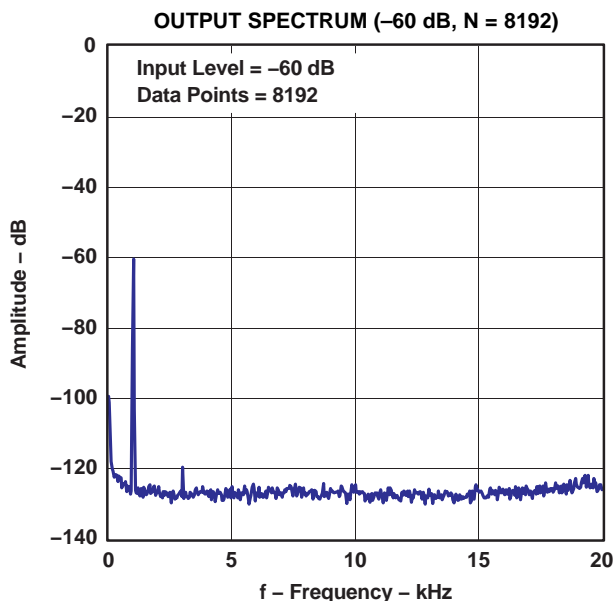


Figure 14.

## TYPICAL PERFORMANCE CURVES (Continued)

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $V_{DD}$ = 3.3 V, master mode, $f_S$ = 48 kHz, system clock = 512 $f_S$, 24-bit data, unless otherwise noted.

## OUTPUT SPECTRUM (Continued)
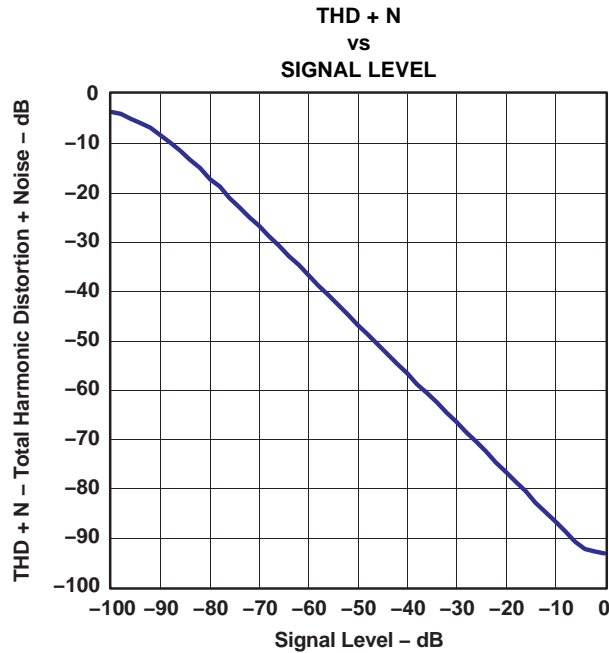


**Figure 15.**

## SUPPLY CURRENT



**Figure 16.**

## SYSTEM CLOCK

The PCM1808-Q1 supports 256 $f_S$, 384 $f_S$ and 512 $f_S$ as system clock, where $f_S$ is the audio sampling frequency. The system clock must be supplied on SCKI (pin 6).

The PCM1808-Q1 has a system clock detection circuit which automatically senses if the system clock is operating at 256 $f_S$, 384 $f_S$, or 512 $f_S$ in slave mode. In master mode, the system clock frequency must be controlled through the serial control port, which uses MD1 (pin 111) and MD0 (pin 10). The system clock is divided down automatically to generate frequencies of 128 $f_S$ and 64 $f_S$, which are used to operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 17 shows system clock timing.

**Table 1. Sampling Frequency and System Clock Frequency**

| SAMPLING FREQUENCY (kHz) | SYSTEM CLOCK FREQUENCY ($f_{SCLK}$) (MHz) | | |
|---|---|---|---|
| | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ |
| 8 | 2.048 | 3.072 | 4.096 |
| 16 | 4.096 | 6.144 | 8.192 |
| 32 | 8.192 | 12.288 | 16.384 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 |
| 48 | 12.288 | 18.432 | 24.576 |
| 64 | 16.384 | 24.576 | 32.768 |
| 88.2 | 22.5792 | 33.8688 | 45.1584 |
| 96 | 24.576 | 36.864 | 49.152 |



| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{w(SCKH)}$ | System clock pulse duration, HIGH | 8 | | ns |
| $t_{w(SCKL)}$ | System clock pulse duration, LOW | 8 | | ns |
| | System clock duty cycle | 40% | 60% | |
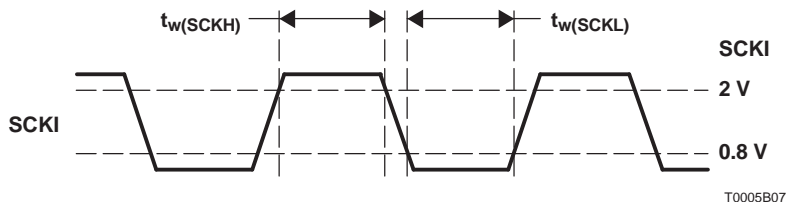
**Figure 17. System Clock Timing**

## FADE-IN AND FADE-OUT FUNCTIONS

The PCM1808-Q1 has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. The level changes from 0 dB to mute or mute to 0 dB are performed using calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade in and fade out depends on the analog input frequency ($f_{in}$). It takes $48/f_{in}$ until processing is completed. If there is no zero cross during $8192/f_S$, DOUT is faded in or out by force during $48/f_S$ (TIME OUT). Figure 18 illustrates the fade-in and fade-out operation processing.
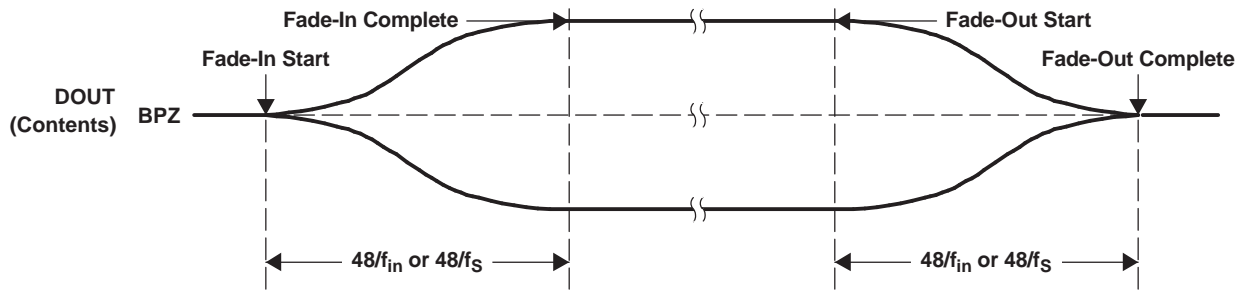
**Figure 18. Fade-In and Fade-Out Operations**

## POWER ON

The PCM1808-Q1 has an internal power-on-reset circuit, and initialization (reset) is performed automatically when the power supply ($V_{DD}$) exceeds 2.2 V (typical). While $V_{DD} < 2.2$ V (typical), and for 1024 system-clock counts after $V_{DD} > 2.2$ V (typical), the PCM1808-Q1 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of $8960/f_S$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_S$ until the data corresponding to the analog input signal is obtained. Figure 19 illustrates the power-on timing and the digital output.
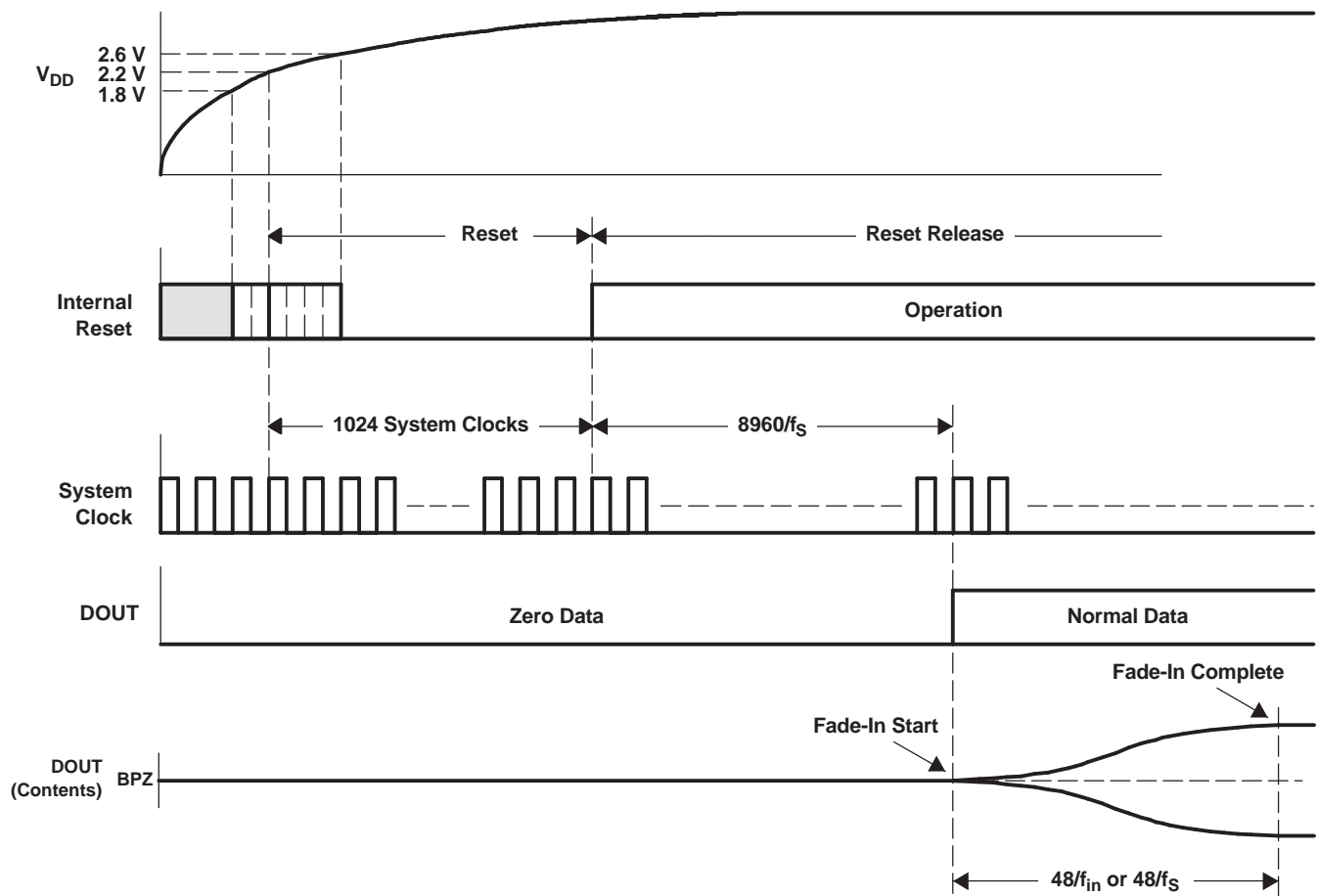


**Figure 19. Power-On Timing**

## CLOCK-HALT POWER-DOWN AND RESET FUNCTION

The PCM1808-Q1 has a power-down and reset function, which is triggered by halting SCKI (pin 6) in both master and slave modes. The function is available anytime after power on. Reset and power down are performed automatically 4 µs (minimum) after SCKI is halted. While the clock-halt reset is asserted, the PCM1808-Q1 stays in the reset and power-down mode, and DOUT (pin 9) is forced to zero. SCKI must be supplied to release the reset and power-down mode. The digital output is valid after the reset state is released and the time of 1024 SCKI + $8960/f_S$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_S$ until the level corresponding to the analog input signal is obtained. Figure 20 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) are required to synchronize with SCKI within $4480/f_S$ after SCKI is resumed. If it takes more than $4480/f_S$ for BCK and LRCK to synchronize with SCKI, SCKI should be masked until the synchronization is achieved again, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 26.

To avoid ADC performance degradation, the clock-halt reset also should be asserted when system clock SCKIor the audio interface clocks BCK and LRCK (sampling rate $f_S$) are changed on the fly.
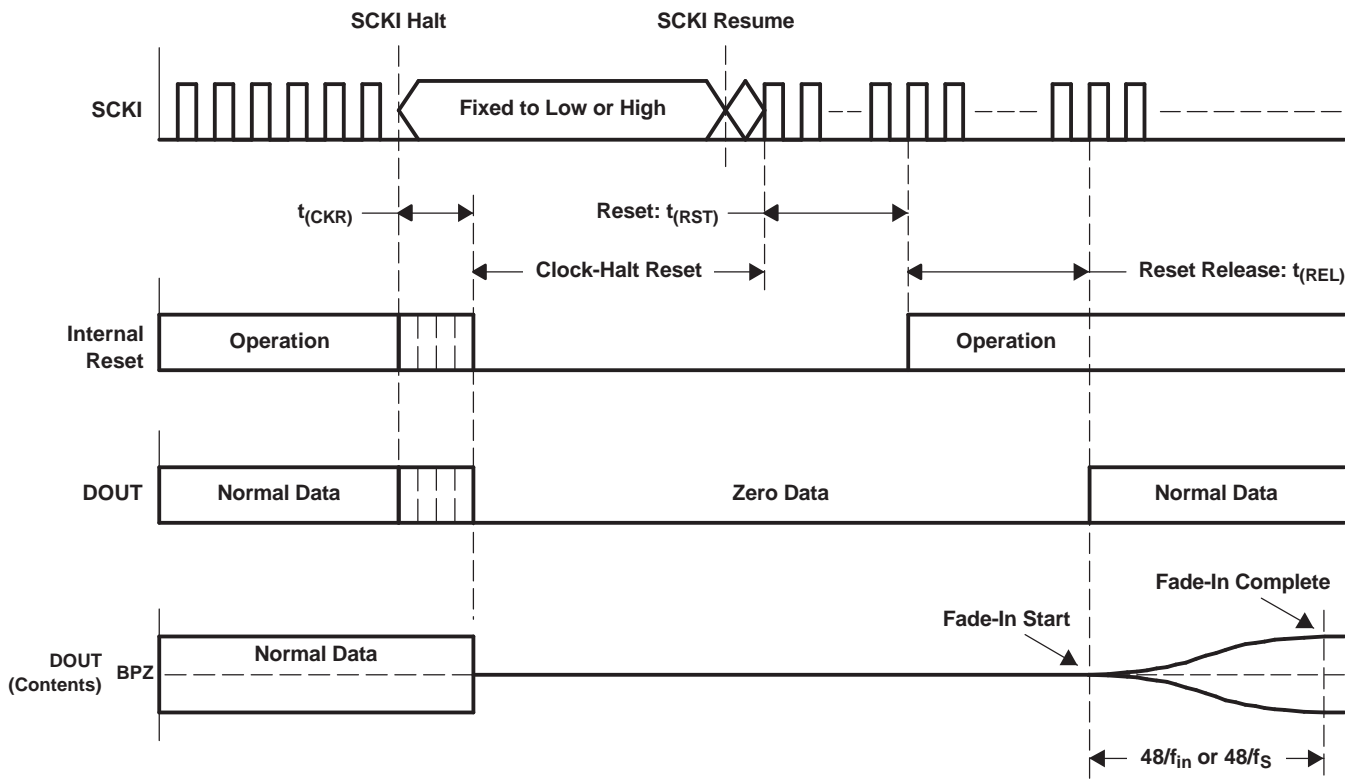


T0081-01

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|-----------|-----|-----|------|
| $t_{(CKR)}$ | Delay time from SCKI halt to internal reset | 4 | | µs |
| $t_{(RST)}$ | Delay time from SCKI resume to reset release | | 1024 SCKI | µs |
| $t_{(REL)}$ | Delay time from reset release to DOUT output | | $8960/f_S$ | µs |

**Figure 20. Clock-Halt Power-Down and Reset Timing**

## SERIAL AUDIO DATA INTERFACE

The PCM1808-Q1 interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

### INTERFACE MODE

The PCM1808-Q1 supports master mode and slave mode as interface modes, which are selected by MD1 (pin 11) and MD0 (pin 10), as shown in Table 2. MD1 and MD0 must be set prior to power on.

In master mode, the PCM1808-Q1 provides the timing of serial audio data communications between the PCM1808-Q1 and the digital audio processor or external circuit. While in slave mode, the PCM1808-Q1 receives the timing for data transfer from an external controller.

**Table 2. Interface Modes**

| MD1 (Pin 11) | MD0 (Pin 10) | INTERFACE MODE |
|---|---|---|
| Low | Low | Slave mode (256 $f_S$, 384 $f_S$, 512 $f_S$ autodetection) |
| Low | High | Master mode (512 $f_S$) |
| High | Low | Master mode (384 $f_S$) |
| High | High | Master mode (256 $f_S$) |

#### *Master mode*

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing which is generated in the clock circuit of the PCM1808-Q1. The frequency of BCK is fixed at 64 BCK/frame.

#### *Slave mode*

In slave mode, BCK and LRCK work as input pins. The PCM1808-Q1 accepts 64-BCK/frame or 48-BCK/frame format (only for a 384-$f_S$ system clock), not 32-BCK/frame format.

### DATA FORMAT

The PCM1808-Q1 supports two audio data formats in both master and slave modes. The data formats are selected by FMT (pin 12), as shown in Table 3. Figure 21 illustrates the data formats in slave mode and master mode.

**Table 3. Data Format**

| FORMAT NO. | FMT (Pin 12) | FORMAT |
|---|---|---|
| 0 | Low | I$^2$S, 24-bit |
| 1 | High | Left-justified, 24-bit |

**FORMAT 0: FMT = LOW**

24-Bit, MSB-First, I²S
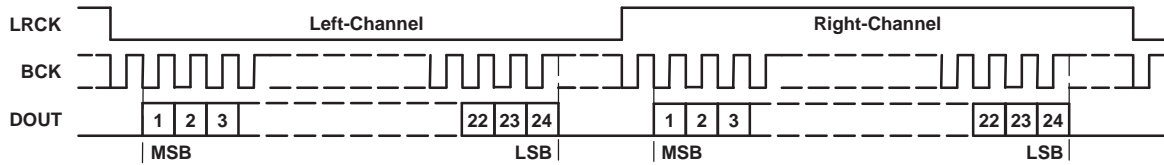


**FORMAT 1: FMT = HIGH**
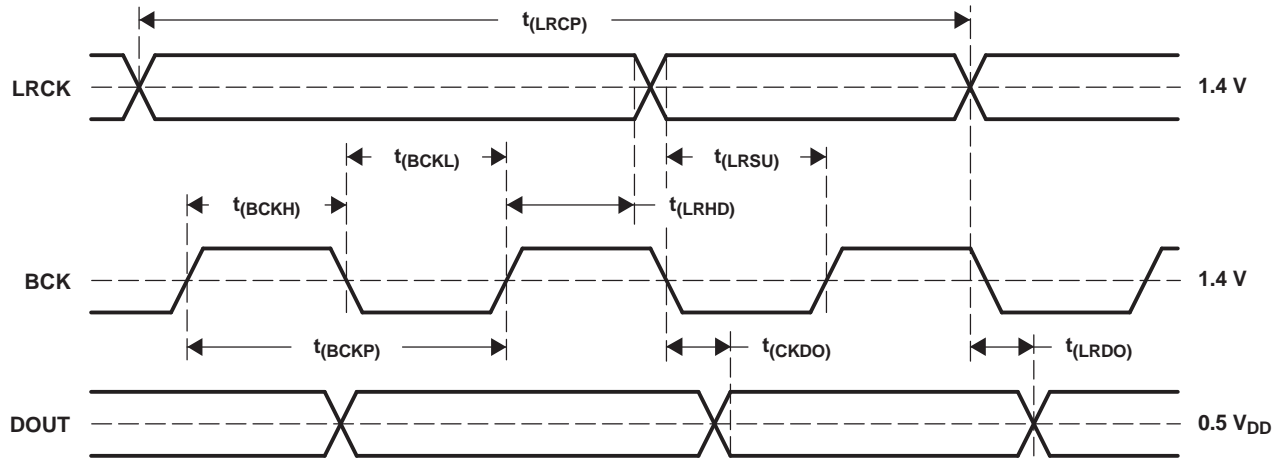
24-Bit, MSB-First, Left-Justified
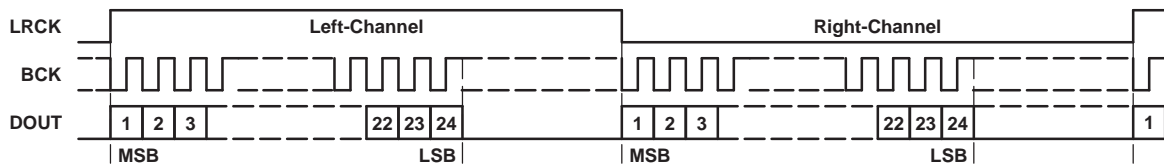


T0016-17

**Figure 21.  Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode
and as Outputs in Master Mode)**

## INTERFACE TIMING

Figure 22 and Figure 23 illustrate the interface timing in slave mode and master mode, respectively.
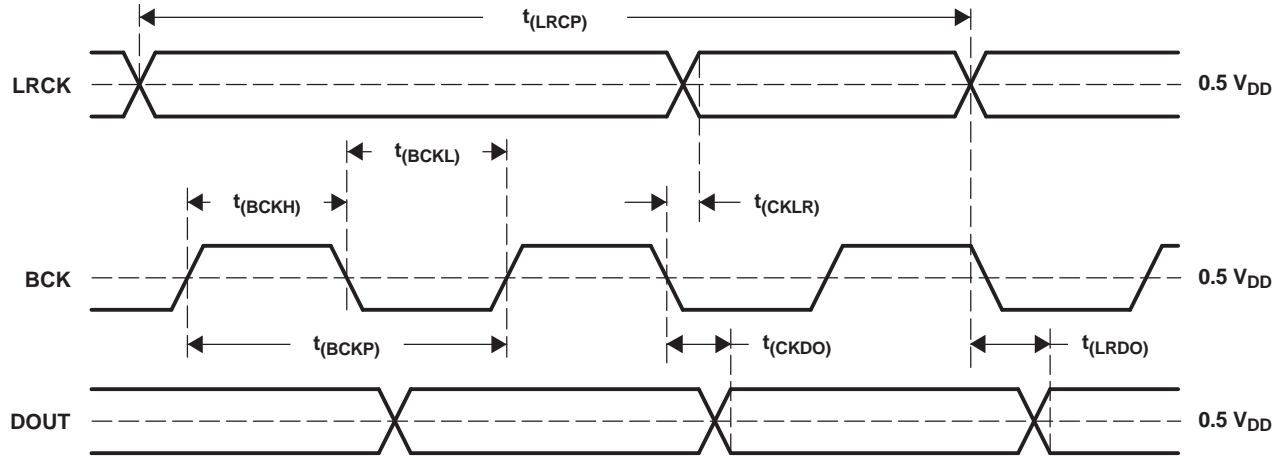


| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(BCKP)}$ | BCK period | $1/(64 f_S)$ | | | ns |
| $t_{(BCKH)}$ | BCK pulse duration, HIGH | $1.5 \times t_{(SCKI)}$ | | | ns |
| $t_{(BCKL)}$ | BCK pulse duration, LOW | $1.5 \times t_{(SCKI)}$ | | | ns |
| $t_{(LRSU)}$ | LRCK setup time to BCK rising edge | 50 | | | ns |
| $t_{(LRHD)}$ | LRCK hold time to BCK rising edge | 10 | | | ns |
| $t_{(LRCP)}$ | LRCK period | 10 | | | μs |
| $t_{(CKDO)}$ | Delay time, BCK falling edge to DOUT valid | −10 | | 40 | ns |
| $t_{(LRDO)}$ | Delay time, LRCK edge to DOUT valid | −10 | | 40 | ns |
| $t_r$ | Rise time of all signals | | | 20 | ns |
| $t_f$ | Fall time of all signals | | | 20 | ns |

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 $V_{DD}$ for output. Rise and fall times are from 10% to 90% of the input/output signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ is the SCKI period.

**Figure 22. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|-----------|-----|-----|-----|------|
| $t_{(BCKP)}$ | BCK period | 150 | $1/(64 f_S)$ | 2000 | ns |
| $t_{(BCKH)}$ | BCK pulse duration, HIGH | 65 | | 1200 | ns |
| $t_{(BCKL)}$ | BCK pulse duration, LOW | 65 | | 1200 | ns |
| $t_{(CKLR)}$ | Delay time, BCK falling edge to LRCK valid | −10 | | 20 | ns |
| $t_{(LRCP)}$ | LRCK period | 10 | $1/f_S$ | 125 | µs |
| $t_{(CKDO)}$ | Delay time, BCK falling edge to DOUT valid | −10 | | 20 | ns |
| $t_{(LRDO)}$ | Delay time, LRCK edge to DOUT valid | −10 | | 20 | ns |
| $t_r$ | Rise time of all signals | | | 20 | ns |
| $t_f$ | Fall time of all signals | | | 20 | ns |

NOTE:  Timing measurement reference level is 0.5 $V_{DD}$. Rise and fall times are from 10% to 90% of the input/output signal swing. Load capacitance of all signals is 20 pF.

**Figure 23.  Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)**
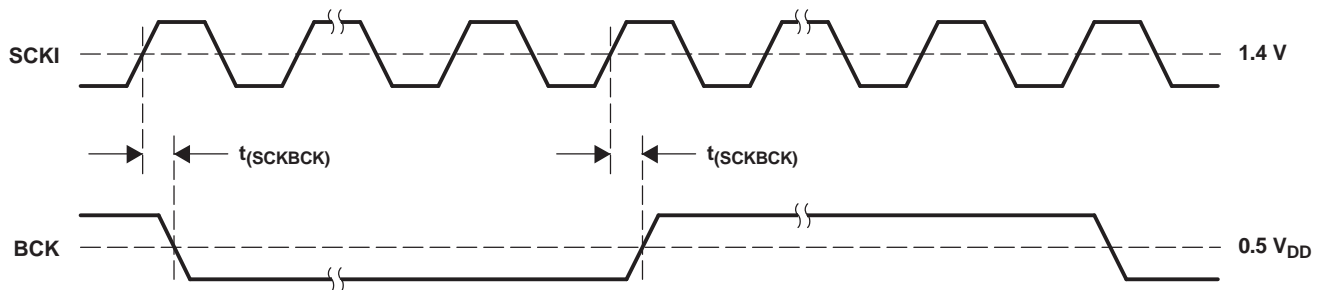


| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|-----------|-----|-----|-----|------|
| $t_{(SCKBCK)}$ | Delay time, SCKI rising edge to BCK edge | 5 | | 30 | ns |

NOTE:  Timing measurement reference level is 1.4 V for input and 0.5 $V_{DD}$ for output. Load capacitance of BCK is 20 pF. This timing is applied when SCKI frequency is less than 25 MHz.

**Figure 24.  Audio Clock Interface Timing (Master Mode: BCK Works as Output)**

## SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1808-Q1 operates under LRCK (pin 7), synchronized with system clock SCKI (pin 6). The PCM1808-Q1 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced to zero data (BPZ code) until resynchronization between LRCK and SCKI is established.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 25 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1808-Q1 can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in the audio signal. The digital output is valid after resynchronization completes and the time of $32/f_S$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_S$ until the level corresponding to the analog input signal is obtained. If synchronization is lost during the fade-in or fade-out operation, the operation stops and DOUT (pin 9) is forced to zero data immediately. The fade-in operation resumes from mute after the time of $32/f_S$ following resynchronization.
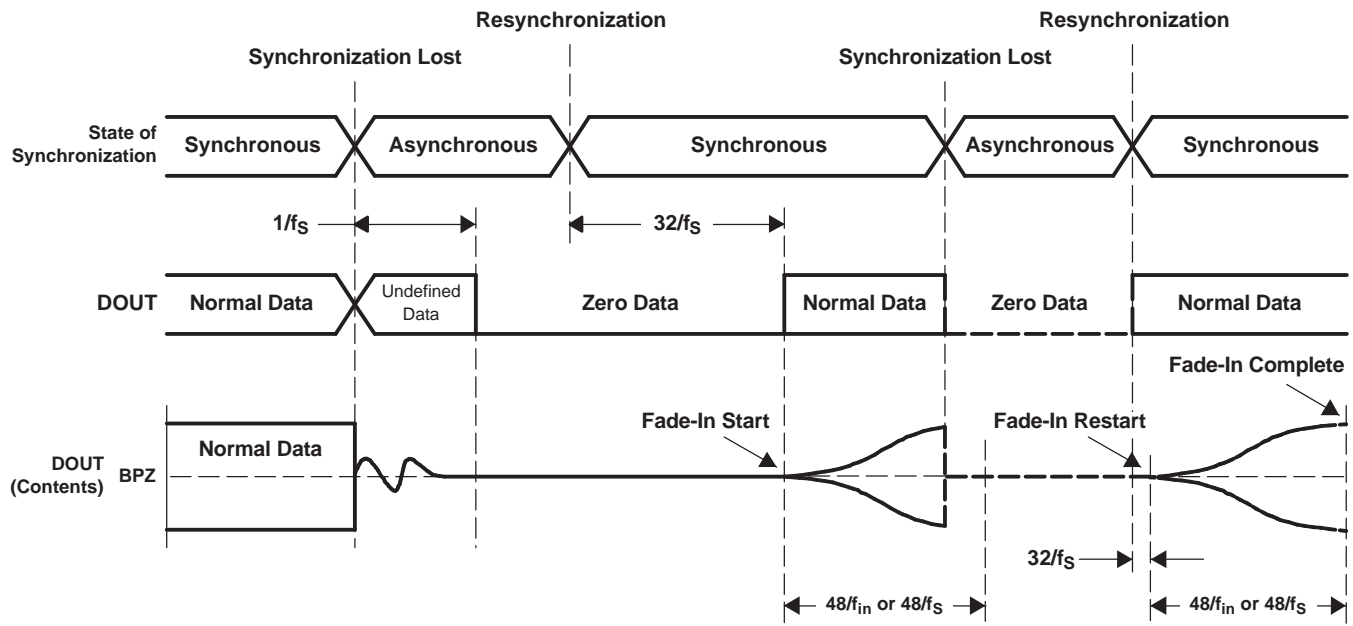


**Figure 25. ADC Digital Output for Loss of Synchronization and Resynchronization**

## APPLICATION INFORMATION

### TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 26 is a typical circuit connection diagram. The antialiasing low-pass filters are integrated on the analog inputs, $V_{IN}L$ and $V_{IN}R$. If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are needed. A passive RC filter (100 Ω and 0.01 µF to 1 kΩ and 1000 pF) generally is used.
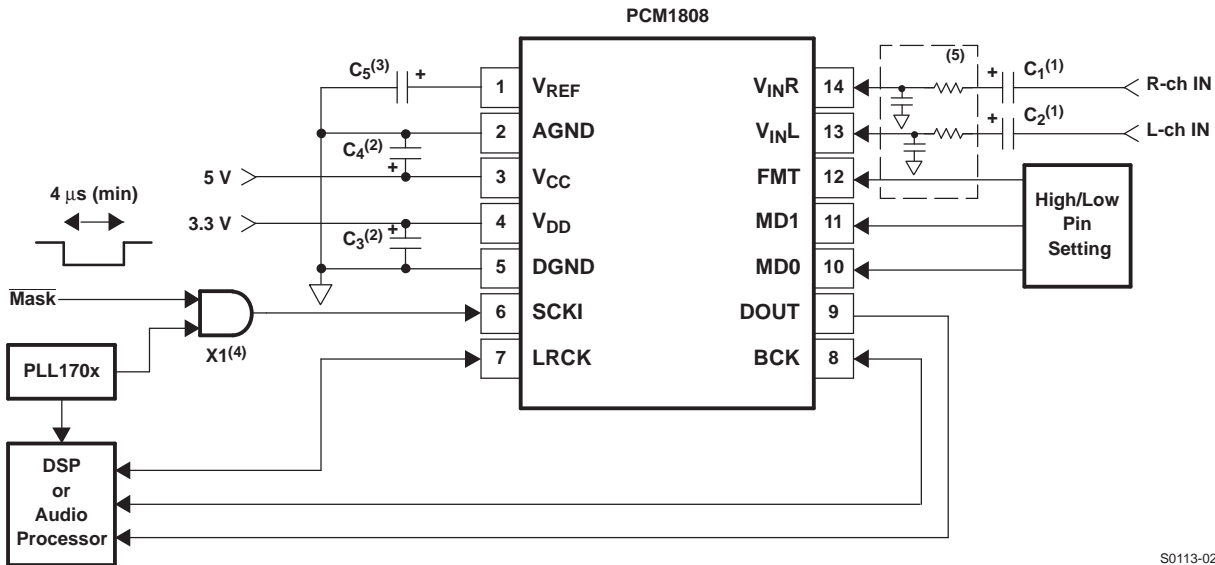


(1)   C1, C2: A 1-µF electrolytic capacitor gives 2.7 Hz (τ = 1 µF × 60 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.

(2)   C3, C4: Bypass capacitors, 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply

(3)   C5: 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended.

(4)   X1: X1 masks the system clock input when using the clock-halt reset function with external control.

(5)   Optional external antialiasing filter could be required, depending on the application.

**Figure 26.  Typical Circuit Connection Diagram**

### BOARD DESIGN AND LAYOUT CONSIDERATIONS

#### $V_{CC}$, $V_{DD}$ PINS

The digital and analog power supply lines to the PCM1808-Q1 should be bypassed to the corresponding ground pins with both 0.1-µF ceramic and 10-µF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

#### AGND, DGND PINS

To maximize the dynamic performance of the PCM1808-Q1, the analog and digital grounds are not internally connected. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1808-Q1 package to reduce potential noise problems.

#### $V_{IN}L$, $V_{IN}R$ PINS

$V_{IN}L$ and $V_{IN}R$ are single-ended inputs. The antialias low-pass filters are integrated on these inputs to remove the high-frequency noise outside the audio band. If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are required. A passive RC filter (100 Ω and 0.01 µF to 1 kΩ and 1000 pF) is generally used.

**V$_{REF}$ PIN**

To ensure low source impedance of the ADC references, 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended between V$_{REF}$ and AGND. These capacitors should be located as close as possible to the V$_{REF}$ pin to reduce dynamic errors on the ADC references.

**DOUT PIN**

The DOUT pin has a large load-drive capability, but if the DOUT line is long, locating a buffer near the PCM1808-Q1 and minimizing load capacitance is recommended to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

**SYSTEM CLOCK**

The quality of the system clock can influence dynamic performance, as the PCM1808-Q1 operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

# REVISION HISTORY

**Changes from Original (March, 2011) to Revision A**                                              **Page**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1808QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | P1808Q | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF PCM1808-Q1 :**

• Catalog: PCM1808

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1808QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| PCM1808QPWRQ1 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

PW (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

0,65        0,30
            0,19          ⊕ | 0,10 Ⓜ

14                8

          4,50    6,60
     D    4,30    6,20

1           7

     5,10
     4,90
     ⟋C⟍

0,15 NOM

Gage Plane

0°−8°              0,25

                   0,75
                   0,50

1,20 MAX      0,15
              0,05

Seating Plane

◁ | 0,10
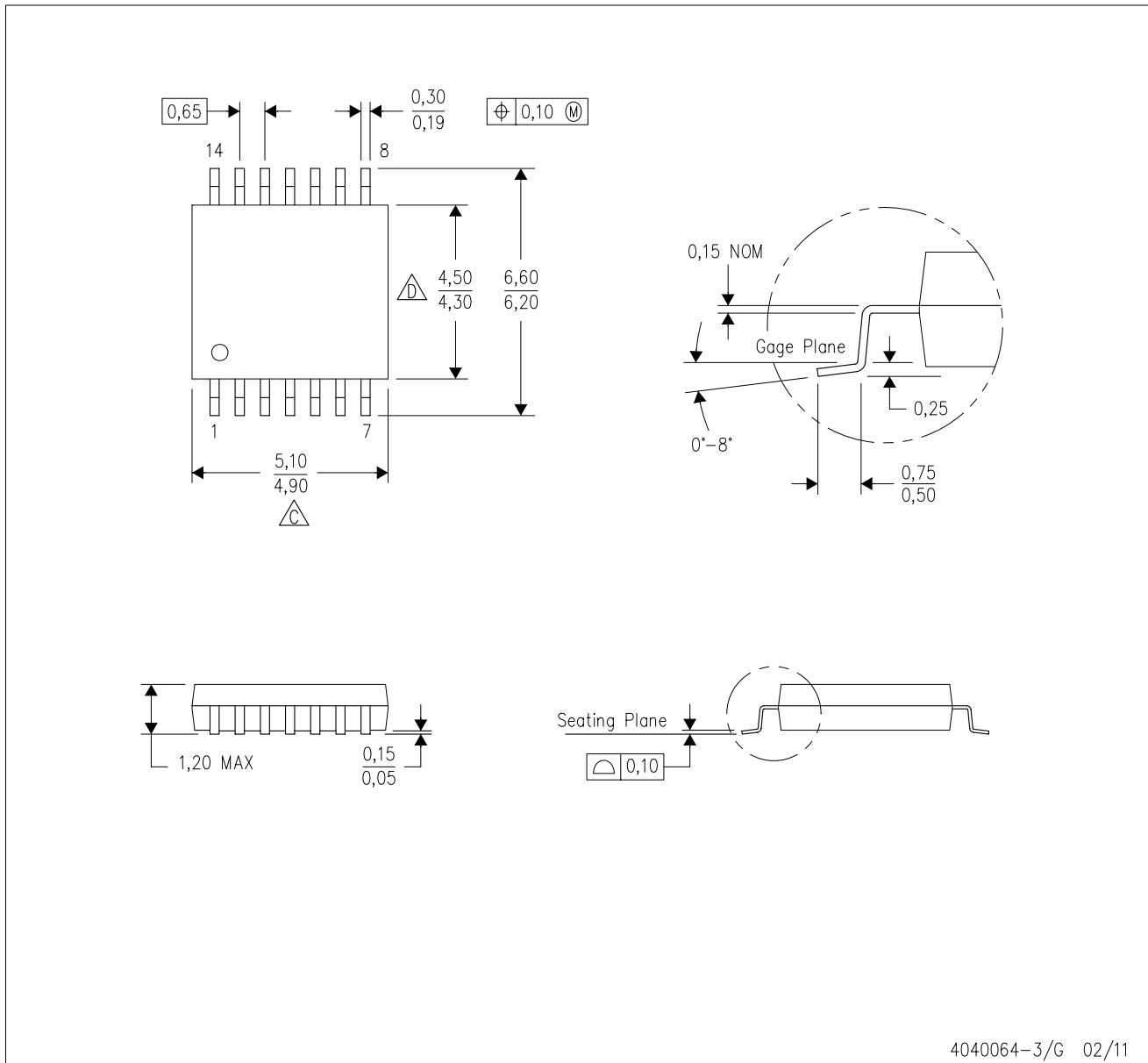
4040064−3/G   02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         ⟋C⟍  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         ⟋D⟍  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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## PW (R−PDSO−G14)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x0,65

14x0,30

12x0,65

14x1,55

5,60

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284−2/G   08/15

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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