PRELIMINARY DATASHEET

CGY2122XUH/C2

25-43 GHz Ultra Low Noise Amplifier

DESCRIPTION

The CGY2122XUH is a high performance GaAs Low Noise Amplifier MMIC designed to operate in the Ka Band.

The CGY2122XUH has an exceptionally low noise figure of 1.5dB and 32dB of gain over the whole 25-43 GHz frequency band. The on chip matching provides 8 dB of Input Return Loss and Output Return Loss over the frequency range. It can be used in Radar, Telecommunication and instrumentation applications.

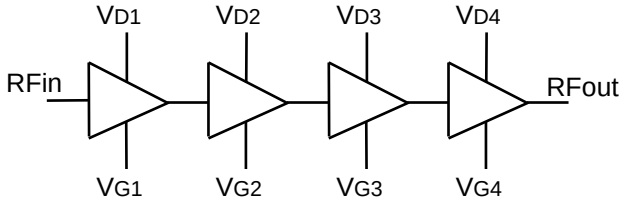
The die is manufactured using OMMIC's advanced 70nm gate length high indium contain MHEMT technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability.

APPLICATIONS

- Radar
- Telecommunications
- Instrumentation
- SATCOM

FEATURES

- Operating frequency range : 25 to 43 GHz
- Noise Figure : 1.5 dB from 25 to 43 GHz
- Gain : 32dB
- Input Return Loss : > 8 dB
- Output Return Loss : > 8 dB
- Power Supply : 30 mA at 1.1V
- Die size = 3 x 2 mm
- Tested, Inspected Known Good Die (KGD)
- Demonstration Boards available



CGY2122X Ultra Low Noise Amplifier Bloc diagram

RoHS Compliant

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MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1}, V_{G2}, V_{G3}, V_{G4}	Gate voltage		- 2.5	0	V
V_{D1}, V_{D2}, V_{D3}, V_{D4}	Drain voltage		0	1.2	V
I_{D1}, I_{D2}, I_{D3} I_{D4}	Drain current			50	mA
I_{G1}, I_{G2}, I_{G3}, I_{G4}	Gate Current		- 1	+ 1	mA
P_{IN}	RF Input power			+ 1	dBm
T_{amb}	Ambient temperature		- 40	+ 85	° C
T_j	Junction temperature			+ 175	° C
T_{stg}	Storage temperature		- 55	+ 85	° C

Operation of this device outside the parameter ranges given above may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j\ -\ amb)}$	Thermal resistance from junction to ambient (DC power at T_{amb} max)	TBD	° C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, $V_{D1,}$ $V_{D2,}$ $V_{D3,}$ V_{D4} = 1,1V, $I_{D1,}$ $I_{D2,}$ $I_{D3,}$ I_{D4} = 7.5 mA, unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RFin	Input frequency		25		43	GHz
Performances on Reference Board at f_i = 29 GHz						
$V_{D1,2,3,4}$	Drain Supply voltage			+ 1.1		V
$I_{D1,2,3,4}$	Total supply current	$V_{D1,2,3,4}$ = 1.1 V		30		mA
G	Gain			32		dB
NFmin	Minimum Noise Figure	@32GHz	1.2			dB
NF	Noise Figure			1.5		dB
P1dB	1dB compression point			1.2		dBm
OIP3	Output third order intercept point			10		dBm
ISO_{rev}	Reverse Isolation	RF_{OUT}/RF_{IN}		-50		dB
S_{11}	Input reflection coefficient	50 Ohms			-8	dB
S_{22}	Output reflection coefficient	50 Ohms			-8	dB

(*) Measurement reference planes are the INPUT and OUTPUT plans of the CGY2122XUH MMIC.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

S-PARAMETERS

Conditions : V_{D1}, V_{D2}, V_{D3}, V_{D4} = 1.1V, I_{D1}, I_{D2}, I_{D3}, I_{D4} = 7.5 mA, T_{amb} = + 25°C

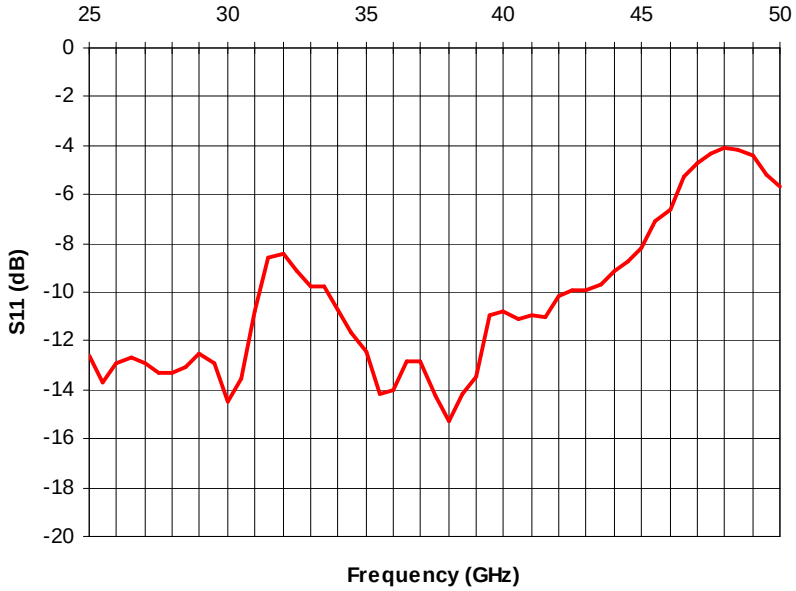

Figure 1 : S11 vs Frequency measurements

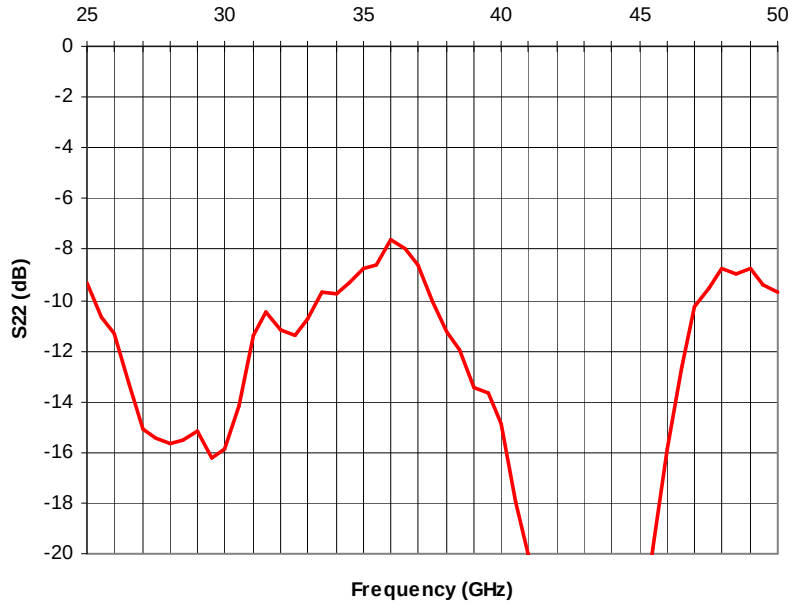

Figure 2 : S22 vs Frequency measurements

S-PARAMETERS

Conditions : V_{D1}, V_{D2}, V_{D3}, V_{D4} = 1.1V, I_{D1}, I_{D2}, I_{D3}, I_{D4} = 7.5 mA, T_{amb} = + 25°C

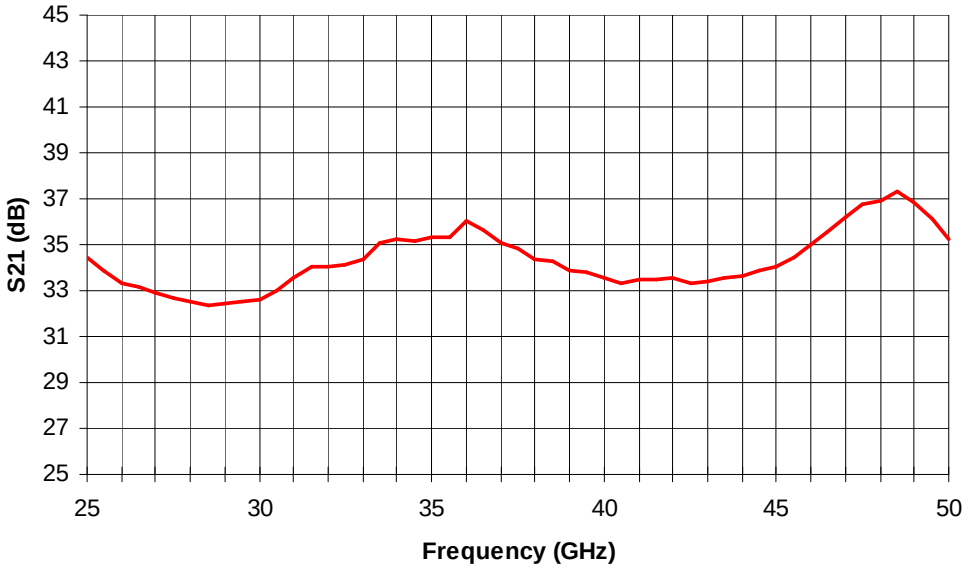

Figure 3 : Gain vs Frequency measurements

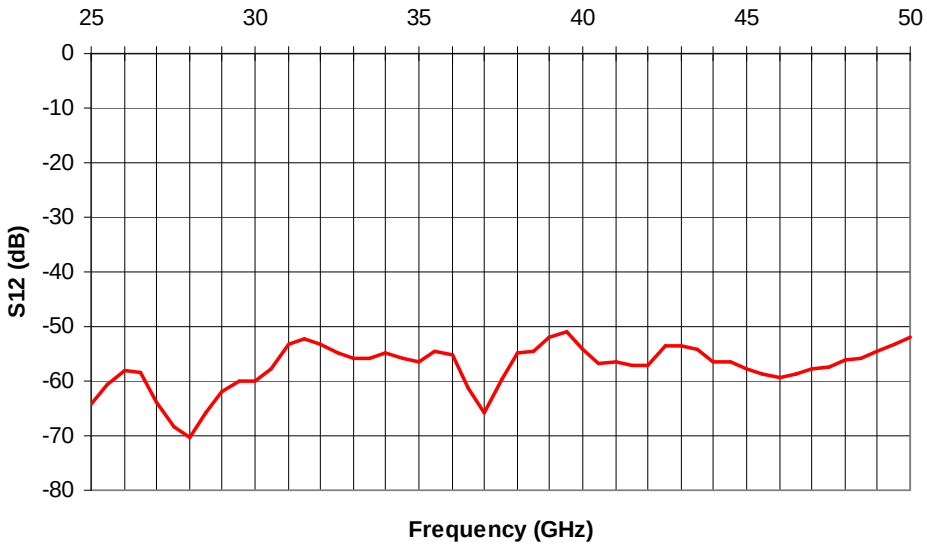

Figure 4 : Reverse isolation vs Frequency measurements

S PARAMETERS

Conditions : $V_{D1}, V_{D2}, V_{D3}, V_{D4}$ = 1.1V, $I_{D1}, I_{D2}, I_{D3}, I_{D4}$ = 7.5 mA, T_{amb} = + 25°C

GHz	|S11|	S11 Phase	|S21|	S21 Phase	|S12|	S12 Phase	|S22|	S22 Phase
25	-12,61	-99,97	34,41	166	-64,07	71,82	-9,331	-71,86
25.5	-13,71	-89,22	33,85	150,9	-60,6	62,18	-10,68	-76,57
26	-12,89	-83,71	33,35	137,2	-57,98	25,43	-11,34	-81,71
26.5	-12,66	-87,62	33,18	123,2	-58,36	-25,14	-13,21	-89,22
27	-12,92	-89,35	32,92	108,7	-63,75	-73,89	-15,07	-82,32
27.5	-13,32	-90,94	32,65	94,77	-68,43	-105,4	-15,41	-78,69
28	-13,33	-88,29	32,5	81,99	-70,44	-129,5	-15,68	-74,86
28.5	-13,1	-86,26	32,37	69,29	-65,68	174,5	-15,5	-71,87
29	-12,5	-89,29	32,46	57,58	-61,84	99,02	-15,18	-74,38
29.5	-12,95	-94,62	32,55	44,72	-60	24,21	-16,22	-74,84
30	-14,48	-88,76	32,63	33,16	-60,1	-46,22	-15,86	-61,47
30.5	-13,56	-75,19	32,97	22,19	-57,73	-91,69	-14,14	-56,23
31	-10,77	-71,05	33,58	8,32	-53,33	-142,7	-11,4	-61,61
31.5	-8,622	-83,57	34,05	-7,907	-52,37	174,1	-10,48	-76,38
32	-8,411	-100,6	34,02	-22,77	-53,19	133,1	-11,18	-87,66
32.5	-9,131	-108,7	34,1	-35,78	-54,71	114,2	-11,4	-86,42
33	-9,764	-113,2	34,39	-48,26	-55,68	101,6	-10,72	-87,2
33.5	-9,791	-118,1	35,06	-62,61	-55,95	102,2	-9,654	-96,12
34	-10,72	-126,4	35,23	-80,49	-54,69	78,12	-9,737	-103,2
34.5	-11,66	-128,2	35,17	-94,46	-55,81	73,9	-9,297	-107,9
35	-12,44	-130,4	35,33	-109,5	-56,6	68,63	-8,766	-115,2
35.5	-14,21	-128,6	35,36	-123,2	-54,38	62,97	-8,609	-124,2
36	-14,02	-114,7	36,02	-138,5	-55,03	32,19	-7,586	-134,4
36.5	-12,84	-118,2	35,64	-157,6	-61,29	19,53	-7,97	-150
37	-12,81	-123,1	35,09	-172,6	-65,87	36,43	-8,634	-162,1
37.5	-14,28	-126	34,87	173,8	-59,63	95,17	-10,01	-173,3
38	-15,24	-113	34,37	161,6	-54,85	77,21	-11,21	-178,8
38.5	-14,18	-104,9	34,24	149,2	-54,65	58,92	-11,97	173,6
39	-13,47	-100,9	33,84	138,1	-52,07	50,62	-13,43	168
39.5	-10,92	-105,2	33,78	125,2	-50,86	19,52	-13,67	161,1
40	-10,79	-113,7	33,59	113,8	-54,31	1,232	-14,91	147,7
40.5	-11,14	-118,7	33,34	103,5	-56,63	-6,949	-17,92	136,5
41	-10,94	-117,2	33,49	91,21	-56,31	-0,6229	-20	136,6
41.5	-11,03	-117,3	33,46	80,28	-57,1	-1,053	-21,71	130,8
42	-10,18	-117,9	33,52	67,77	-57,03	-8,746	-23,36	135,4
42.5	-9,946	-121,7	33,29	55,48	-53,53	-8,549	-23,3	113,8
43	-9,906	-127,1	33,4	46,13	-53,55	-34,19	-25,83	83,56

S PARAMETERS

Conditions : V_{D1}, V_{D2}, V_{D3}, V_{D4} = 1.1V, I_{D1}, I_{D2}, I_{D3}, I_{D4} = 7.5 mA, T_{amb} = + 25°C

GHz	|S11|	S11 Phase	|S21|	S21 Phase	|S12|	S12 Phase	|S22|	S22 Phase
43	-9,906	-127,1	33,4	46,13	-53,55	-34,19	-25,83	83,56
43.5	-9,679	-124	33,53	34,34	-54,22	-53,61	-29,87	60,34
44	-9,162	-123,9	33,65	23,29	-56,49	-73,91	-25,79	22,41
44.5	-8,749	-125,7	33,86	11,91	-56,58	-89,48	-24,97	-11,72
45	-8,225	-124,3	34,05	0,7534	-57,86	-110,6	-23,55	-19,59
45.5	-7,125	-128,6	34,42	-10,96	-58,8	-145,9	-19,81	-22,81
46	-6,583	-132,8	34,96	-22,16	-59,42	-159	-15,84	-30,79
46.5	-5,305	-137,9	35,53	-36,3	-58,73	169,5	-12,64	-49,51
47	-4,723	-145	36,17	-49,62	-57,84	143,8	-10,27	-71,04
47.5	-4,302	-153,5	36,76	-66,73	-57,26	128,7	-9,519	-91,24
48	-4,087	-162,5	36,94	-83,22	-55,98	110,1	-8,777	-108,9
48.5	-4,185	-169,4	37,32	-101,5	-55,85	93,54	-8,954	-124,2
49	-4,42	179,6	36,82	-124,4	-54,37	86,84	-8,767	-137,8
49.5	-5,162	174,9	36,12	-137,8	-53,27	80,12	-9,365	-151,4
50	-5,678	167,7	35,21	-153,3	-51,9	70,97	-9,648	-160,4

NOISE

Conditions : V_{D1}, V_{D2}, V_{D3}, V_{D4} = 1.1V, I_{D1}, I_{D2}, I_{D3}, I_{D4} = 7.5 mA, T_{amb} = + 25°C

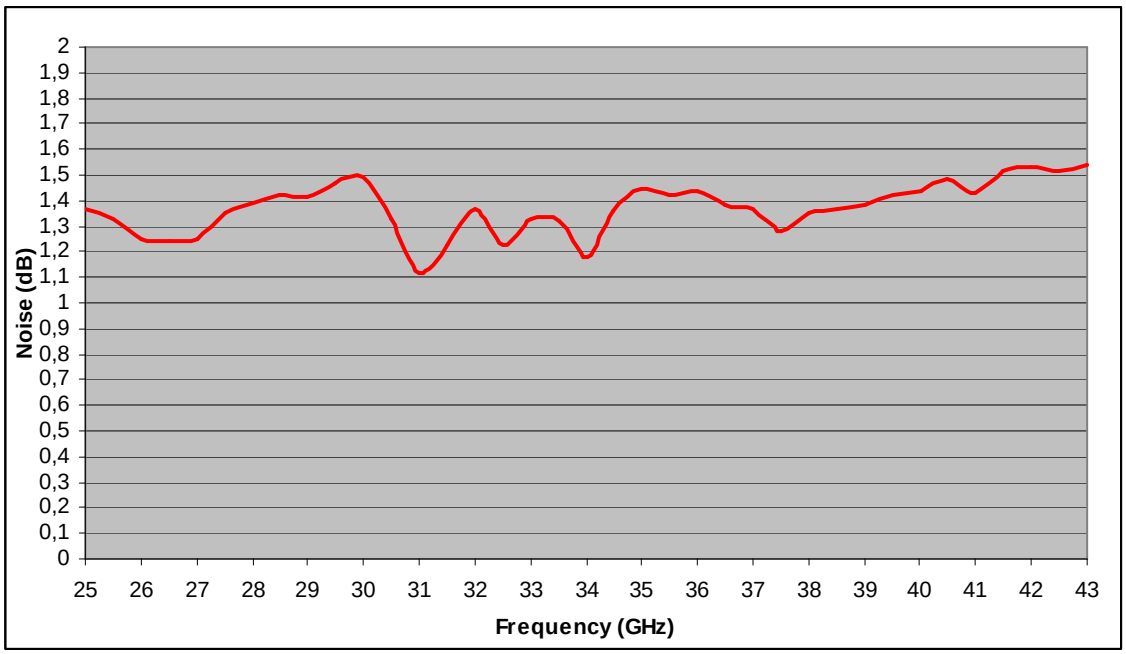

Figure 5 Noise Figure vs Frequency measurements

APPLICATION INFORMATION

Typical application scheme

A recommended module layout is proposed below. In the reference design, RF input and output are using coplanar transmission lines, microstrip transmission lines can also be used with similar performances. Due to the very high frequency, all path lengths and physical sizes of components should be minimized.

Both RF input and output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as short as possible to reduce parasitic inductance. Degradation of gain and match will be evident at higher RF input and output inductances. Ribbon bonding technique can also be used.

All others bonding inductances (pads V_{D1}, V_{D2}, V_{D3}, V_{D4}, and V_{G1}, V_{G2}, V_{G3}, V_{G4}) should be kept as short as possible.

Decoupling chip capacitors 47 pF and Surface Mount Devices capacitors of 100 nF can be used to improve the power supply rejection and prevent unwanted inside and outside bandpath oscillations.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is key to use an uninterrupted ground plane. AuSn solder or silver conductive epoxy material can be used for capacitors and die attach.

The reference board is using Southwest removable millimeter wave connectors.

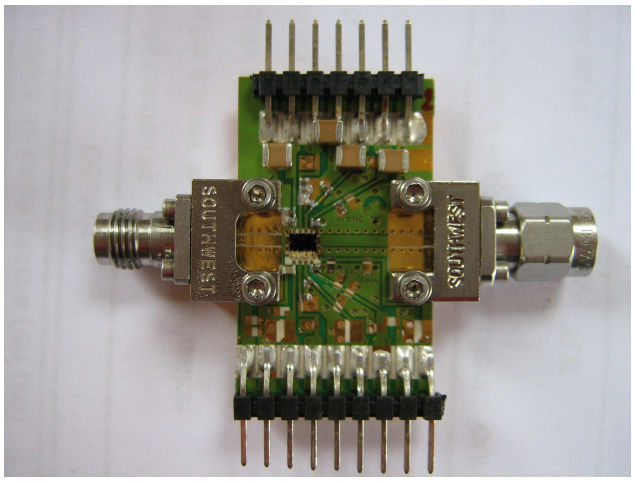

Figure 6 CGY2122X reference board

The layout of the decoupling capacitor are shown below, it can be noticed that drain and gates are carefully decoupled. Bondings between die pads and chip capacitors should be kept as short as possible reducing the equivalent inductance. A 47pF chip capacitor is connected to each DC pad, it is also recommended to insert a second row of 100 nF CMS capacitor in cascade on gates and drain supply connections.
The capacitors present on gates can form with a serie resistor a low-pass filter slowing down the activation in case of grid control.

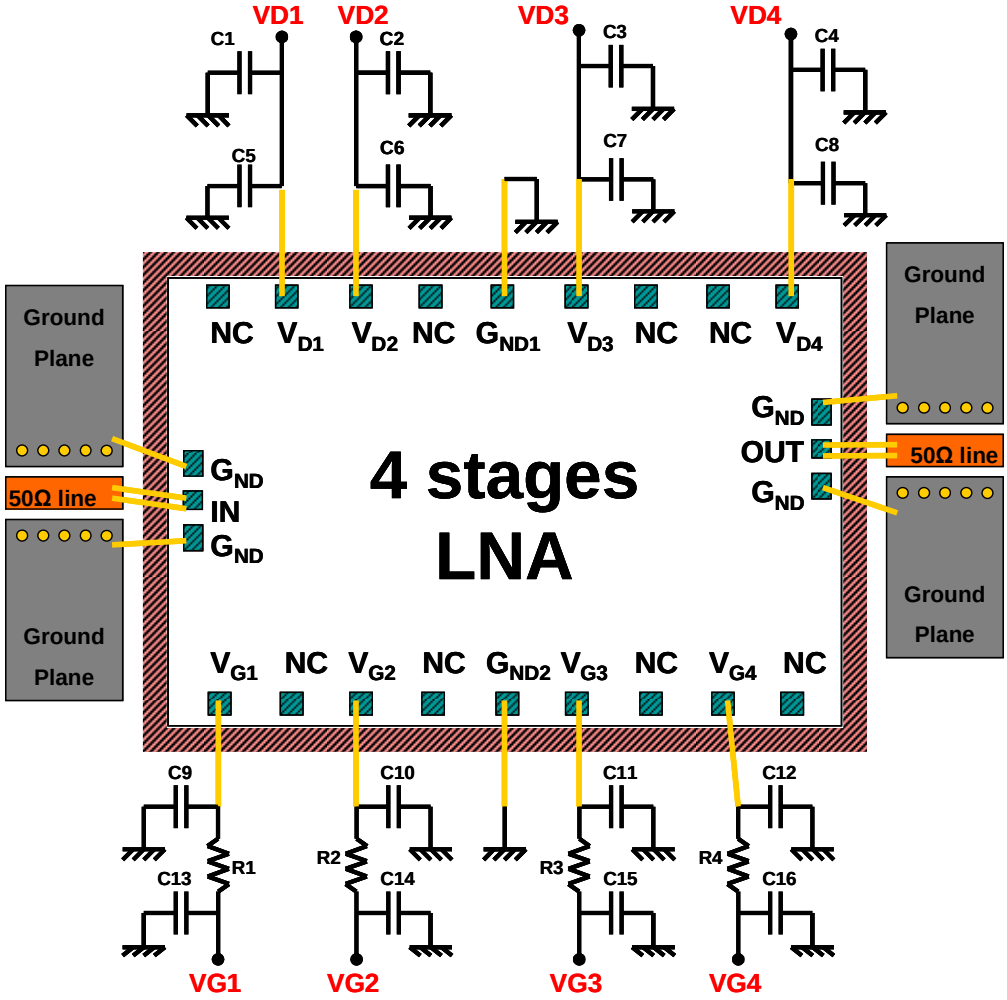

Figure 7 Typical application layout

BILL OF MATERIALS

COMPONENT	DESCRIPTION
C5, C6, C7, C8, C9, C10, C11, C12	47 pF Chip Capacitor
R1, R2, R3, R4	1 kΩ Resistor
C1, C2, C3, C4, C13, C14, C15, C16	100 nF SMD Capacitor

BONDINGS PAD COORDINATES

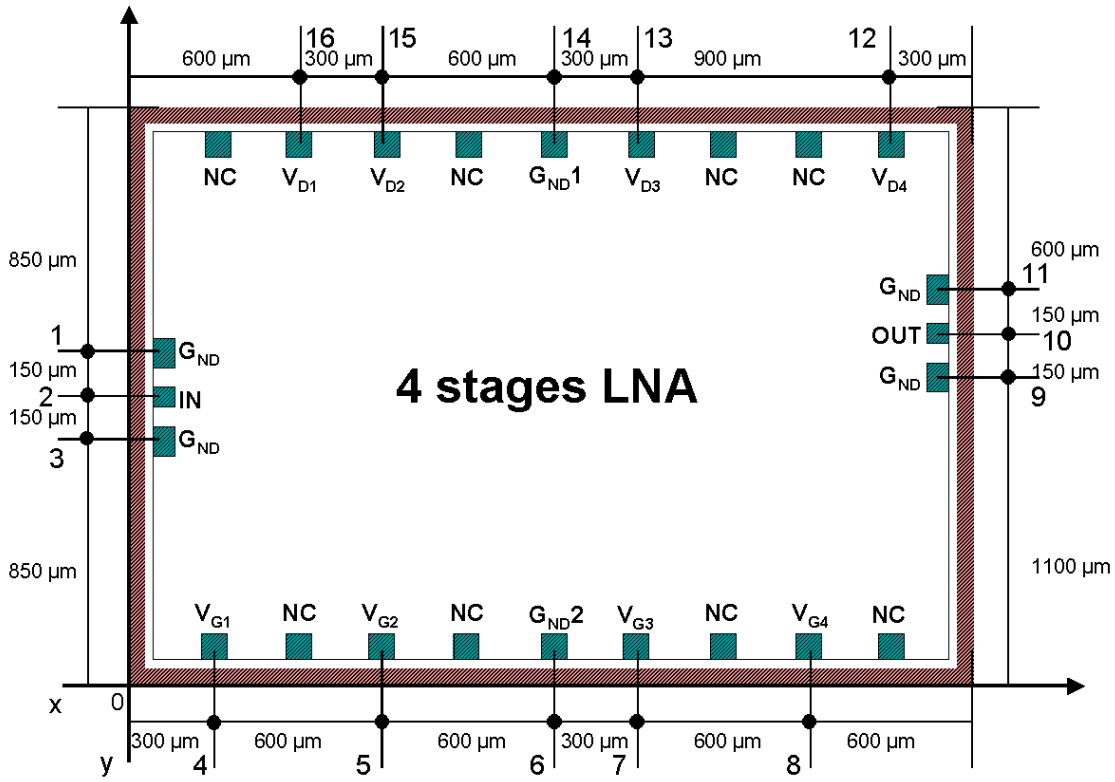

Figure 8 Bondings pad coordinates

PINOUT

The amplifier has a North and South face, North is top and South is Bottom when RF input is on the left and RF output on the right.

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD1	V_{D1}	First stage Drain
VD2	V_{D2}	Second stage Drain
VD3	V_{D3}	Third stage Drain
VD4	V_{D4}	Forth stage Drain
VG1	V_{G1}	First stage Gate
VG2	V_{G2}	Second stage Gate
VG3	V_{G3}	Third stage Gate
VG4	V_{G4}	Forth stage Gate

GND1	$G_{ND}1$	Ground
GND2	$G_{ND}2$	Ground
NC	NC	Unconnected pad
GND	BACKSIDE	Ground

Note :
In order to ensure good RF performances and stability It is key to connected to the ground the metalized backside of the die.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Package size (mm)
DIE	100% RF and DC on-wafer tested	10	-	3 x 2 x 0.1

SOLDERING

To avoid permanent damages or impact on reliability during soldering process, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400°C

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2122X	UH	C2	-	On-Wafer measured Die