L-Band 6-Bit Digital Phase Shifter

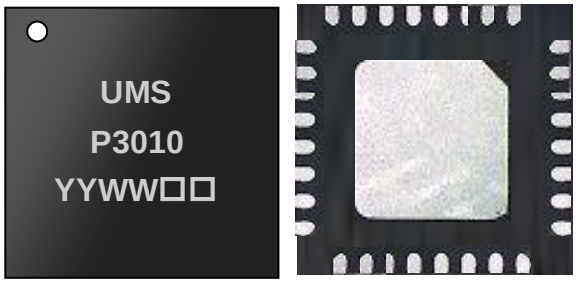
GaAs Monolithic Microwave IC in SMD leadless package

Description

CHP3010-QFG is an L-Band (1.2,1.4GHz) monolithic 6 bit digital phase-shifter with a 0-360° range and a high phase accuracy. The typical RMS phase error is 1.5°. The circuit provides 7dB insertion loss associated with input and output return losses better than 15dB under all logic states. An on-chip DC-interface is compatible with both CMOS (0/+3.3V) and TTL (0/+5V) logics.

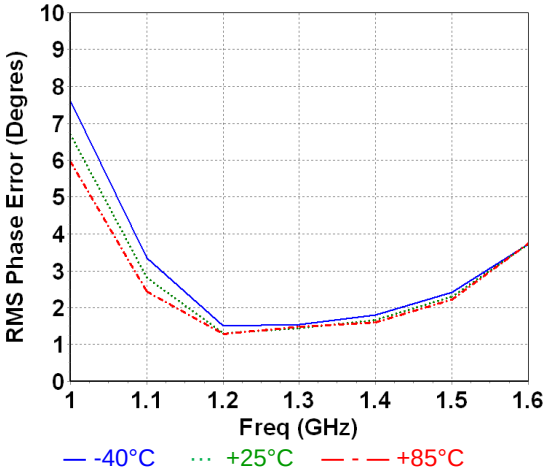
The circuit is mainly dedicated to defense and space systems and is also well suited for a wide range of microwave applications and systems.

The MMIC is developed on a robust 0.25µm gate length pHEMT process and is packaged in a standard surface mount 32-lead QFN5x5.



Main Features

- 1.5 deg RMS Phase error
- Low I/O return losses (all states)
- 24dBm Input P1dB
- 16dBm Output P1dB
- CMOS /TTL compatibility: V+=+3.3/5 Volt
- DC-decoupled I/O
- 32L-QFN5x5
- MSL2



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	1.2		1.4	GHz
PPE	Peak Phase Error		(-1,+3)		deg
RMS_PE	RMS Phase Error		1.5		deg
P1dB	Input power @ 1dBcomp (CW)		24		dBm

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Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	1.2		1.4	GHz
PhS	Phase Shifting Range	0		360	deg
PhS step	Phase Shifting Step		5.625		deg
PPE	Peak Phase Error		(-1,+3)		deg
RMS_PE	RMS Phase Error		1.5		deg
IL	Insertion Loss		7		dB
Av	Amplitude Variation		±0.5		dB
RMS_Av	RMS Amplitude Variation		0.15		dB
VSWR_In	Input Return Loss		15		dB
VSWR_Out	Output Return Loss		15		dB
P1dB	Input power @ 1dBcomp (CW)		24		dBm
OP1dB	Output power @ 1dBcomp (CW)		16		dBm
Vlow	Control Input – low level	0		0.4	V
Vhigh	Control Input – high level	2.4		5	V
V+	Positive Supply Voltage		5 , 3.3		V
V-	Negative Supply Voltage		- 5		V
I+	Positive Supply Current		4		mA
I-	Negative Supply Current		3.5		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply voltage	+6	V
V-	Maximum DC negative supply voltage	-6	V
Vlow	Minimum phase shifter control voltage	-2	V
Vhigh	Maximum phase shifter control voltage	+6	V
Tj	Maximum junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Peak Phase Error (PPE) definition

PPE(i) = measured_Phase(S21)@state(i) - measured_Phase(S21)@state(0) - theoreticalPhaseValue@State(i)

Amplitude Variation (Av) definition

Av(i) = Measured_dB(S21)@state(i) - Measured_dB(S21)@state(0)

RMS Phase Error (RMS_PE) definition

$$\text{RMS\_PE} = \sqrt{\frac{\sum_{i=0}^{63} PPE^2(i)}{64}}$$

where i is the state number (from 0 to 63)

RMS Amplitude variation (RMS_Av) definition

$$RMS\_AV = \overline{Av} = \frac{\sum_{i=0}^{63} Av(i)}{64}$$

where i is the state number (from 0 to 63)

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Typical Bias Conditions

The following two options are possible for the positive value of the biasing circuit without impact on the RF performances.

Option 1

Symbol	PIN N°	Parameter	Values	Unit
V+	32	Positive Supply Voltage	+5	V
V-	31	Negative Supply Voltage	-5	V
V+	30	Positive Supply Voltage	NC	
Bit1 to Bit6	29 to 24	Control Input Voltage	0 / +3.3	V

Option 2

Symbol	PIN N°	Parameter	Values	Unit
V+	32	Positive Supply Voltage	+3.3	V
V-	31	Negative Supply Voltage	-5	V
V+	30	Positive Supply Voltage	+3.3	V
Bit1 to Bit6	29 to 24	Control Input Voltage	0 / +3.3	V

Device thermal performances

Since all the FETs of the RF part of the circuit work under null DC drain-source voltage, while the DC-interface power consumption amounts to less than 20mW

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Phase shifter control table

Voltage to apply on Bit1 to Bit6 (pins #29 to #24)

State	Phase (deg)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	State	Phase (deg)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
0	0	0	0	0	0	0	0	32	180	3.3	0	0	0	0	0
1	5.625	0	0	0	0	0	3.3	33	185.625	3.3	0	0	0	0	3.3
2	11.25	0	0	0	0	3.3	0	34	191.25	3.3	0	0	0	3.3	0
3	16.875	0	0	0	0	3.3	3.3	35	196.875	3.3	0	0	0	3.3	3.3
4	22.5	0	0	0	3.3	0	0	36	202.5	3.3	0	0	3.3	0	0
5	28.125	0	0	0	3.3	0	3.3	37	208.125	3.3	0	0	3.3	0	3.3
6	33.75	0	0	0	3.3	3.3	0	38	213.75	3.3	0	0	3.3	3.3	0
7	39.375	0	0	0	3.3	3.3	3.3	39	219.375	3.3	0	0	3.3	3.3	3.3
8	45	0	0	3.3	0	0	0	40	225	3.3	0	3.3	0	0	0
9	50.625	0	0	3.3	0	0	3.3	41	230.625	3.3	0	3.3	0	0	3.3
10	56.25	0	0	3.3	0	3.3	0	42	236.25	3.3	0	3.3	0	3.3	0
11	61.875	0	0	3.3	0	3.3	3.3	43	241.875	3.3	0	3.3	0	3.3	3.3
12	67.5	0	0	3.3	3.3	0	0	44	247.5	3.3	0	3.3	3.3	0	0
13	73.125	0	0	3.3	3.3	0	3.3	45	253.125	3.3	0	3.3	3.3	0	3.3
14	78.75	0	0	3.3	3.3	3.3	0	46	258.75	3.3	0	3.3	3.3	3.3	0
15	84.375	0	0	3.3	3.3	3.3	3.3	47	264.375	3.3	0	3.3	3.3	3.3	3.3
16	90	0	3.3	0	0	0	0	48	270	3.3	3.3	0	0	0	0
17	95.625	0	3.3	0	0	0	3.3	49	275.625	3.3	3.3	0	0	0	3.3
18	101.25	0	3.3	0	0	3.3	0	50	281.25	3.3	3.3	0	0	3.3	0
19	106.875	0	3.3	0	0	3.3	3.3	51	286.875	3.3	3.3	0	0	3.3	3.3
20	112.5	0	3.3	0	3.3	0	0	52	292.5	3.3	3.3	0	3.3	0	0
21	118.125	0	3.3	0	3.3	0	3.3	53	298.125	3.3	3.3	0	3.3	0	3.3
22	123.75	0	3.3	0	3.3	3.3	0	54	303.75	3.3	3.3	0	3.3	3.3	0
23	129.375	0	3.3	0	3.3	3.3	3.3	55	309.375	3.3	3.3	0	3.3	3.3	3.3
24	135	0	3.3	3.3	0	0	0	56	315	3.3	3.3	3.3	0	0	0
25	140.625	0	3.3	3.3	0	0	3.3	57	320.625	3.3	3.3	3.3	0	0	3.3
26	146.25	0	3.3	3.3	0	3.3	0	58	326.25	3.3	3.3	3.3	0	3.3	0
27	151.875	0	3.3	3.3	0	3.3	3.3	59	331.875	3.3	3.3	3.3	0	3.3	3.3
28	157.5	0	3.3	3.3	3.3	0	0	60	337.5	3.3	3.3	3.3	3.3	0	0
29	163.125	0	3.3	3.3	3.3	0	3.3	61	343.125	3.3	3.3	3.3	3.3	0	3.3
30	168.75	0	3.3	3.3	3.3	3.3	0	62	348.75	3.3	3.3	3.3	3.3	3.3	0
31	174.375	0	3.3	3.3	3.3	3.3	3.3	63	354.375	3.3	3.3	3.3	3.3	3.3	3.3

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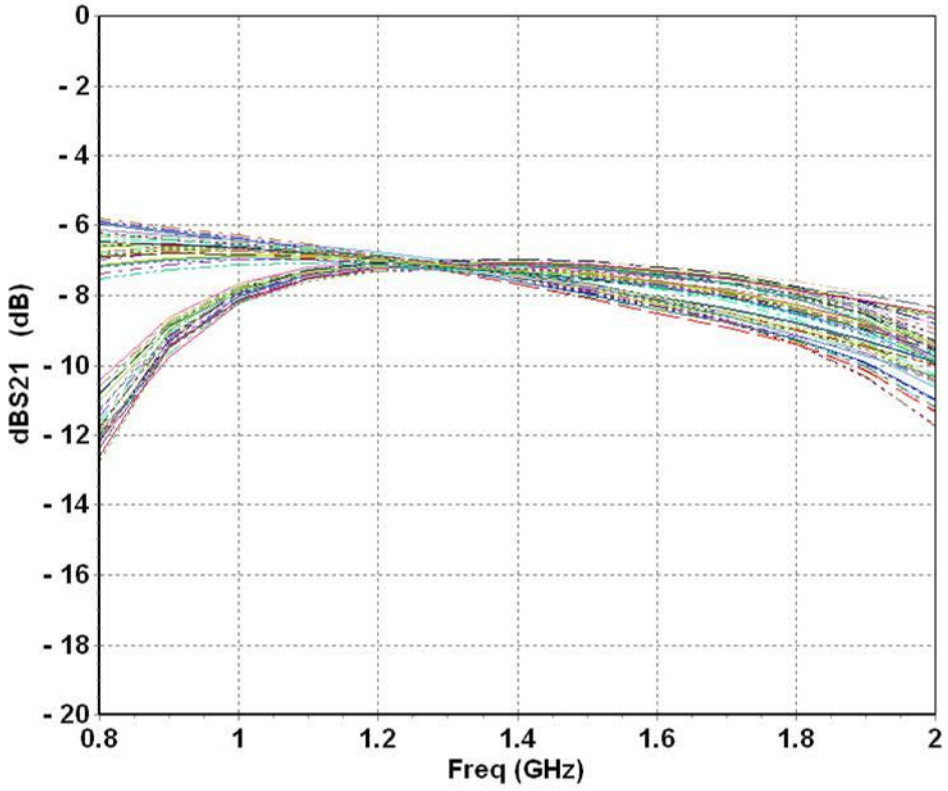
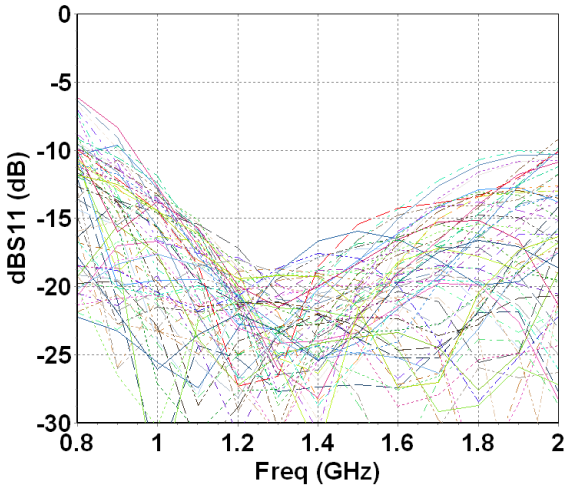
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

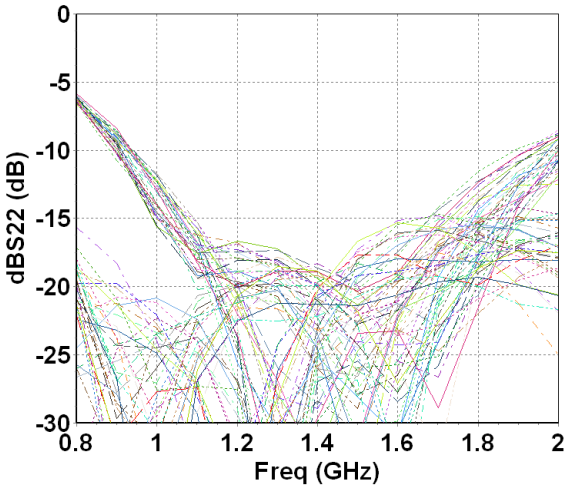
Insertion Loss versus Frequency @ All States
(input/output reference planes are the package access planes)



Input Return Loss @ All States



Output Return Loss @ All States



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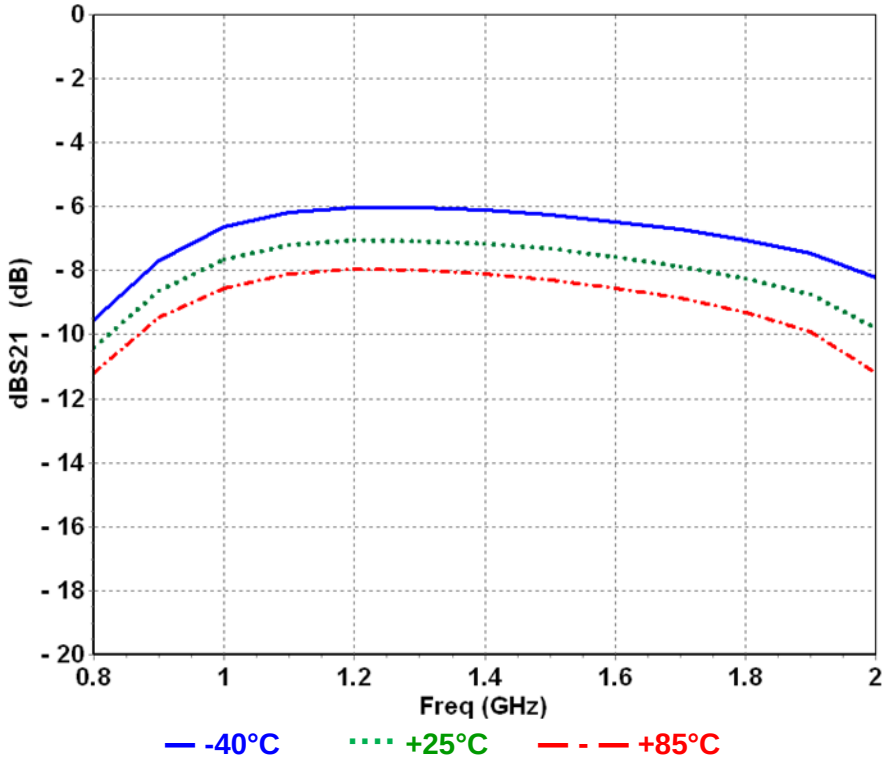
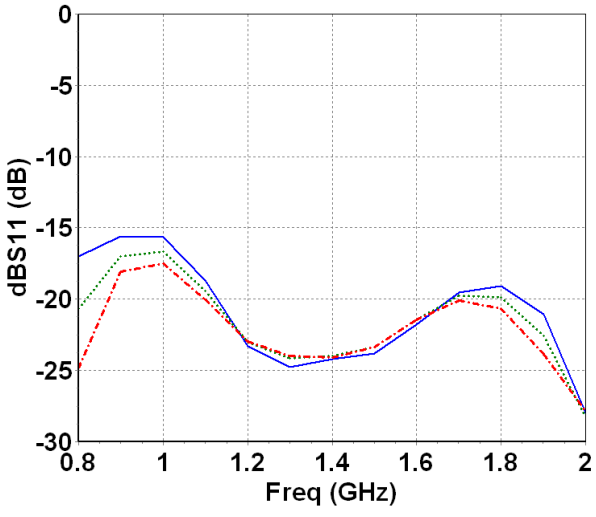
Typical Board Measurements

Temperature .-40°C,+25°C, +85°C V+ = +5V, V- = -5V

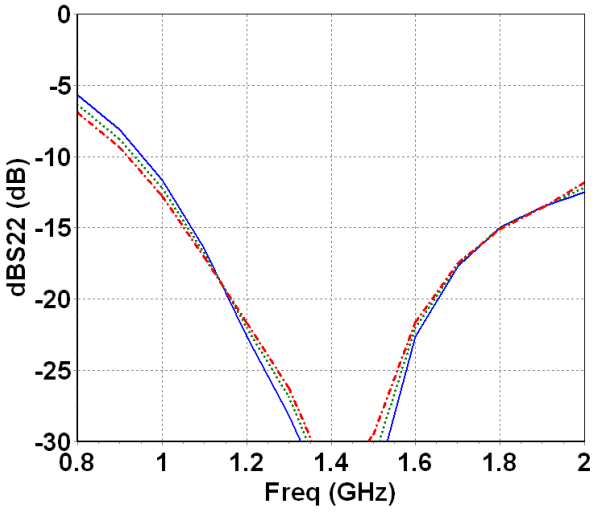
Insertion Loss versus Frequency @ State 0
(input/output reference planes are the package access planes)



Input Return Loss @ State 0



Output Return Loss @ State 0



-40°C +25°C +85°C

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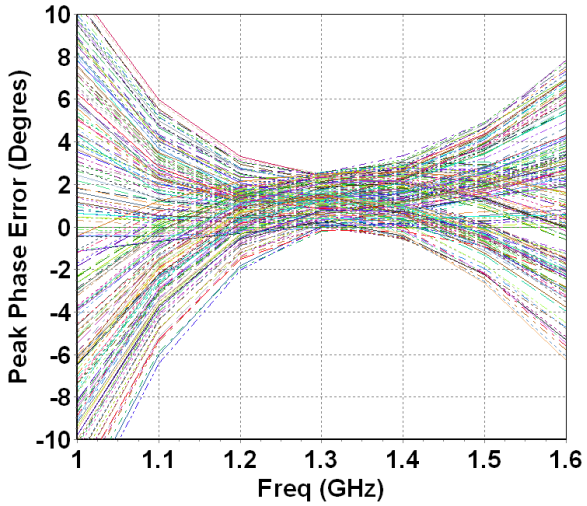
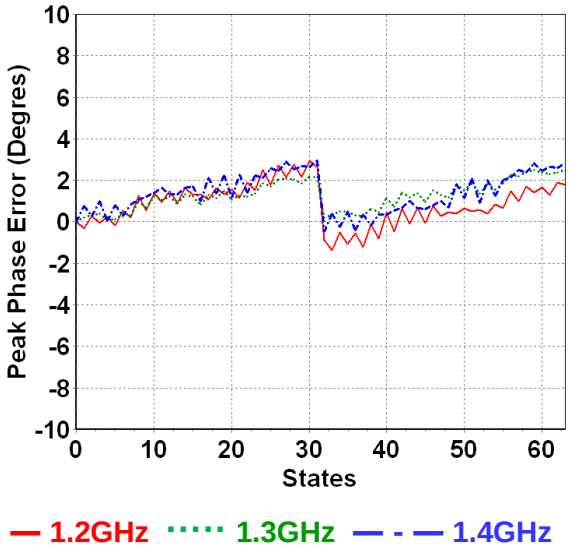
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

Peak Phase Error versus Frequency (All States)

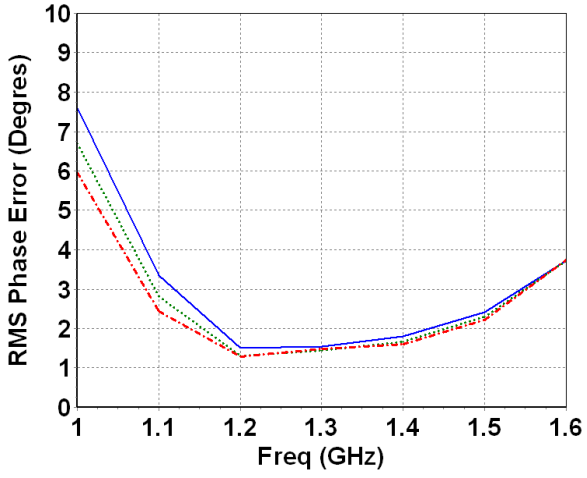


Peak Phase Error versus States



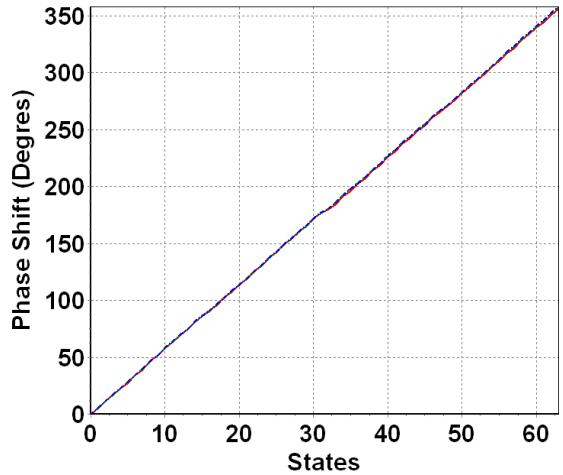
— 1.2GHz ····· 1.3GHz — · — 1.4GHz

RMS Phase Error versus Frequency



— -40°C ··· +25°C — · — +85°C

Phase Shift versus States (1.2 GHz ≤ Frequency ≤ 1.4GHz)



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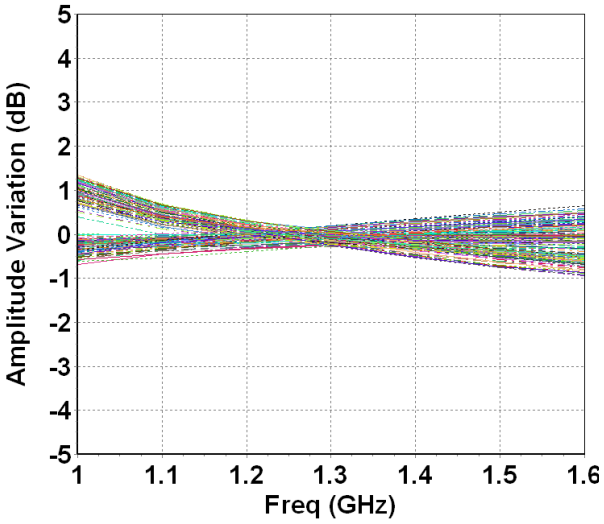
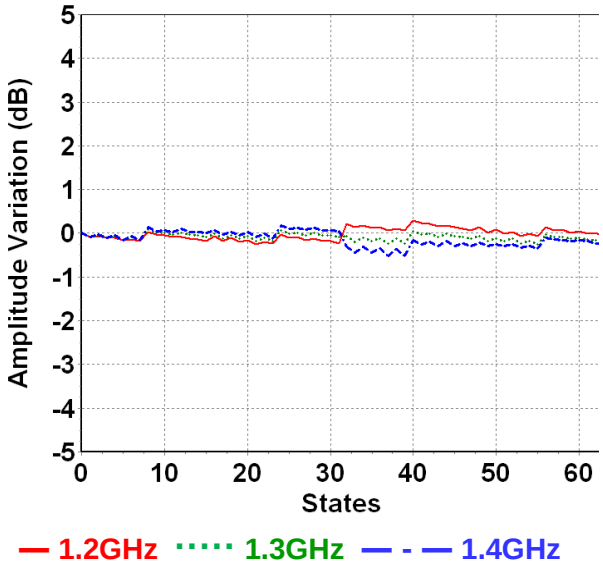
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

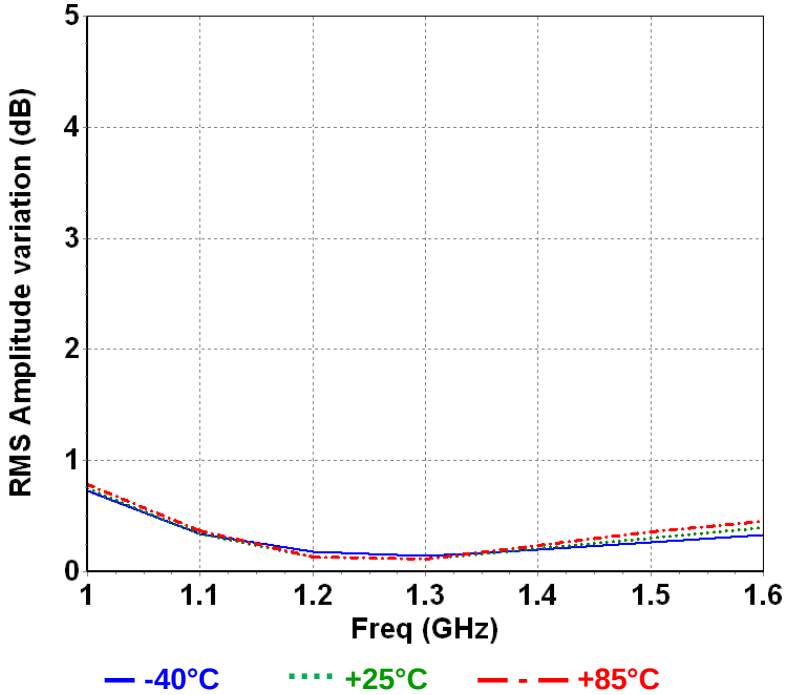
Amplitude Variation versus Frequency (All States)



Amplitude Variation versus States



RMS Amplitude Variation versus Frequency



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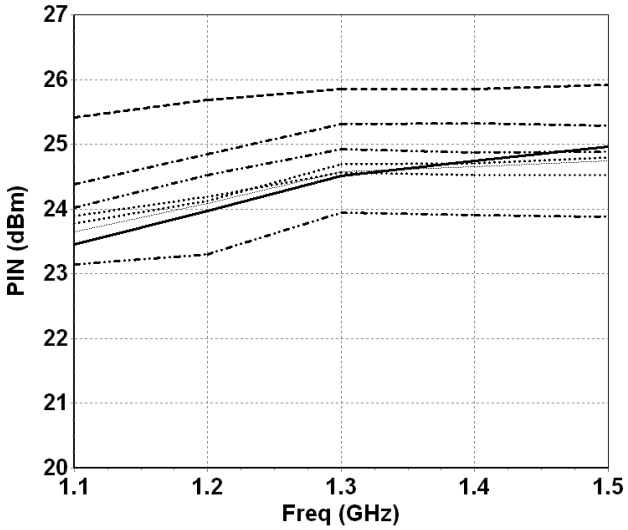
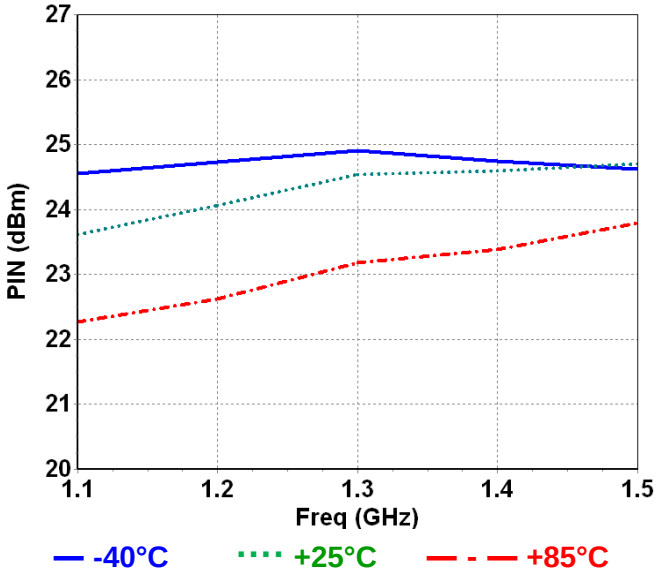
Typical Board Measurements

Measurement input/output reference planes are the package access planes
Tamb.= +25°C, V+ = +5V, V- = -5V

Input Power @ 1dBcomp (Main States)



Input Power @ 1dBcomp (Reference State)



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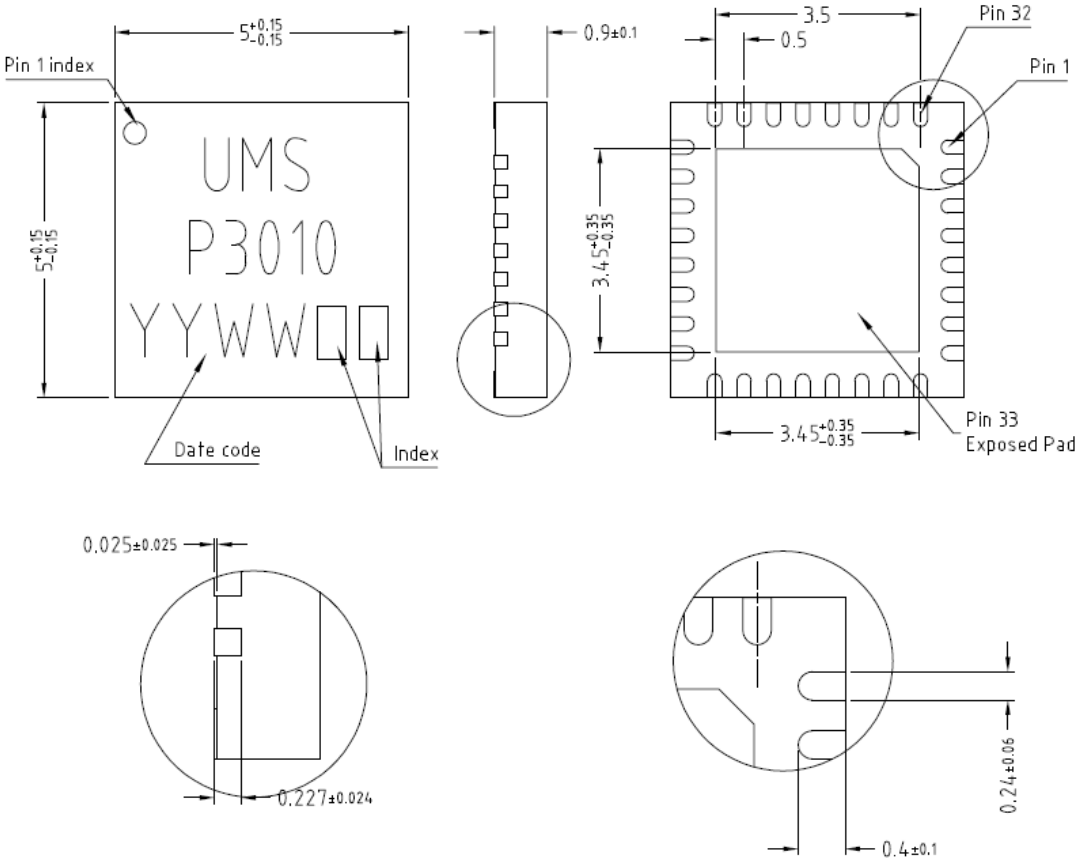
Package outline (1)



Matt tin, Lead Free	(Green)	1-	Nc	12-	Nc	23-	RF out
Units :	mm	2-	RF in	13-	Nc	24-	Bit 6
From the standard :	JEDEC MO-220 (VGGD)	3-	Gnd(2)	14-	Nc	25-	Bit 5
		4-	Nc	15-	Nc	26-	Bit 4
33-	GND	5-	Nc	16-	Nc	27-	Bit 3
		6-	Nc	17-	Nc	28-	Bit 2
		7-	Nc	18-	Nc	29-	Bit 1
		8-	Nc	19-	Nc	30-	V+
		9-	Nc	20-	Nc	31-	V-
		10-	Nc	21-	Nc	32-	V+
		11-	Nc	22-	Gnd(2)		

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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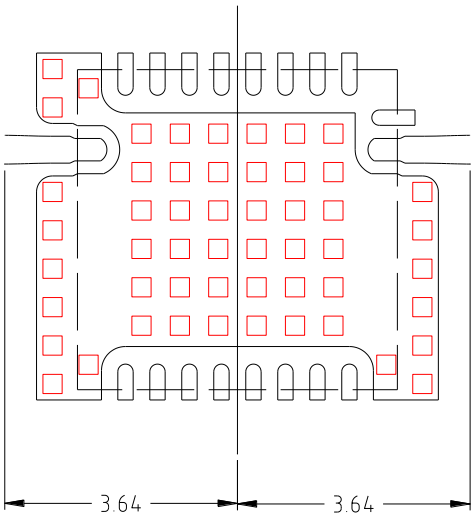
Definition of the Sij reference planes

The reference planes used for the provided Sij measurements are symmetrical from the symmetry axis of the package (see drawing beside). The input and output reference planes are located at 3.64mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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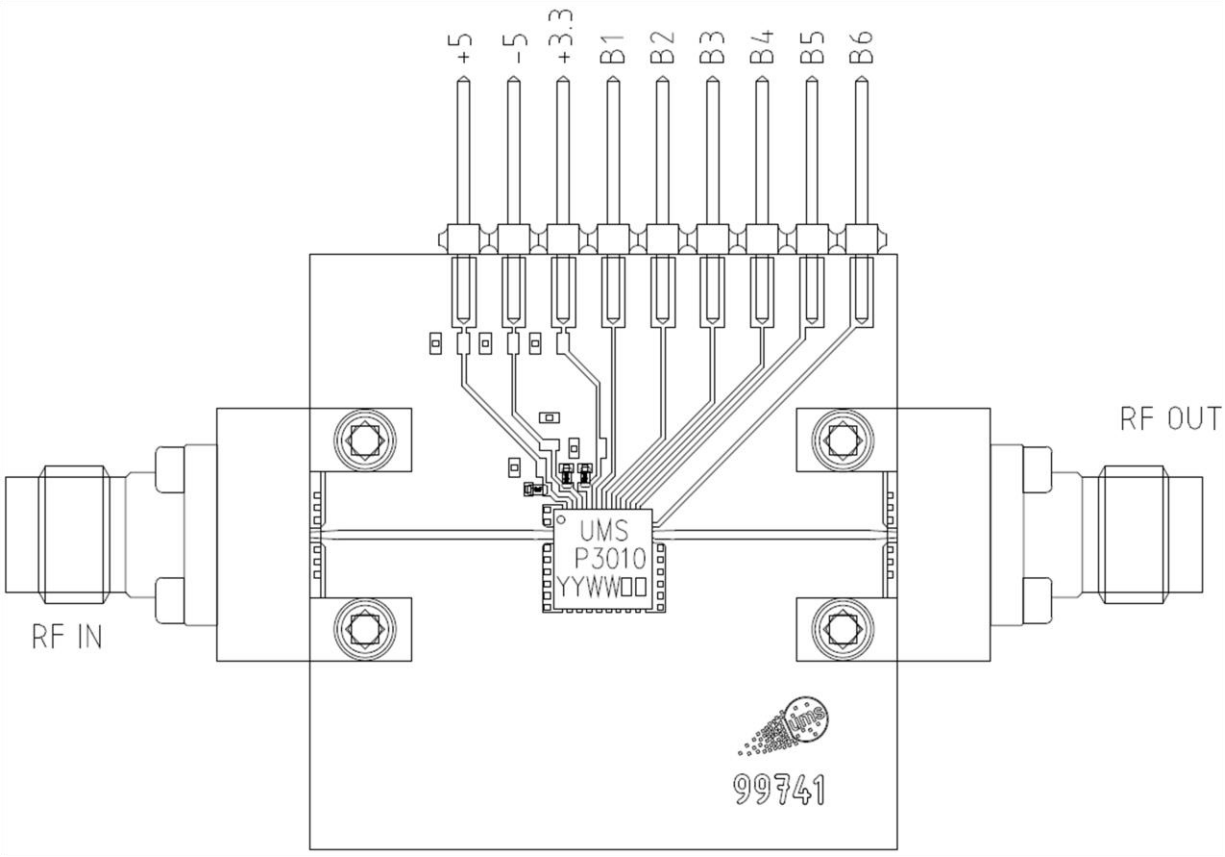
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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Block Diagram

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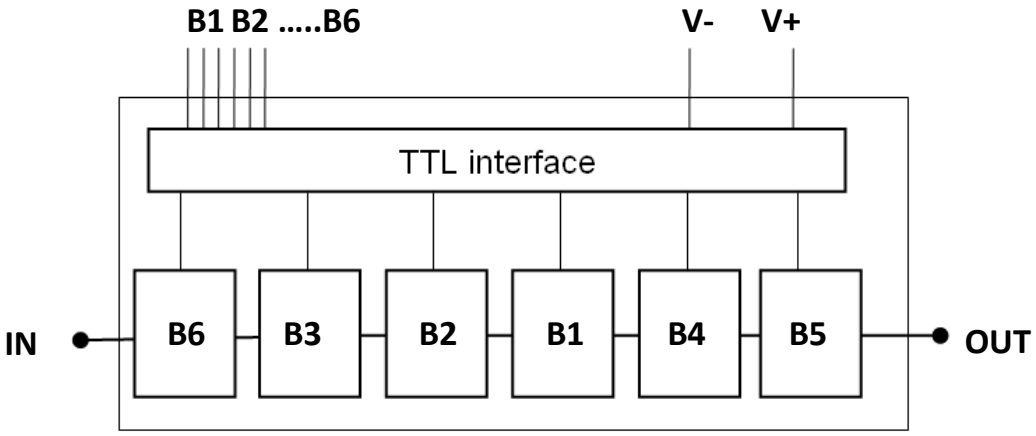

No ESD protections are implemented at interface accesses.
The DC connections do not include any decoupling capacitor in package, nevertheless it is not mandatory to provide external DC decoupling on the PC board

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Notes

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 RoHS compliant package:	CHP3010-QFG	
	Stick: XY = 20	Tape & reel: XY = 21

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