CH334/CH335 Datasheet

V2.2

http://wch.cn

Overview

CH334 and CH335 are USB2.0 protocol compliant 4-port USB HUB controller chips, supporting USB2.0 high-speed and full-speed for uplink ports, and USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps for downlink ports, supporting not only low-cost STT mode (single TT schedules 4 downlink ports in time share), but also supports high performance MTT mode (4 TTs each corresponding to 1 port, concurrent processing).
Industrial grade design with streamlined peripherals for use in computer and industrial control machine motherboards, peripherals, embedded systems, etc.

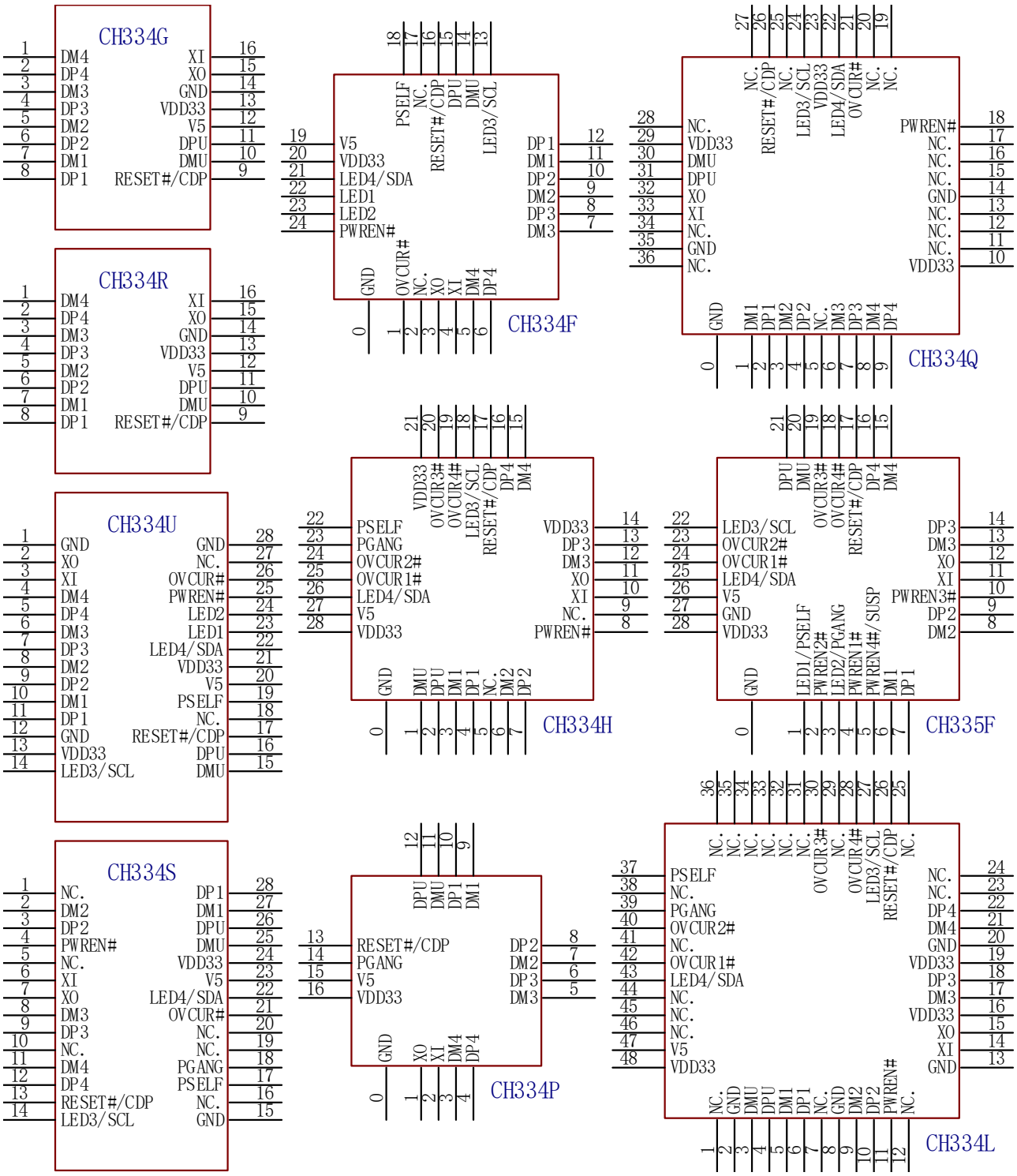
Features

- 4-port USB HUB, providing 4 USB 2.0 downlink ports, backward compatible with USB 1.1 protocol specification
- Support each port independent power control or GANG overall linkage power control
- Support independent overcurrent detection of each port or overall overcurrent detection of GANG, support 5V tolerant overcurrent signal input
- Support high performance MTT mode, providing independent TT for each port to achieve full bandwidth concurrent transmission, with 4 times the total bandwidth of STT
- Support port status LED indicators
- Configurable via external EEPROM to support composite devices, non-removable devices, custom VIDs, PIDs and port configurations
- Built-in information memory, for industry-specific needs can be customized in bulk manufacturer or product information and configuration
- Self-developed dedicated USB PHY, low-power consumption technology, significantly reduced compared to the first generation of HUB chips, support self-powered or bus-powered
- Self-powered or bus-powered mode configurable via I/O pins or external EEPROM
- Provide crystal oscillator with built-in capacitor, supports external 12MHz input, and built-in PLL provides 480MHz clock for USB PHY
- Built-in 1.5KΩ pull-up resistor on the uplink port, built-in pull-down resistor on the downlink port required for USB Host, streamlined periphery
- Built-in LDO linear buck regulator converts USB bus supply voltage to 3.3V operating power for the chip
- 6KV enhanced ESD performance, Class 3A
- Industrial-grade temperature range: -40～85℃
- QFN28, SOP16, QSOP28 and other small, low-cost, easy-to-process packages are available

Chapter 1 Pinouts and pin definition

1.1 Pin Arrangement

Figure 1-1 Pin Distribution



Note: Pin 0# refers to the QFN package backplane (exposed pad).

1.2 Model Comparison

Table 1-1 Function comparison of the same cluster model

Model / Function	CH334G	CH334R	CH334P	CH334U CH334F	CH334S CH334Q	CH334H CH334L	CH335F
TT mode	STT	MTT	MTT	MTT	MTT	MTT	MTT
Overcurrent detection	×	×	×	GANG mode	GANG mode	Independent / GANG	Independent / GANG
Power Control	×	×	×	GANG mode	GANG mode	GANG mode	Independent / GANG
LED indicator	×	×	1-LED	5-LED	1-LED	1-LED	5-LED / 9-LED
I/O pin configuration Power supply mode	×	×	×	√	√	√	√
External EEPROM Provide configuration information	×	×	×	√	√	√	√
Custom configuration information	√	√	√	√	√	√	√
USB3.0 pass-through	×	—	—	—	—	—	√

1.3 Packaging

Table 1-2 Package Description

Package form	Shaping width		Pin spacing		Package Description	Order Model
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin chip	CH334G
QSOP16	3.9mm	150mil	0.635mm	25mil	1/4 size 16-pin SMD	CH334R
QSOP28	3.9mm	150mil	0.635mm	25mil	1/4 size 28-pin SMD	CH334U
SSOP28	5.3mm	209mil	0.65mm	25mil	Reduced 28-pin chip	CH334S
QFN16_3x3	3*3mm		0.5mm	19.7mil	Quad side leadless 16-pin	CH334P
QFN24_4x4	4*4mm		0.5mm	19.7mil	Quad side leadless 24-pin	CH334F
QFN28_5x5	5*5mm		0.5mm	19.7mil	Quad side leadless 28-pin	CH334H
QFN36_6x6	6*6mm		0.5mm	19.7mil	Quad side leadless 36-pin	CH334Q
LQFP48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin chip	CH334L
QFN28_4x4	4*4mm		0.4mm	15.7mil	Quad side leadless 28-pin	CH335F

Note: Preferred CH334P, small size; CH335 full pinout; other package forms focus on PCB compatibility; CH334L is available for bulk booking only.

1.4 Pin Description

Table 1-3 Pin definition

Pin number (Pin with the same name can be referred to)								Pins Name	Type	Function Description
335F	G/R	4F	4U	4S	4Q	4H	4L			
20	10	14	15	25	30	1	3	DMU	USB	Uplink port USB2.0 signal cable D-
21	11	15	16	26	31	2	4	DPU	USB	Uplink port USB2.0 signal line D+
6	7	11	10	27	1	3	5	DM1	USB	1# downlink port USB signal cable D-
7	8	12	11	28	2	4	6	DP1	USB	1# downlink port USB signal line D+
8	5	9	8	2	3	6	9	DM2	USB	2# downlink port USB signal cable D-
9	6	10	9	3	4	7	10	DP2	USB	2# downlink port USB signal line D+
13	3	7	6	8	6	12	17	DM3	USB	3# downlink port USB signal cable D-
14	4	8	7	9	7	13	18	DP3	USB	3# downlink port USB signal line D+
15	1	5	4	11	8	15	21	DM4	USB	4# downlink port USB signal cable D-
16	2	6	5	12	9	16	22	DP4	USB	4# downlink port USB signal line D+
11	16	4	3	6	33	10	14	XI	I	Crystal oscillator input, connected to the external

										crystal end
12	15	3	2	7	32	11	15	XO	O	Crystal oscillator inverted output, connected to the other end of the external crystal
17	9	16	17	13	26	17	26	RESET# CDP	5I	External reset input with built-in pull-up resistor, active low. It is recommended to be completely suspended when not reset.
26	12	19	20	23	-	27	47	V5	P	5V or 3.3V power input, external 1uF or larger capacitor
28	13	20	21	24	29	28	48	VDD33	P	Main power supply, LDO output and 3.3V input. External 0.1uF+10uF decoupling capacitor, or 1uF decoupling capacitor
-	-	-	13	-	10 23	14 21	16 19	VDD33	P	3.3V power input, external 1uF or 0.1uF decoupling capacitor
27	14	-	1 12 28	15	14 35	-	2 8 13 20	GND	P	Common ground terminal
0	-	0	-	-	0	0	-	GND	P	Common ground terminal (base plate)
24	-	1	26	21	21	25	42	OVCUR# OVCUR1 #	5I	GANG integral mode line port overcurrent detection input pin. 1# downlink port overcurrent detection input pin, low overcurrent
23	-	-	-	-	-	24	40	OVCUR2 #	5I	2# Downlink port overcurrent detection input pin, low overcurrent
19	-	-	-	-	-	20	30	OVCUR3 #	5I	3# Downlink port overcurrent detection input pin, low overcurrent
18	-	-	-	-	-	19	28	OVCUR4 #	5I	4# downlink port overcurrent detection input pin, low overcurrent
4	-	24	25	4	18	8	11	PWREN# PWREN1 #	O	GANG integral mode line port power output control pins. 1# downlink port power output control pin, low on
2	-	-	-	-	-	-	-	PWREN2 #	O	2# downlink port power output control pin, low on
10	-	-	-	-	-	-	-	PWREN3	O	3# downlink port power output control pin, low on

								#		
5	-	-	-	-	-	-	-	SUSP PWREN4 #	O	GANG overall mode SUSPEND sleep state output pin, high level indicates sleep state, low level indicates normal state. 4# downlink port power output control pin, low on
-	-	18	19	17	-	22	37	PSELF	I	Configure power supply mode with built-in pull-up resistor: default high level is self-powered, low level is set for bus power
-	-	-	-	18	-	23	39	PGANG	I/O	Configure power overcurrent protection mode during reset with built-in pull-up resistor. Switch to sleep/normal state output after reset is complete. Default high level for overall overcurrent detection and overall power control, with low output indicating normal state and high indicating sleep state after reset. External pull-down resistor set low for independent overcurrent detection, after reset the output high indicates normal state, low indicates sleep state
1	-	22	23	-	-	-	-	LED1 PSELF	I/O	LED1: port status indication signal 1. PSELF: configure power supply mode during reset, built-in pull-up, default high for self-power, plus pull-down to set low for bus power
3	-	23	24	-	-	-	-	LED2 PGANG	I/O	LED2: port status indication signal 2. PGANG: configure power overcurrent protection mode during reset, built-in pull-up, default high for overall overcurrent detection and overall power control, plus pull-down to set low for independent overcurrent detection
22	-	13	14	14	24	18	27	LED3 SCL	I/O	LED3: port status indication signal 3. SCL: Output for EEPROM clock signal line during reset
25	-	21	22	22	22	26	43	LED4 SDA	I/O	LED4: port status indication signal 4. SDA: EEPROM bi-directional data signal line during reset

-	-	2 17	18 27	1 5 10 16 19 20	*	5 9	*	NC.		Empty pins or reserved pins, disable connection

Pin Type:

1) I: 3.3V signal input.
2) O: 3.3V signal output.
3) 5I: Rated 3.3V signal input, supports 5V tolerant voltage.
4) P: Power or ground.

Chapter 2 Structure

2.1 System Architecture

Figure 2-1 System block diagram

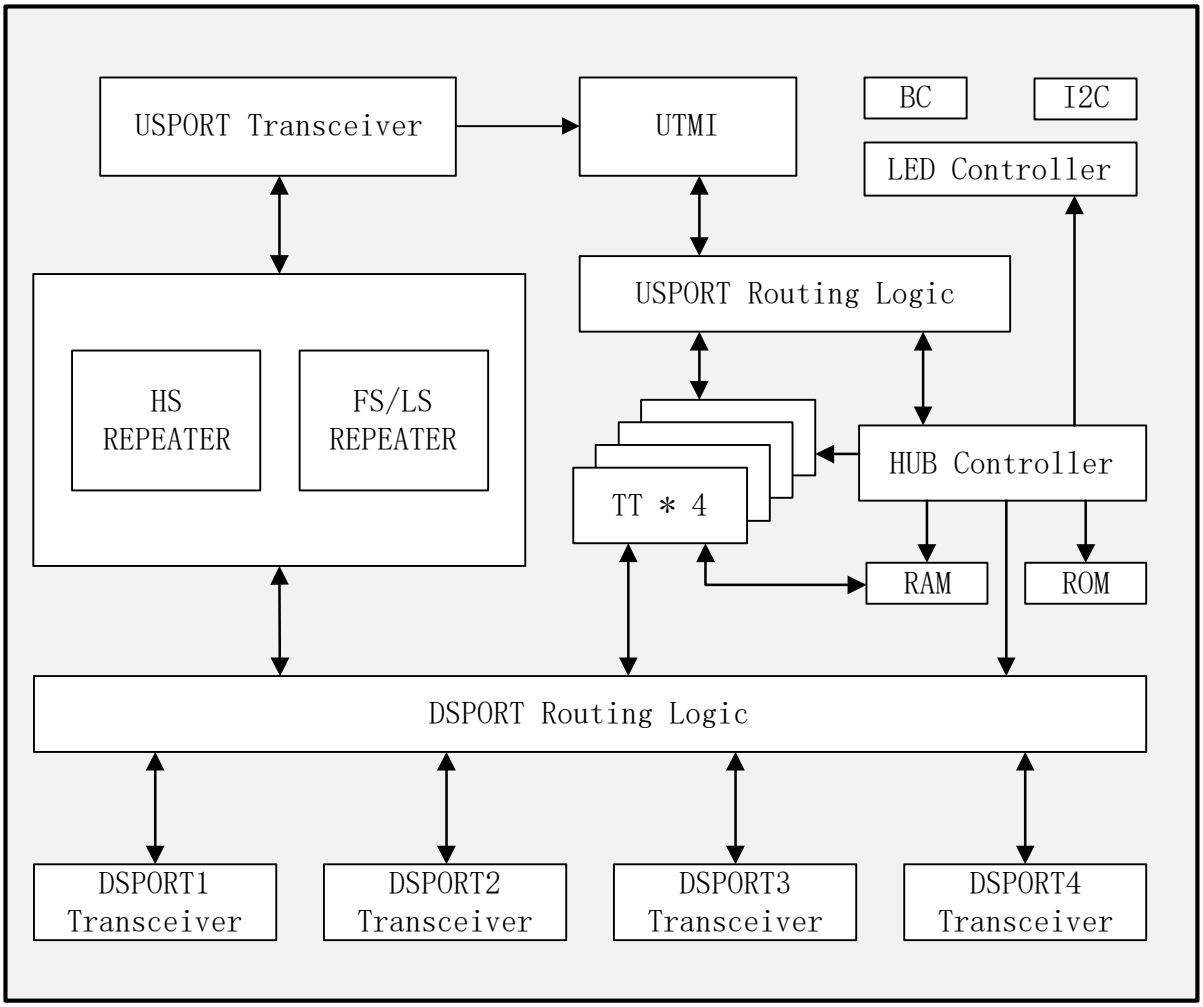


Figure 2-1 is a block diagram of the internal structure of the HUB controller system. The HUB controller consists of three main modules: Repeater, TT and controller. The controller is similar to an MCU processor for global management and control. The routing logic will connect the port to Repeater when the speed of uplink port and downlink port are the same, and connect the port to TT when the speed of uplink port and downlink port are not the same.

TT is divided into single TT and multiple TT, i.e., STT and MTT, STT is a single TT core dispatched in time to handle the transactions sent down to all downlink ports by the USB host, MTT refers to multiple TT in parallel, which is 4 TT cores corresponding to and processing the transactions of one downlink port in real time, so MTT can provide fuller bandwidth for the access devices of each downlink port and better support multi-port large concurrent transmission of large data volumes.

Notes:

USPORT Transceiver: Uplink port transceiver PHY

DSPORT Transceiver: downlink port transceiver PHY

REPEATER: HUB Repeater

TT: Processing converter.

Chapter 3 Functions

3.1 Overcurrent detection

CH334/CH335 support three overcurrent protection modes: Individual independent control power and independent overcurrent detection, GANG overall control power and independent overcurrent detection, and GANG overall linked control power and overall overcurrent detection (Default mode), as shown in Table 3-1.

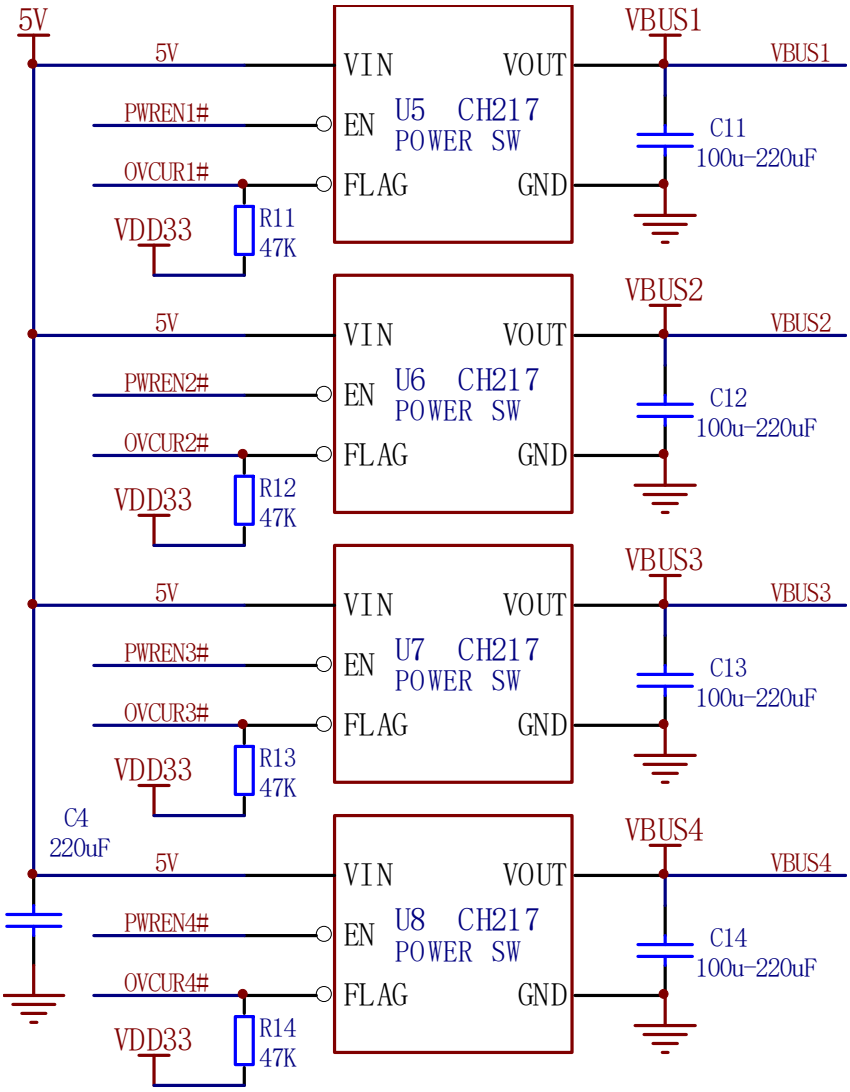
Table 3-1 Overcurrent protection control pin description

Overcurrent protection mode	**Power control pins**	**Sampling pins for overcurrent detection**	**Reference Chart**
Dual independent mode	PWREN1#PWREN2#，PWREN3#，PWREN4#	OVCUR1#，OVCUR2#，OVCUR3#，OVCUR4#	Figure 3-1-1
The whole control solo inspection mode	PWREN#（PWREN1#）	OVCUR1#，OVCUR2#，OVCUR3#，OVCUR4#	Figure 3-1-2
GANG overall model	PWREN#（PWREN1#）	OVCUR#（OVCUR1#）	Figure 3-1-3

CH335F supports dual independent mode and GANG overall mode; CH334H/L supports whole control solo check mode and GANG overall mode; CH334U/S/F/Q supports GANG overall mode only; CH334G/R/P does not support overcurrent detection.

3.1.1 Dual independent mode

Figure 3-1-1 Dual independent mode, R11~R14 can be omitted



U5 to U8 are USB current-limiting distribution switch chips with integrated internal overcurrent detection for VBUS power distribution management, such as CH217 chip or similar functions. In applications without external power supply at 5V, it is recommended to set the current limit below 1A or even 500mA through ISET external resistors. the FLAG pins of U5~U8 are open-drain outputs, which require R11~R14 pull-ups respectively. Under the default configuration, OC_LEVEL=0, the OVCUR# pin of HUB chip provides built-in weak pull-up current, so R11~R14 can be omitted. the capacity of C11~C14 is selected according to the need, the minimum 120uF in the specification. the dual independent mode requires setting GANG_MODE=0 to select independent overcurrent detection mode.
In the figure, VBUS1/VBUS2/VBUS3/VBUS4 are connected to the VBUS power pins of downlink ports 1/2/3/4 respectively.

3.1.2 Whole control solo inspection model

The preferred whole control solo check circuit is based on Figure 3-1-1 dual independent mode circuit modification, with PWREN# simultaneously controlling U5 to U8. Considering that C11 to C14 are charged simultaneously when the 4 groups of switches are turned on, it is recommended that the capacity of C4 is not less than the accumulated capacity of C11 to C14.

Figure 3-1-2 Another non-preferred circuit for the whole control solo check mode

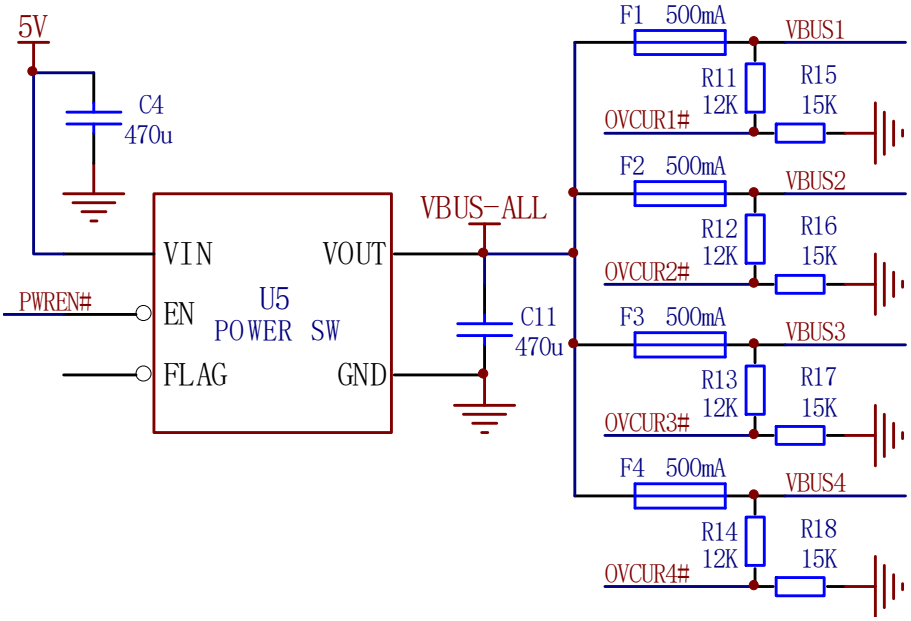
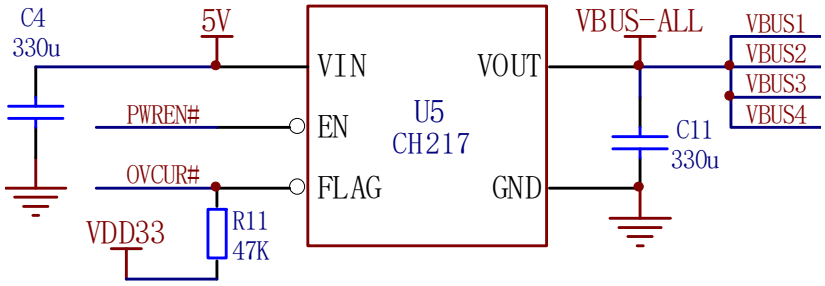


Figure 3-1-2 is another option, U5 is the shared power switch chip, F1 to F4 are the insurance resistors, and C11 is selected as needed. Alternatively, there is a simplified application that removes power control, based on Figure 3-1-2 that omits U5/C4 and shorts the VBUS-ALL to 5V.

3.1.3 GANG overall model

Figure 3-1-3 GANG overall mode, R11 can be omitted



U5 is a USB current-limiting power switch chip. R11 can be omitted in the default configuration, and the capacity of C11 can be selected as needed.

Figure 3-1-4 Simplified GANG overall mode power control and overcurrent detection circuit Schematic

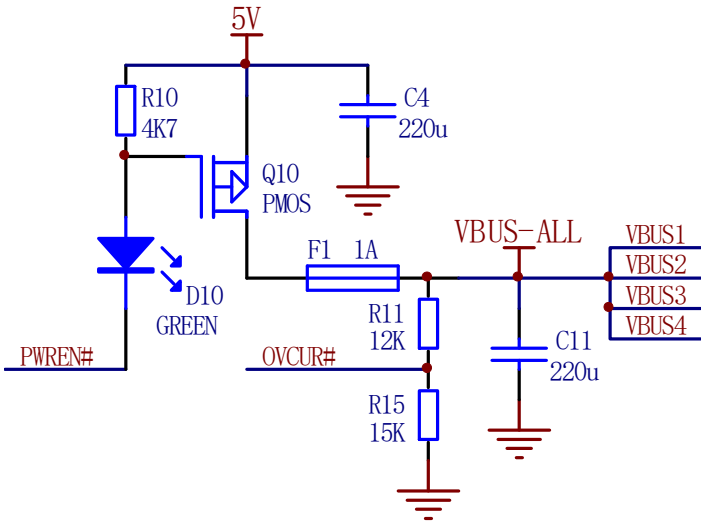


Figure 3-1-4 is a simplified schematic, for principle reference only. The default configuration OC_LEVEL=0, R11 and R15 voltage divider to select the overcurrent detection point for VBUS down to about 4V. If the configuration OC_LEVEL = 1, then you can remove R15 and change R11 to 1K.

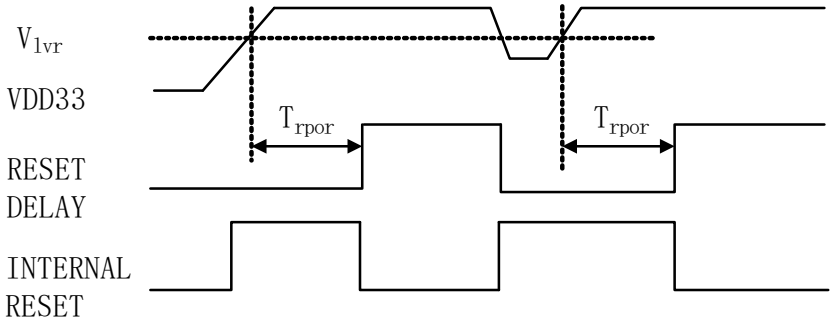
3.2 Reset

A power-on reset module is embedded in the chip, which generally eliminates the need for an externally provided reset signal. An external reset input pin, RESET#/CDP, which has a built-in pull-up resistor, is also provided.

3.2.1 Power-on reset

When the power supply is powered on, the chip's internal POR power-on reset module generates a power-on reset timing and delays Trpor for about 12mS to wait for the power supply to stabilize. During operation, when the power supply voltage falls below V_{lvr}, the chip's internal LVR low voltage reset module generates a low voltage reset until the voltage comes back up, and delays until the power supply stabilizes. Figure 3-2-1 shows the power-on reset process and the low-voltage reset process.

Figure 3-2-1 Reset during power-up



3.2.2 External reset

The external reset input pin RESET#/CDP has a built-in pull-up resistor of about 25KΩ, so if the chip needs to be reset externally, then the pin can be driven low, and the drive internal resistance is recommended to be no greater than 800Ω, and the low-level pulse width of the reset needs to be greater than 4uS.

Table 3-2 Reset Pin Control and Mode Description

RESET#/CDP pin	Conditions	Results
Drive is low	During power-up or during normal operation	Reset HUB chip
Drive is high	During power-up	Enable CDP and turn off low-power sleep
No drive or no connection(default)	During power-up	No CDP enabled, low-power sleep support
Drive high or no drive	During normal operation	No effect

Note: CDP is a configurable function, some package forms/partial lots of CH334/5 may not enable CDP.

For applications where the MCU pin directly drives the RESET#/CDP pin of the HUB chip, if the MCU pin outputs a high-level during power-up, it may enable the charging function of CH334/CH335 and turn off the low-power sleep, so if you want to avoid enabling the charging function and reduce the sleep current, then you need to connect a series connection between the MCU pin and the RESET#/CDP pin of the HUB chip. diode, refer to Figure 3-2-2.

Figure 3-2-2 MCU pin driven reset and avoid enabling charging function

3.2.3 Charging function

In addition to CDP, we can also provide Type-C and USB PD high-voltage fast charging whole solutions.

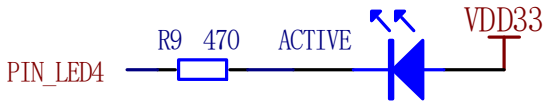
3.3 LED indicators

According to USB2.0 protocol specification, CH334/CH335 provides downlink port status LED indicator control pins, the corresponding green LED of the port is on to indicate normal port status, the green LED is off to indicate no device or hanging Suspend, and the corresponding red LED of the port is on to indicate abnormal port. CH334/CH335 can dynamically drive 1-LED application and 5-LED application, and CH335 also supports 9-LED application. The LED current limiting resistors R5 to R8 in each figure can be selected from 100Ω to 1KΩ range.

3.3.1 LED4 pin 1-LED application

The LED4 pin can dynamically drive an LED in a time-sharing manner, with LED indicating normal operation Active and off indicating HUB chip sleep Suspend. As shown in Figure 3-3-1, the LED current limiting resistor R9 in the figure is selectable from 200Ω to 1KΩ range.

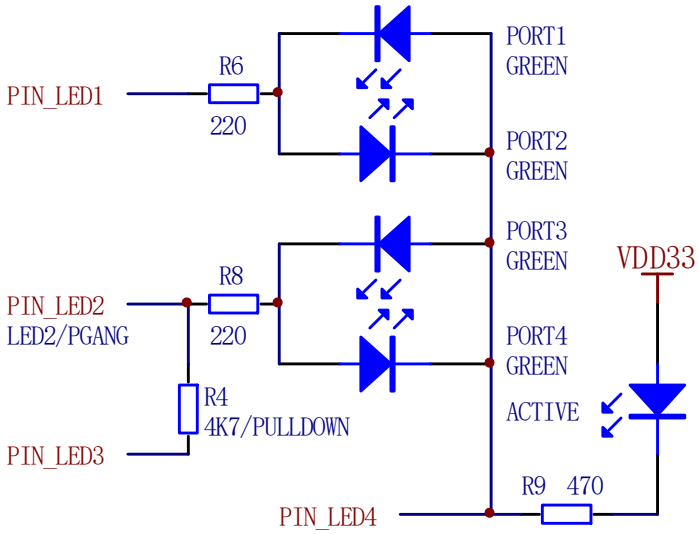
Figure 3-3-1 LED indicator 1 application schematic



3.3.2 5-LED application of CH335

For CH335, pins LED1/PSELF or LED2/PGANG are supported to be pulled down externally for configuration during reset. Because pins LED1/2 double as LED drive outputs, LED1 and LED2 cannot be directly shorted to GND. the specific pull-down method is to connect a 4.7KΩ resistor between pins LED1 or LED2 and pin LED3, optionally in the range of 3KΩ to 6.8KΩ. LED3 is output low during reset, and LED1/PSELF or LED2/PGANG pull-down as shown in Figure 3-3-2. If pin LED1 or LED2 has been used to drive LED indicators, to avoid conflicts, then it is recommended to give preference to EEPROM configuration or custom configuration.
GANG mode is selected by default, no PGANG configuration is required for independent overcurrent detection, and R4 should be removed from the figure.

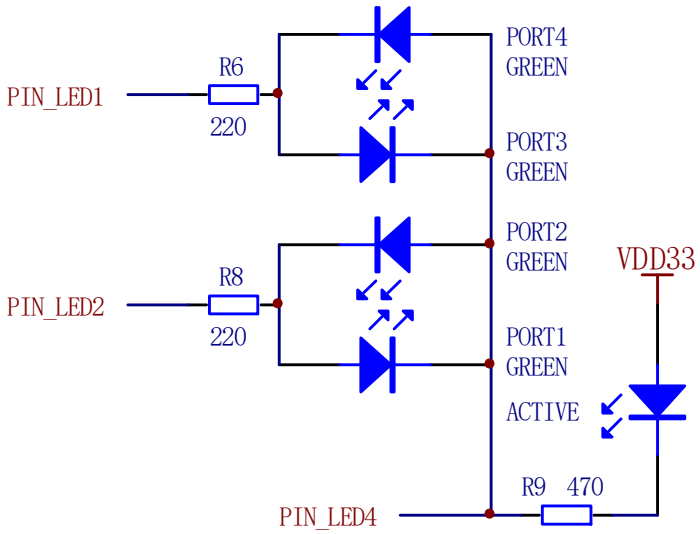
Figure 3-3-2 5-LED application with PGANG enabled for CH335



3.3.3 5-LED application of CH334U/F

For CH334U and CH334F, there are independent PSELF pins available for configuration, and they do not support independent overcurrent detection and do not require PGANG configuration options, so pins LED1 and LED2 do not need to be used for PSELF and PGANG configuration.
The 5-LED application of CH334U/CH334F is shown in Figure 3-3-3, note the LEDs correspond to the ports. The green LED corresponding to each port is on to indicate that the port status is normal, and the green LED is off to indicate that there is no device on the port or Suspend is hung. all LEDs are optional.

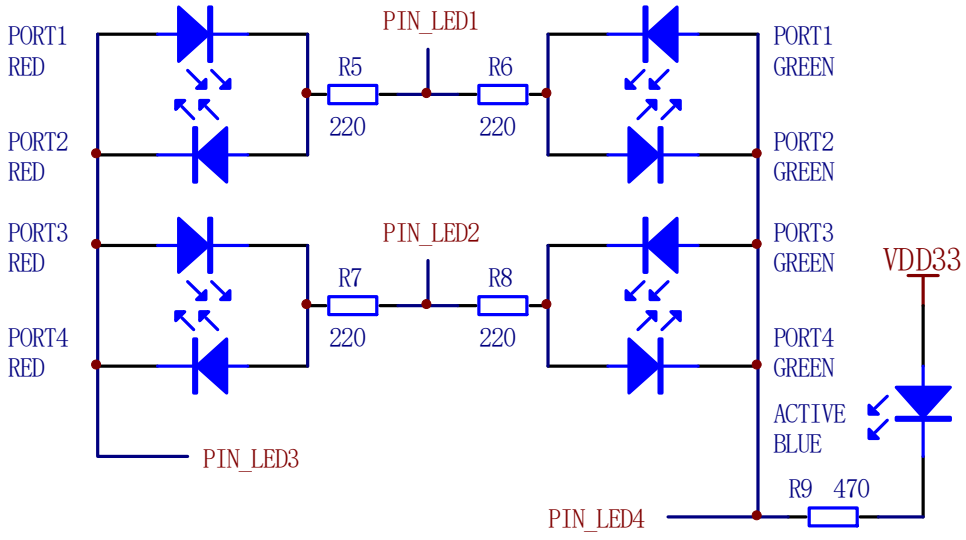
Figure 3-3-3 5-LED application of CH334U/F



3.3.4 All 9-LED application

The 9-LED application is mainly used for CH335, as shown in Figure 3-3-4. The 9-LED application adds four red LEDs compared to the 5-LED application, and the corresponding red LEDs on the port indicate port abnormalities, including port overcurrent or transmission errors, etc.

Figure 3-3-4 9-LED indicator application schematic



3.3.5 PGANG pin LEDs

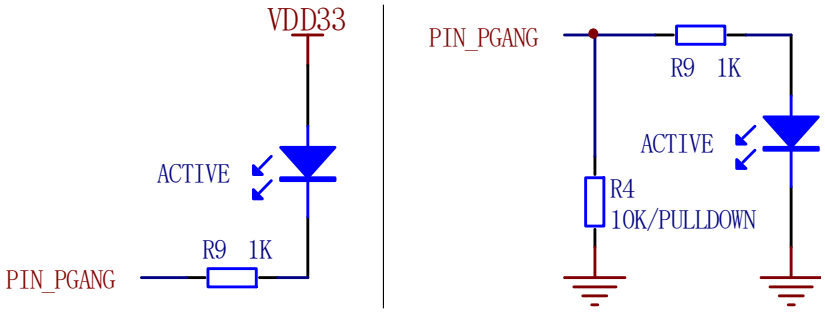
Some package forms provide PGANG pin or PSELF pin, PSELF is a built-in pull-up resistor input pin, used to configure the power supply mode. PGANG is a bi-directional pin, built-in pull-up resistor, during the reset to configure the power supply overcurrent protection mode, after the completion of the reset to sleep Suspend, normal Active state output. PGANG pin driven LED Equivalent to LED4 pin driven 1-LED applications, the difference is that the LED4 pin is dynamic time-sharing drive LED, PGANG pin is static drive, LED current limit resistor R9 can be larger.

As shown in the left diagram of Figure 3-3-5, the PGANG pin is pulled up by the built-in resistor by default and goes high by default to select overall overcurrent detection and overall power control. the PGANG pin outputs low and the LED is on to indicate Active and the LED is off to indicate Suspend.

As shown in Figure 3-3-5 right, the PGANG pin is pulled down by external resistor R4, low by default, and

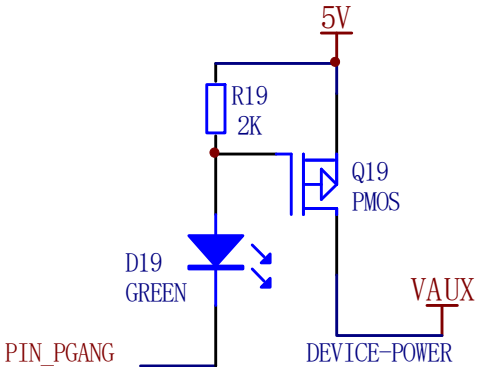
independent overcurrent detection is selected. the PGANG pin is internally inverted to output, and the PGANG pin outputs high and the LED is on to indicate Active, and the LED is off to indicate Suspend.

Figure 3-3-5 PGANG pin driving LED, the right picture is enabled PGANG



The statically driven PGANG pin can be used to control power to external devices, such as powering off peripherals during Suspend.

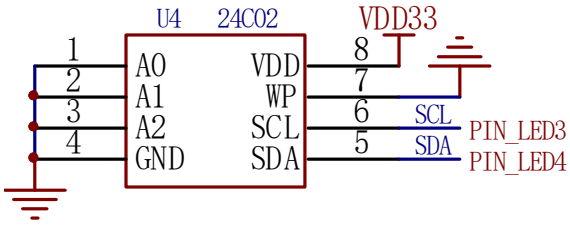
Figure 3-3-6 PGANG pin control external device power schematic



3.4 EEPROM configuration interface

CH334 and CH335 provide a 2-wire I2C interface to communicate with an external EEPROM memory chip with address 0 and custom manufacturer ID, product ID, configuration, etc. The SCL pin outputs a clock frequency of 187.5KHz and the SDA pin has a built-in pull-up current of approximately 250uA to support open-drain bi-directional data communication. No external pull-up resistor is required. Referring to Figure 3-4, there is no conflict between connecting external EEPROM and LED driver, supporting 9-LED, 5-LED, 1-LED, and no-LED applications.

Figure 3-4 External EEPROM connection diagram



CH334 and CH335 have built-in information memory, which can replace the external EEPROM for batch customization of vendor or product information and configuration for industry-specific needs, such as setting the number of downlink ports and setting the non-removable characteristics of devices on the downlink ports, etc.

3.5 EEPROM contents

CH334/CH335 supports loading configuration information such as vendor identification code VID and product identification code PID from external EEPROM. After the chip is powered on, the data of internal ROM is loaded first, and the data of external EEPROM is loaded after loading internal ROM data. If the checksum of data in EEPROM is invalid, all data in EEPROM is dropped; if the CHKSUM of EEPROM is valid, all data in EEPROM is loaded. The specific layout of EEPROM is shown in Table 3-5-1, and the definition of each address in EEPROM is explained in Table 3-5-2.

Table 3-5-1 EEPROM Address Layout

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00h	VID_L	VID_H	PID_L	PID_H	CHKSUM	FF	Device Removable	Port Number	Max Power	SIG	CFG	FF	FF	FF	FF	FF
10h	Vendor Length	Vendor String (UNICODE)														
20h																
30h	Vendor String End															
40h	Product Length	Product String (UNICODE)														
50h																
60h	Product String End															
70h	SN Length	Serial Number String (UNICODE)														
80h-9Fh	Serial Number String End															
A0h-FFh	Reserved															

Table 3-5-2 EEPROM address content definition

Byte Address	Parameter Abbreviation	Parameter Description	Default Value
00h	VID_L	The low byte of the vendor identification code VID.	86h
01h	VID_H	The high byte of the vendor identification code VID.	1Ah
02h	PID_L	The low byte of the product identification code PID.	随型号
03h	PID_H	The high byte of the product identifier PID.	80h
04h	CHKSUM	The checksum CHKSUM must be equal	

		toVID_H+VID_L+PID_L+PID_H+1. Otherwise, all data in the EEPROM is ignored.	
06h	Device Removable	Bit7 to Bit5, Bit0: Reserved. Bit4: A value of 1 indicates that the device connected to downlink port 4 is not removable. Bit3: A 1 indicates that the device connected to downlink port 3 is not removable. Bit2: A 1 indicates that the device connected to downlink port 2 is not removable. Bit1: A value of 1 indicates that the device connected to downlink port 1 is not removable.	00h
07h	Port Number	Number of downlink ports, valid value range 1 to 4.	04h
08h	Max Power	Maximum operating current in 2mA.	32h
09h	SIG	0Ah information CFG valid signature flag, must be 5Ah, otherwise CFG is invalid.	5Ah
0Ah	CFG	Bit7: Reserved. Bit6: EEPROM write permission, 0=write protect, 1=allow to be rewritten by USB tool. Bit5: Overcurrent detection voltage threshold OC_LEVEL selection. Default 0=2.4V and weak pull-up, 1=4.1V and weak pull-down. 4.1V is optional when PMOS is used to simplify power control, otherwise 2.4V is used. Bit4& 3: Select how long the power is delayed after turning on to detect overcurrent OC_DELAY. 00: approximately 300uS, for fast opening and small VBUS capacitance. 01: about 3mS. 10: approximately 10mS. 11: About 30mS, suitable for slow opening and large VBUS capacitance. Bit2: Configure the power supply mode SELF_POWER.	57h

		Default 1 = self-powered (recommended), 0 = bus-powered. EEPROM configuration 0 is equivalent to the pin PSELF set low. Bit1: Indicator enable INDICATOR_EN, default 0, 1=enable indicator. Bit0: Configure the power overcurrent protection mode GANG_MODE. Default 1 = overall linked overcurrent detection, 0 = independent overcurrent detection. EEPROM configuration 0 is equivalent to the pin PGANG or LED2 external pull-down.	

3.6 Bus-powered and self-powered

CH334/CH335 support USB bus power and HUB self-power. The bus power comes from the USB uplink port with 500mA or 900mA, 1.5A and other standards. The USB cable internal resistance loss and HUB's own consumption will reduce the power supply to the downlink port, and the downlink port voltage may be low. Self-powered usually comes from the external power port, depending on the external power supply capacity.

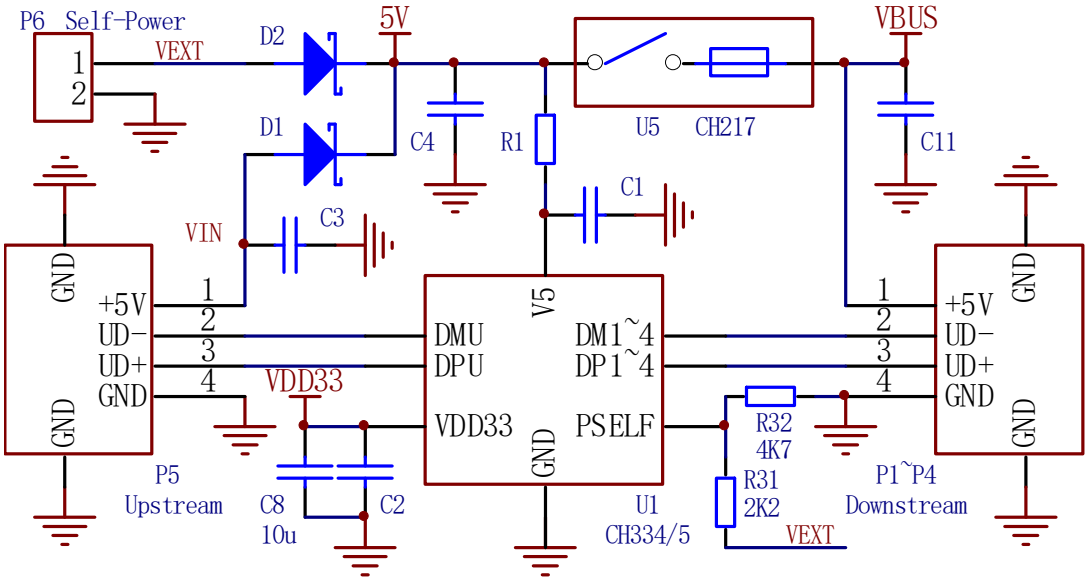
Since the voltages of self-powered and bus-powered are hardly equal, the HUB needs to avoid high currents from direct shorting of the two. In addition, when the USB uplink port is powered off, the HUB also needs to avoid backing up current from the self-powered external power supply to the USB bus and the USB host.

3.6.1 Two-way isolation schematic

Diodes D1 and D2 are used to bi-directionally isolate the VBUS bus power and P6 port external power supply to prevent the two power supplies from backfilling each other, using high power Schottky diodes to reduce their own voltage drop, the downlink port VBUS gets 4.7V or even lower, for illustration purposes only.

Optionally, voltage divider resistors R31 and R32 are used to enable automatic configuration of both bus-powered and self-powered modes.

Figure 3-6-1 Schottky diode bidirectional isolation of VBUS and external power supply

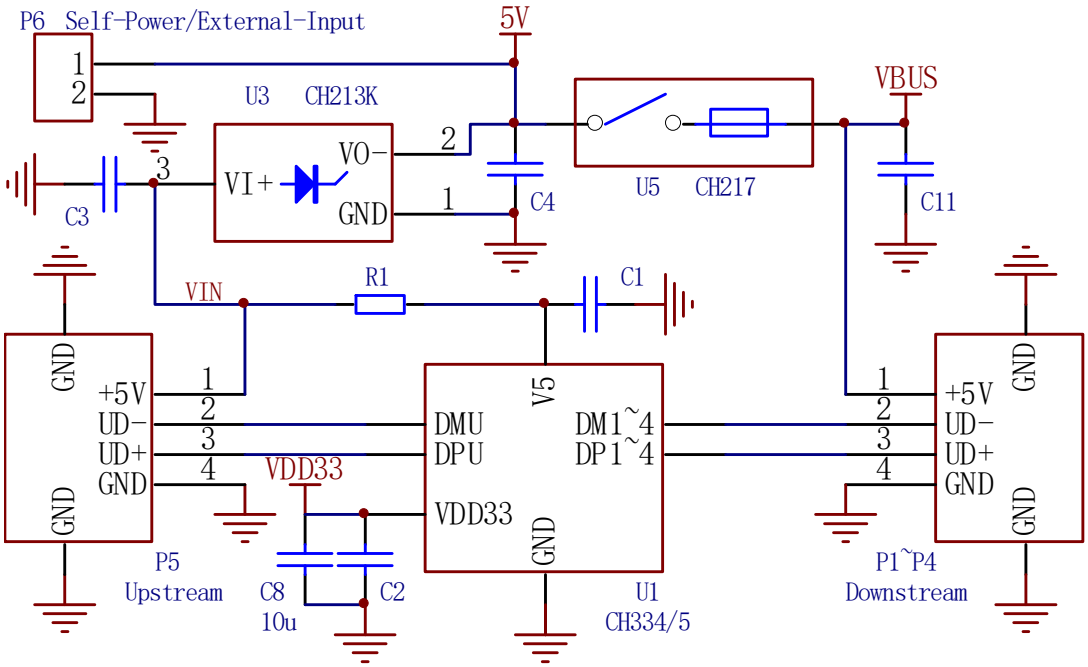


3.6.2 Practical single isolation scheme

The ideal diode functions as a low dropout single conductor, and U3 is used to prevent the external power supply from port P6 from backing up to uplink port VBUS. At 500mA current, the voltage drop of U3 is about one-third of the voltage drop of the Schottky diode, and 4.9V is available at downlink port VBUS.

Optionally, the V5 power supply for CH334/5 in the figure skips U3 to be supplied directly from the uplink port VBUS. In this case, U3 provides simple overcurrent and short-circuit protection for the uplink port VBUS power supply even without the USB current-limited distribution switch CH217.

Figure 3-6-2 The ideal diode isolating VBUS and external power supply



Chapter 4 Parameters

4.1 Absolute maximum value (critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter description	Minimum value	Maximum value	Unit
TA	Ambient temperature at work	-40	85	℃
TS	Ambient temperature during storage	-55	150	℃
V5	LDO input supply voltage (V5 pin to power, GND pin to ground)	-0.4	5.5	V
VDD33	Operating supply voltage (VDD33 pin to power, GND pin to ground)	-0.4	4.0	V
V5I	Voltage on 5V tolerant voltage input pins	-0.4	5.3	V
VUSB	Voltage on USB signal pins	-0.4	VDD33+0.4	V
VGPIO	Voltage on other (3.3V) input or output pins	-0.4	VDD33+0.4	V
VESD	HBM ESD tolerant voltage on USB signal pins	5K	7K	V

4.2 Electrical parameters (test conditions: TA=25℃, V5=5V or V5=VDD33=3.3V)

Name	Parameter description		Minimum value	Typical value	Maximum value	Unit
V5	LDO input supply voltage @ V5	Enable internal LDO	4.6	5.0	5.25	V
	External supply voltage @ V5	No internal LDO required	3.2	3.3	3.4	
VDD33	LDO output voltage @VDD33	Enable internal LDO	3.2	3.3	3.5	V
	External 3.3V supply @VDD33	No internal LDO required	3.2	3.3	3.4	
ILDO	Internal power regulator LDO external load capability				20	mA
ICC	Operating current	Upstream High-speed 4 downstream high-speed		85		mA

		Upstream High-speed	1 downstream high-speed		42		mA
		Upstream High-speed	4 downstream full-speed		25		mA
		Upstream High-speed	1 downstream full-speed		21		mA
		Upstream Full-speed	4 downstream full-speed		20		mA
		Upstream High-speed Upstream Full-speed	No equipment on the downlink 1.5KΩ pull-up included		0.27		mA
ISLP	Deep sleep supply current (without 1.5KΩ pull-up) Or: own sleep power current (not connected to USB host)				0.07	0.3	mA
VIL	Low level input voltage on pins other than overcurrent detection			0		0.8	V
VIH	High level input voltage for pins other than overcurrent detection			2.0		VDD33	V
VILRST	Low input voltage on the RESET# pin			0		0.75	V
VIX	Error of overcurrent detection voltage threshold OC_LEVEL				±0.2		V
VOL	Low Level Output Voltage	LED pin, draws 15mA current			0.5	0.6	V
		PWREN# pin, draws 4mA current			0.5	0.6	V
VOH	High level Output Voltage	LED pin, 10mA output current		VDD33-0.6	VDD33-0.5		V
		PWREN# pin, output 1mA current		VDD33-0.6	VDD33-0.5	4.3	V

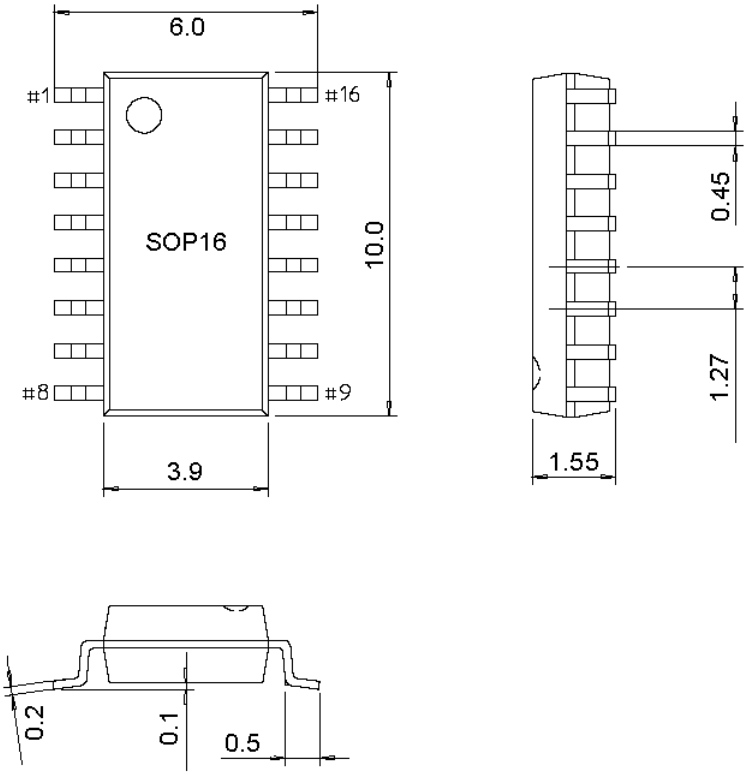
IPU	Pull-up current	LED1/2/3/PSELF/PGANG pins	16	40	80	uA
IPUOC	Pull-up current	OVCUR# pins	8	14	22	uA
IPDOC	Pull-down current	OVCUR# pins	2	5	40	uA
Vlvr	Voltage threshold for power supply low voltage reset		2.4	2.9	3.2	V

Chapter 5 Package information

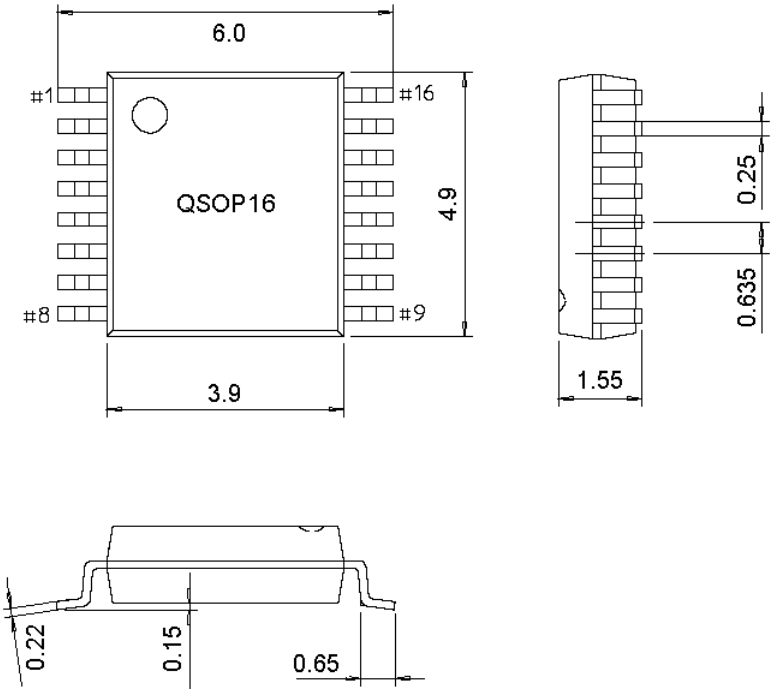
Note: The unit of dimensioning is mm (millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

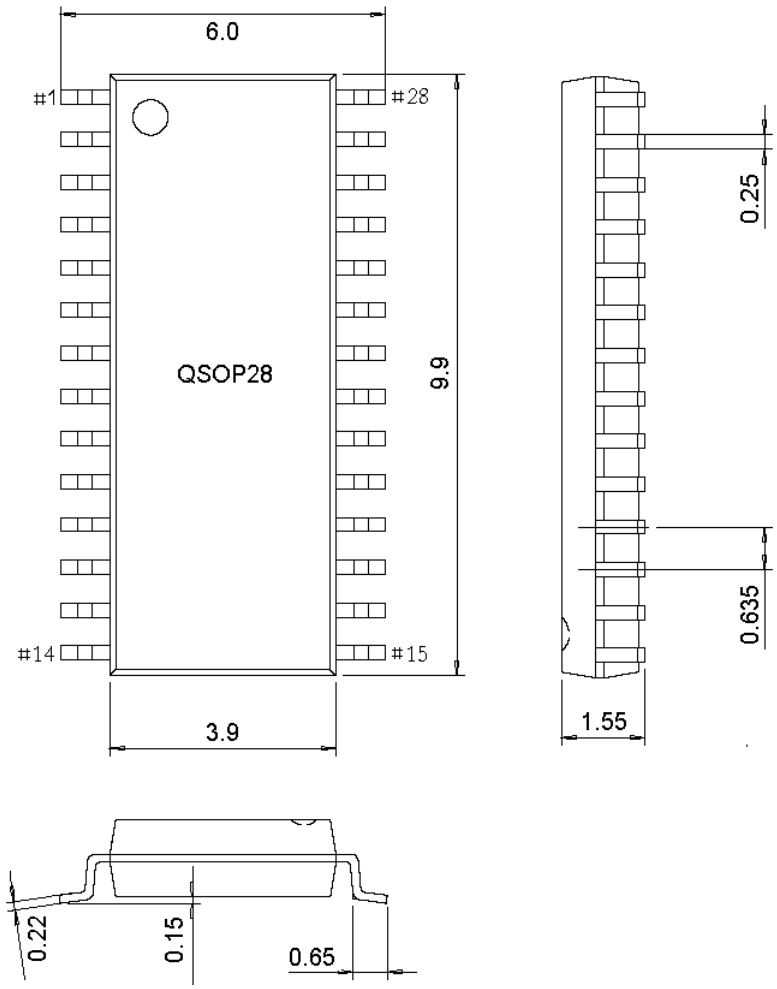
5.1 SOP16



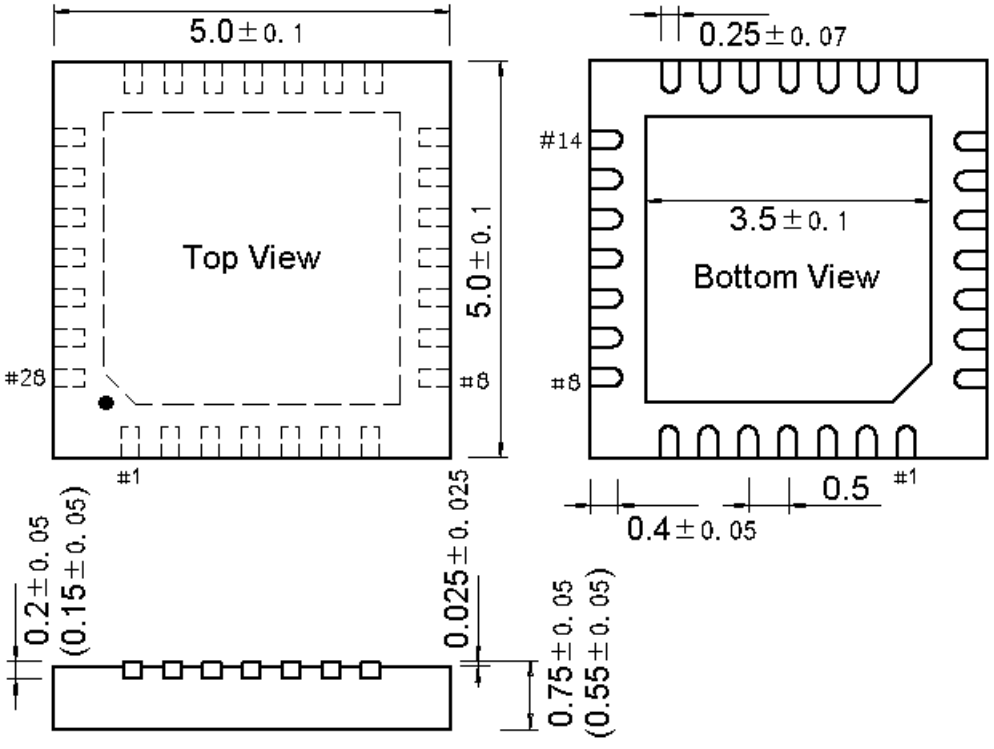
5.2 QSOP16



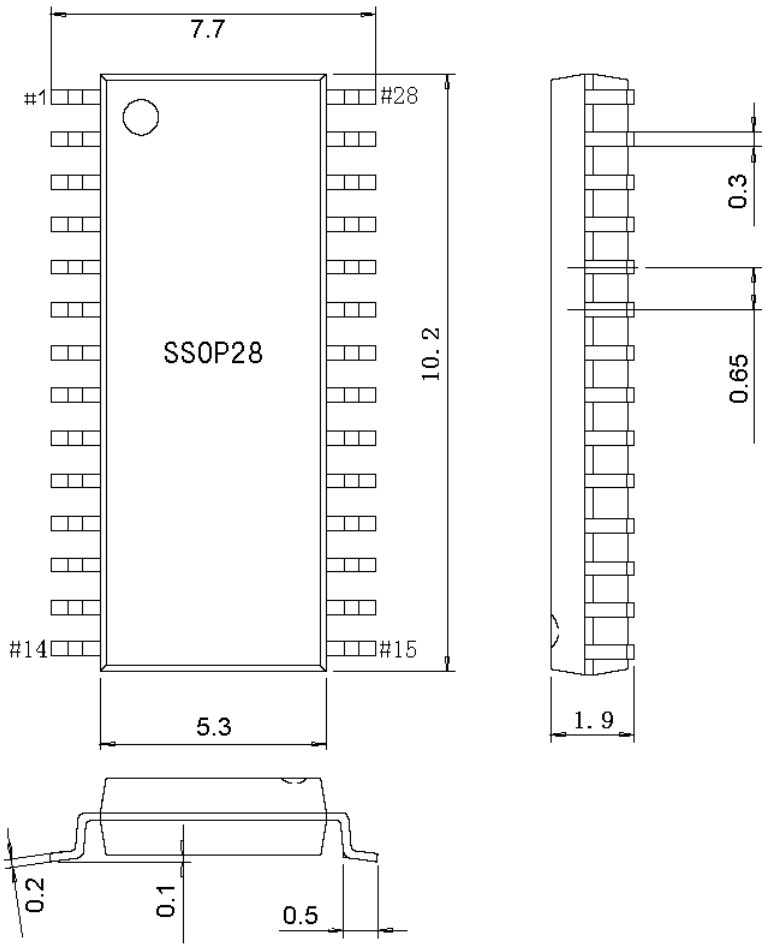
5.3 QSOP28



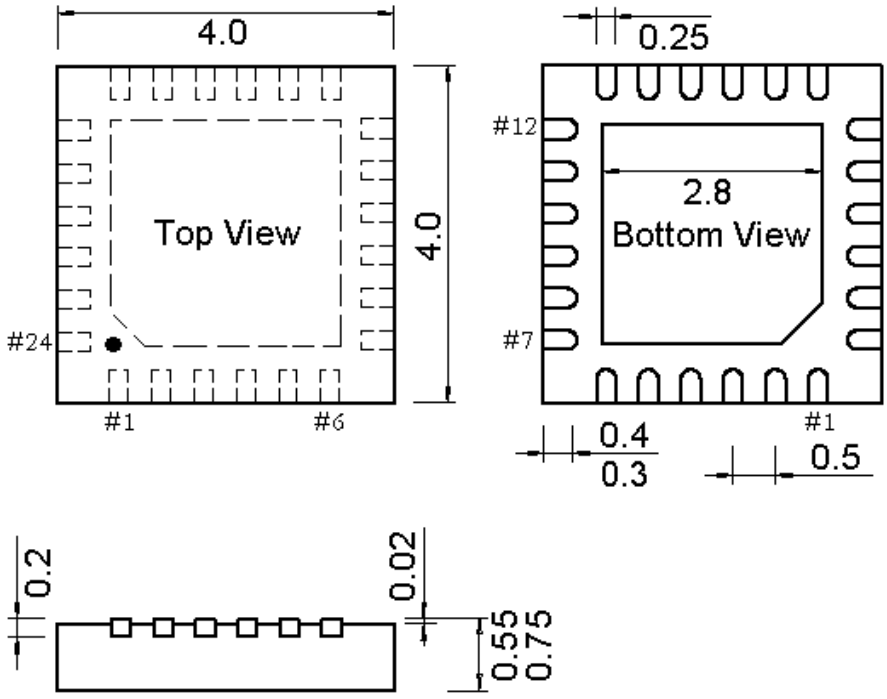
5.4 QFN28_5x5



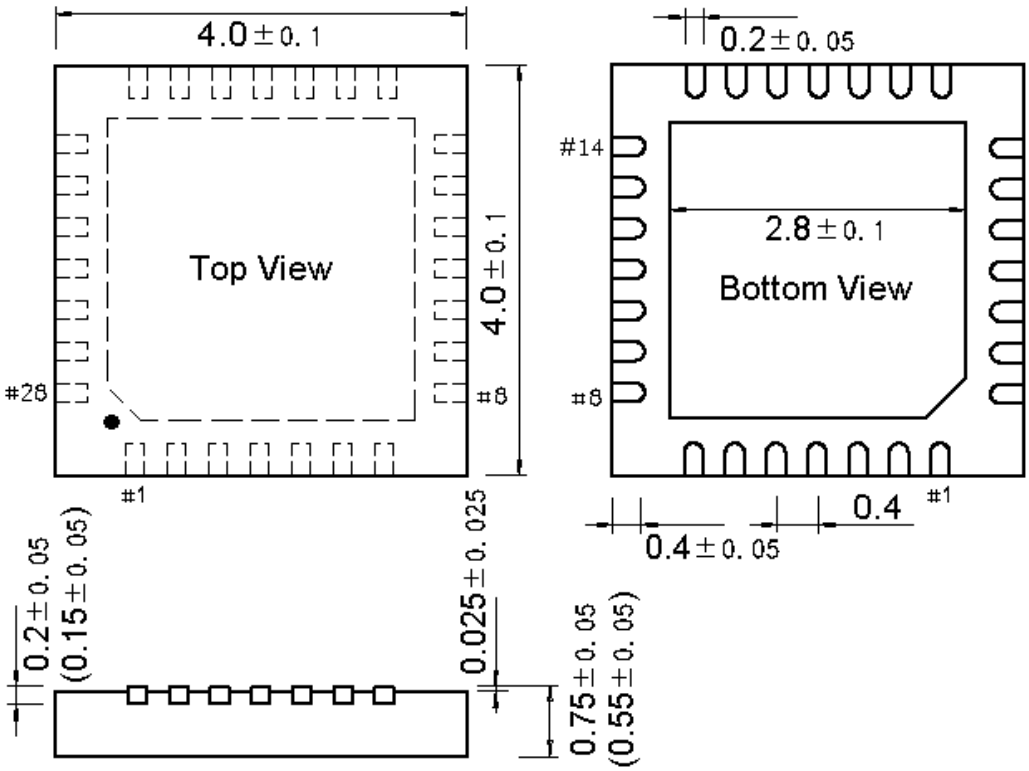
5.5 SSOP28



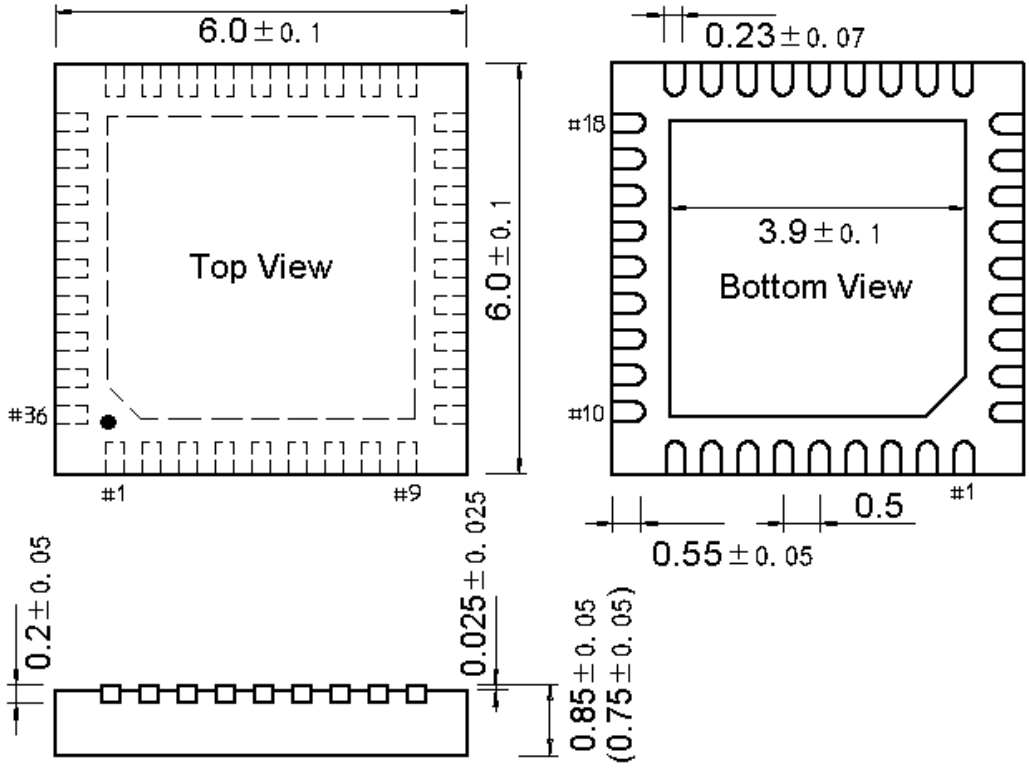
5.6 QFN24_4x4



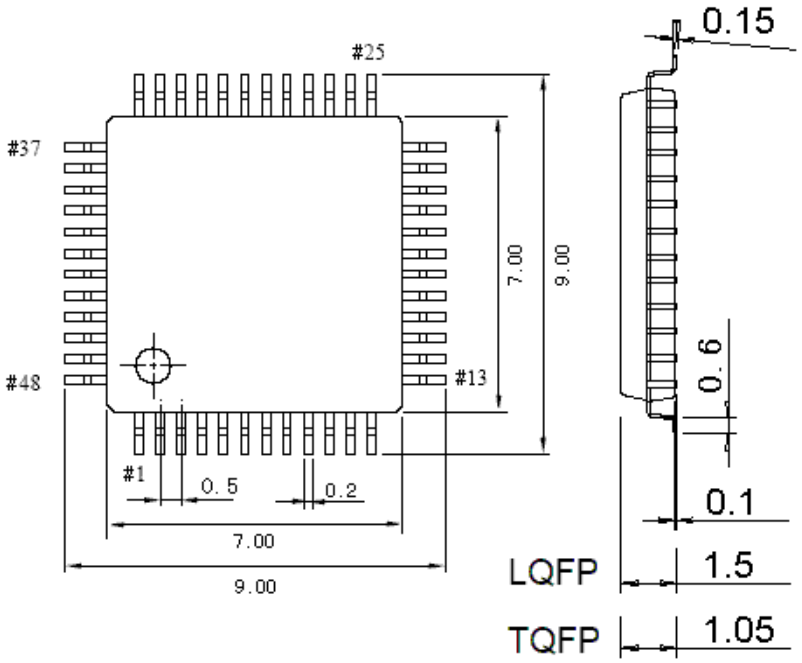
5.7 QFN28_4x4



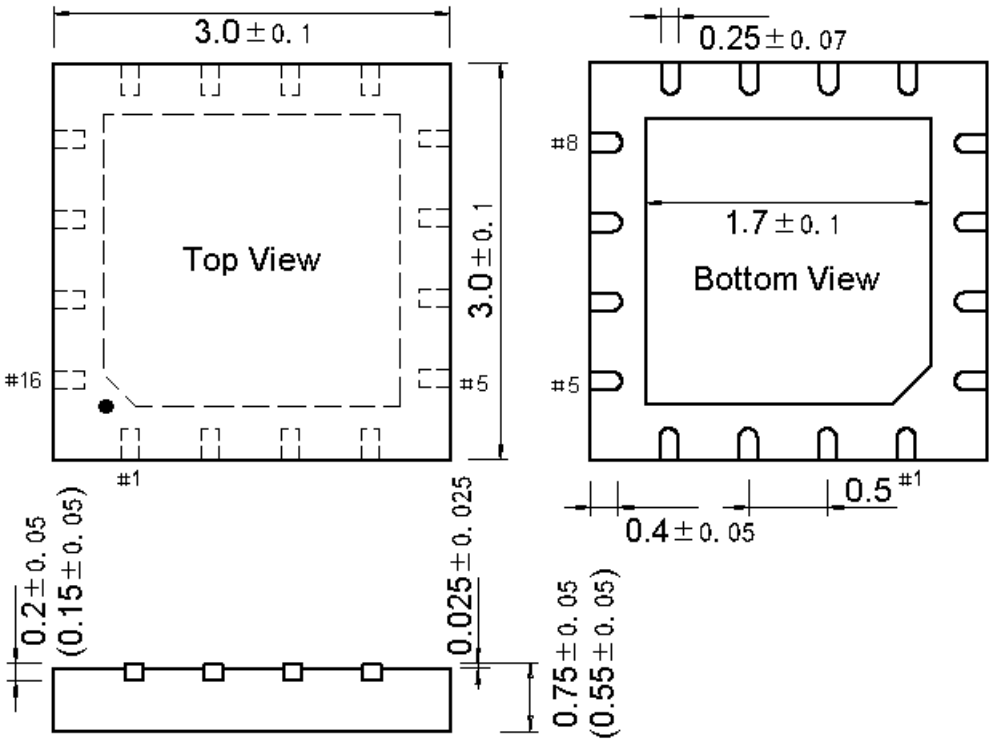
5.8 QFN36_6x6



5.9 LQFP48

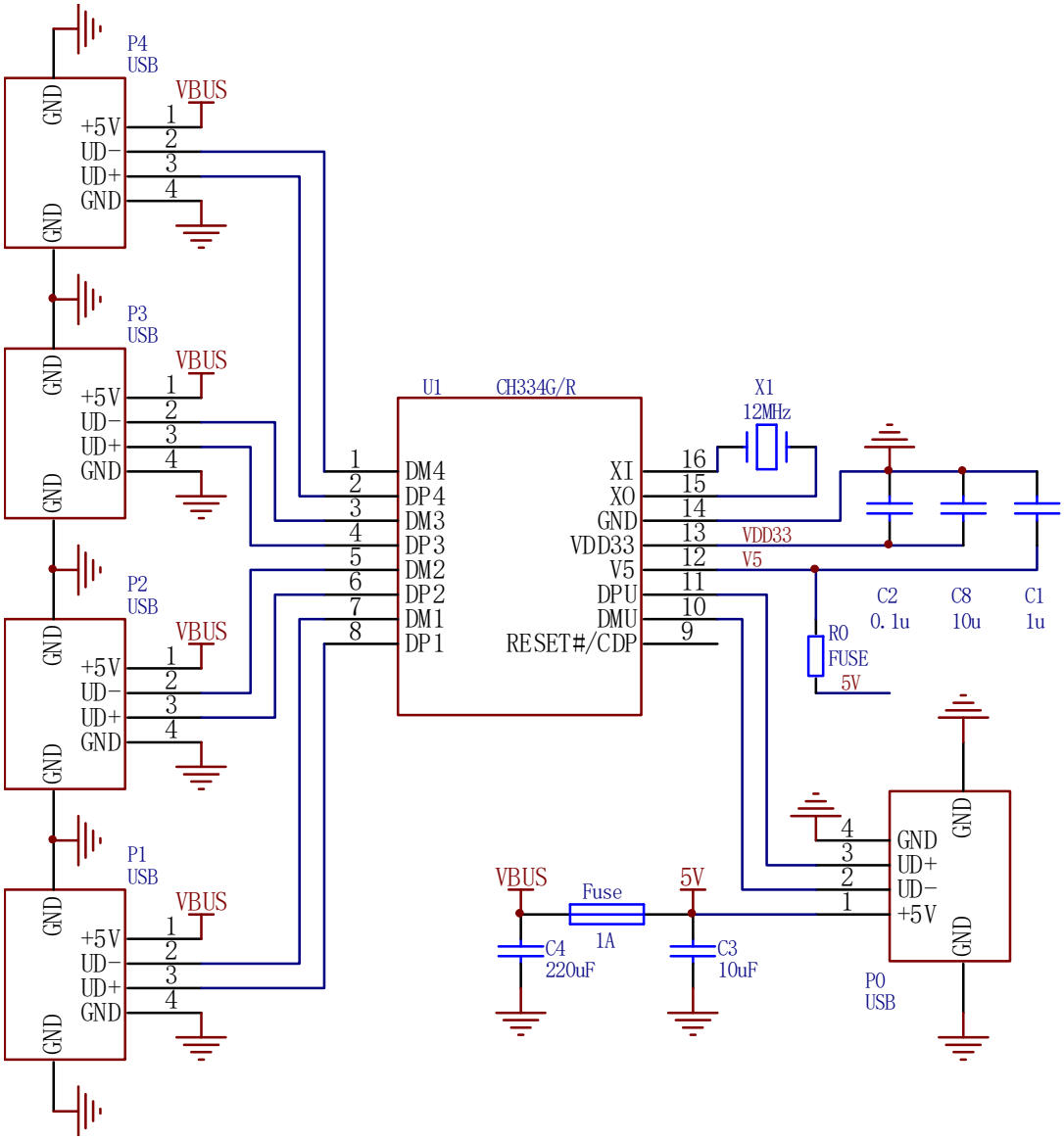


5.10 QFN16_3x3



Chapter 6 Applications

6.1 Simplified application, bus-powered only



R0 is a 100mA fuse resistor, for simplified applications, 0Ω can be used. if there is an overvoltage protection device, it is connected to pin V5.

For the first version of CH334 with 0 in the penultimate 5 digits of the lot number, R0 is changed to 1N4001 or similar diode.

Fuse, the insurance resistor between 5V and VBUS, can be replaced with a USB current-limiting power switch chip for faster protection response and better results.

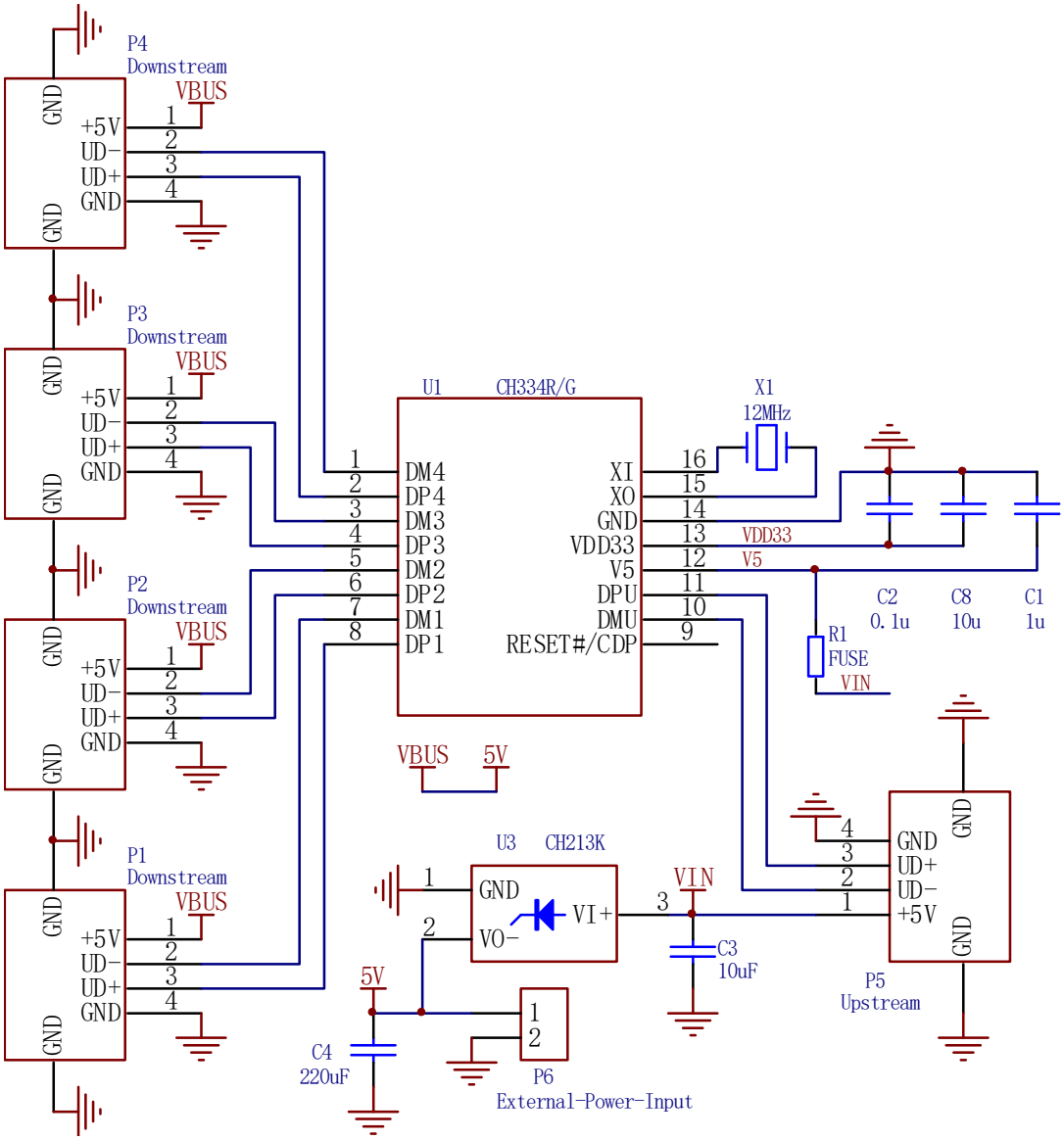
Industrial grade applications are recommended to connect both V5 and VDD33 to an external 3.3V power supply to reduce the maximum power consumption of the HUB chip from 85mA*5V to 85mA*3.3V, which helps to reduce the voltage drop and temperature rise of the HUB chip. It is measured to support extended industrial grade temperature range -40℃~105℃ and available for short term at 125℃ (some parameters will be over). Note that the fuse resistor and USB power switch chip may not support high temperature.

The CH334Q does not have an internal LDO buck regulator and V5 pin, all VDD33 needs to be connected to an external 3.3V supply.

At the moment of powered hot-plug of USB devices on the downlink port, the dynamic load may cause the VBUS and 5V voltages to drop instantaneously, which in turn may generate LVR low-voltage reset and thus the whole HUB disconnected and reconnected. Improvement method. ① Increase the electrolytic capacitor of the 5V power

supply within the allowed range of the specification (increase the capacity of C4 shown in the figure) to alleviate the dip. ② Increase the capacitance of the LDO output of the HUB chip (increase the capacity of C8 shown in the figure, e.g. 22uF). ③ not to use the internal LDO of the HUB, but to externally supply 3.3V to V5 and VDD33 pins, and to increase the capacitance of the 3.3V power supply. ④ Enhance the 5V power supply or change it to self-powered, in addition, improving the quality of the USB cable will also improve the power supply.

6.2 Simplified application with external power supply



The main difference with the circuit in the previous section 6.1 is having an externally powered port P6, U3 is the low voltage drop ideal diode CH213 for avoiding backflow of external power from P6 to the VBUS of uplink port P5, especially in the case when the uplink port, for example, the computer is turned off while P6 is still externally powered. Theoretically U3 can be replaced with a Schottky diode, but it is necessary to choose a device with a lower voltage drop of its own, otherwise it will reduce the output voltage of the VBUS of the downlink port. At 300mA load current, the voltage drop of the Schottky diode is about 0.3V and the voltage drop of the ideal diode is about 0.05V.

Since P6 itself and the external power supply usually have no load, the backflow from P5 to P6 is generally not considered.

The low voltage drop CH213 has simple overcurrent and short-circuit protection with a faster protection response, thus replacing and eliminating the fuse resistor Fuse between 5V and VBUS in the previous section 6.1. The external power supply to which P6 is connected needs to have overcurrent and short-circuit protection itself, otherwise, a

fuse resistor needs to be added between P6 and 5V, or between 5V and VBUS with a USB Otherwise, you need to add a fuse resistor between P6 and 5V, or add a USB power switch chip between 5V and VBUS.

6.3 On-board Embedded HUB

If there is an on-board 3.3V supply, then it is recommended to connect both V5 and VDD33 of the HUB chip to the 3.3V supply. In this case, C8 and C2 can also be combined into a single 1uF capacitor (optional).

If the USB device is also fixed on-board, then the corresponding USB device on the downlink port can also be set to be non-removable, and it is possible to simplify VBUS power control, direct 5V to the USB device, simplify or eliminate overcurrent detection, etc.

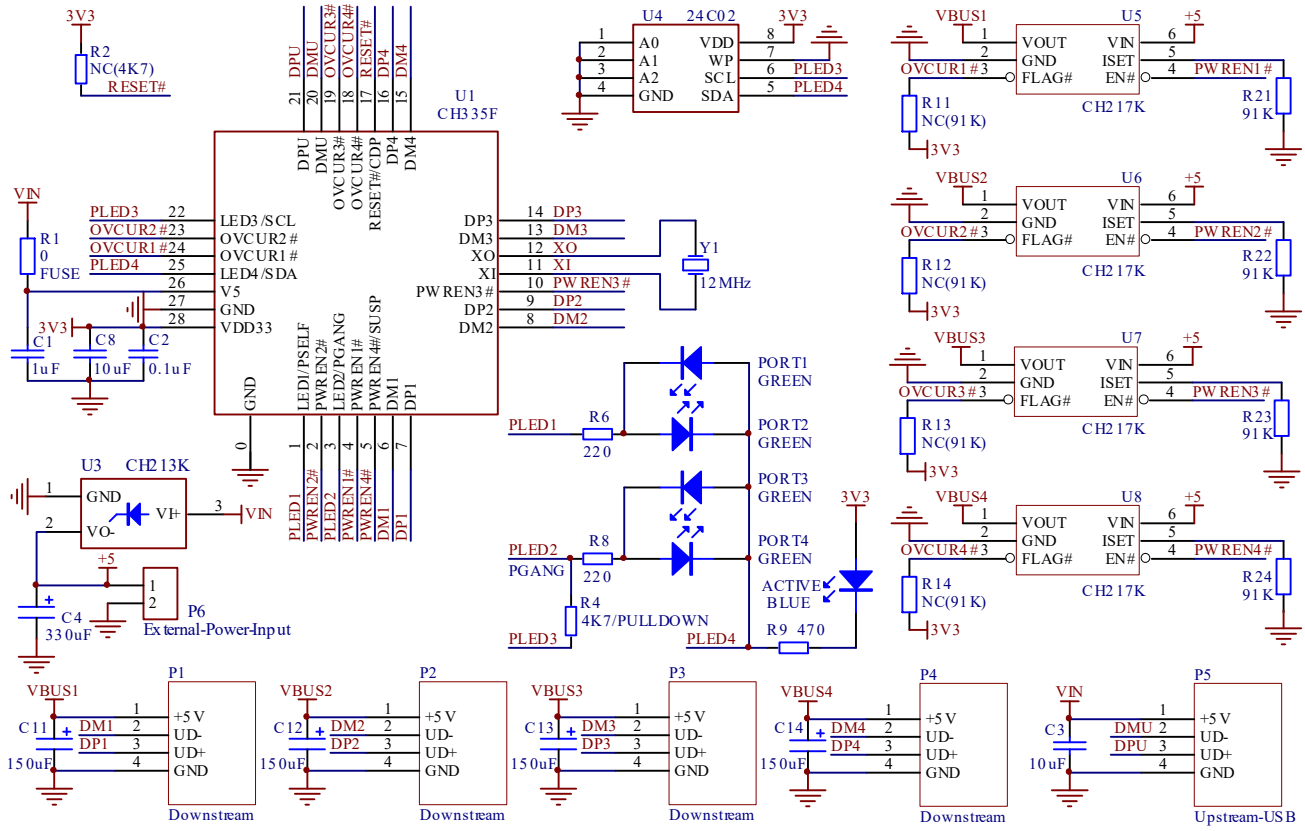
6.4 Independent overcurrent detection applications

The following figure shows the application reference diagram of independent power distribution control and independent overcurrent detection for each port of the HUB, which can be used for computers and HUB hubs. In the diagram, R21 to R24 set the current limit threshold according to the power supply capability, the FLAG# pin of CH217 can generate over-current or over-temperature alarm signal to notify the HUB controller and computer, and the OVCUR# pin of CH334/5 has built-in pull-up resistor (default OC_LEVEL=0).

P6 is the external self-powered input port and the ideal diode U3 is used to avoid backflow of external power to the USB power of the uplink port. If there is no P6 or if anti-backflow is not considered, then U3 is not needed and the connection between VIN and +5V can be shorted.

PCB design needs to consider the actual operating current carrying capacity, VIN, +5V, VOUT (VBUS*) and P6 and each port GND alignment path of the PCB as wide as possible, if there is an over-hole is recommended multiple parallel connection.

It is recommended to add overvoltage protection devices to VIN and ESD protection devices to all USB signals, for example, CH412K, whose VCC should be connected to 3V3.



6.5 Overall overcurrent detection applications

The following diagram shows the application reference diagram of GANG power distribution control and overall overcurrent detection for all ports of the HUB. CH217 is the USB power distribution switch chip that supports overcurrent protection.