CHA6194-QXG

37- 40GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

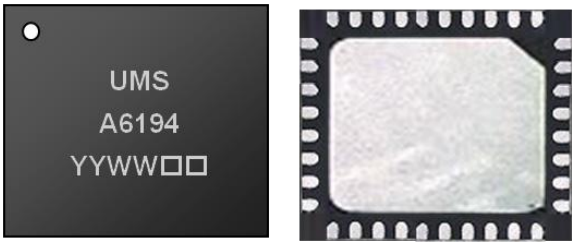
Description

The CHA6194-QXG is a four stage monolithic GaAs high power circuit producing 1.2 Watt output power. It is highly linear with possible gain control and integrates a power detector. ESD protections are included.

It is designed for Point To Point Radio or K-band Sat-Com application.

The circuit is manufactured with a pHEMT process, 0.15µm gate length.

It is supplied in RoHS compliant SMD package.

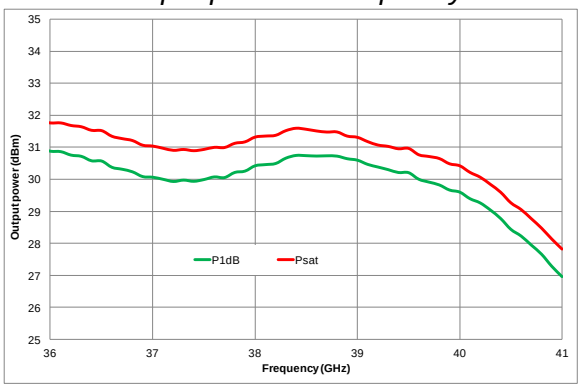


36 lead 6x5 mm QFN package

Main Features

- Broadband performances: 37-40GHz
- 31dBm saturated power
- 38dBm OIP3
- 20dB gain
- DC bias: Vd = 6.0Volt @ Id = 0.8A
- QFN5x6
- MSL3

Output power vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	37		40	GHz
Gain	Linear Gain	18	20	23	dB
Psat	Saturated output power	30	31		dBm
OIP3	Output IP3	36.5	38		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	37		40	GHz
Gain	Small Signal Gain	18	20	23	dB
ΔG	Gain variation in temperature		± 0.04		dB/°C
Psat	Saturated Output Power	30	31		dBm
P1dB	Output power at 1dB compression	29	30		dBm
OIP3	Output IP3	36.5	38		dBm
PAE	PAE at saturation		18		%
CG	Gain regulation range		15		dB
Rlin	Input Return Loss		13		dB
Rlout	Output Return Loss		13		dB
Dr	Detection dynamic range(for output power detection up to Psat)		32		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		5 to 2500		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		0.8		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
Vd	DC Drain bias voltage without RF (2)	8	V
Id	Drain bias quiescent current (2)	1000	mA
Vg	Gate bias voltage@ (2)	-2 to 0	V
Pin	Maximum Input Power (2)	+15	dBm
Tj	Maximum junction temperature in operating conditions	200	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) For an operating temperature of 25°C

Temperature range

Symbol	Parameter	Values	Unit
Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	7	DC Drain voltage 1st stage	6.0	V
Vd2	6	DC Drain voltage 2nd stage	6.0	V
Vd3	4, 23	DC Drain voltage 3rd stage	6.0	V
Vd4	2, 25	DC Drain voltage 4th stage	6.0	V
Vg1	19	DC Gate voltage 1st stage	-0.65	V
Vg2	21	DC Gate voltage 2nd stage	-0.65	V
Vg3	5, 22	DC Gate voltage 3rd stage	-0.65	V
Vg4	3, 24	DC Gate voltage 4th stage	-0.65	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 6V Id= 800mA Pdiss= 4.8W	171	17.8	5.3E+07

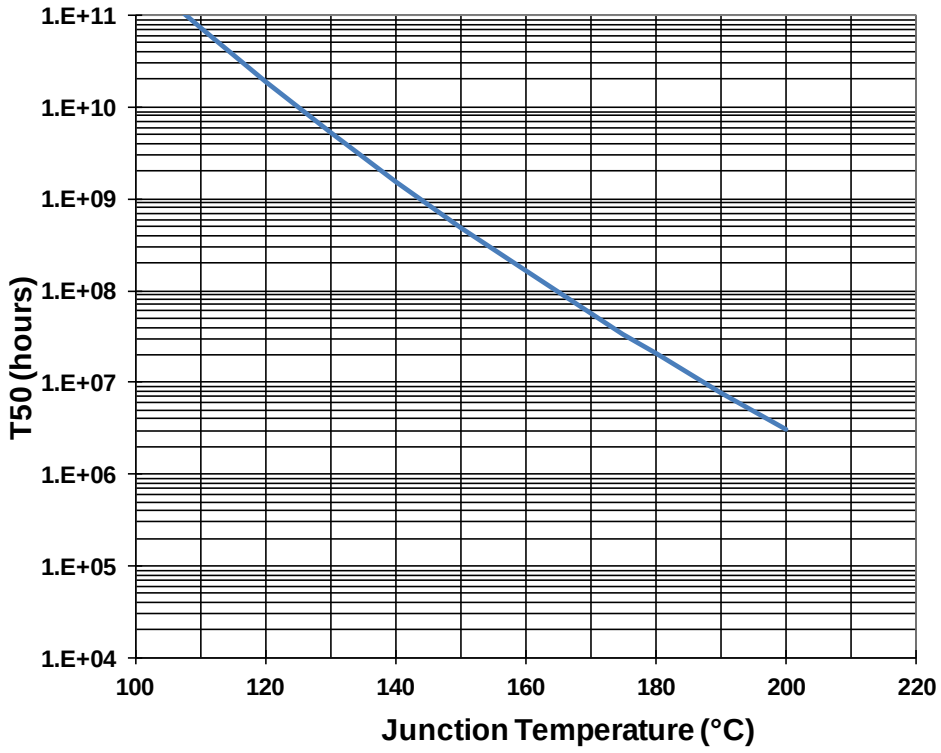
(1) Assuming 85°C Tcase

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (2) Thermal Resistance (Junction to Case)	Vd= 6V Id= 800mA Pdiss= 4.8W	186	18.6	1.4E+07

(2) Assuming 95°C Tcase

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (3) Thermal Resistance (Junction to Case)	Vd= 6V Id= 900mA Pdiss= 5.4W	187	18.1	1.0E+07

(3) Assuming 90°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 800mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
5	-0.848	58.7	-78.174	-64.7	-69.773	6.1	-0.458	77.4
6	-1.122	22.5	-58.913	161.6	-76.522	-115.1	-0.635	52.3
7	-1.727	-27.6	-45.260	113.9	-72.227	88.0	-0.957	23.7
8	-2.305	-97.5	-34.505	50.1	-66.501	39.4	-1.613	-11.9
9	-2.017	-169.5	-23.834	-27.3	-60.368	-92.6	-3.026	-62.0
10	-1.719	133.3	-17.541	-113.8	-57.155	144.6	-4.184	-136.0
11	-1.699	90.6	-13.693	144.3	-53.686	70.0	-3.170	144.1
12	-2.040	56.7	-12.504	62.2	-55.010	3.1	-1.983	88.3
13	-2.571	27.9	-11.737	-14.7	-55.764	-39.6	-1.258	49.1
14	-3.060	3.3	-11.646	-87.6	-59.179	-66.7	-1.002	18.6
15	-3.508	-18.5	-11.675	-156.1	-74.614	-164.1	-0.846	-8.9
16	-3.735	-38.8	-12.726	130.9	-67.969	-27.3	-0.824	-34.4
17	-3.848	-58.4	-14.888	68.4	-66.320	150.5	-0.820	-59.4
18	-3.912	-76.7	-17.829	5.8	-54.010	62.9	-0.879	-84.0
19	-3.974	-93.7	-20.842	-29.7	-54.118	10.4	-0.963	-108.6
20	-4.100	-111.1	-21.495	-64.3	-59.533	-43.8	-1.009	-133.1
21	-4.284	-127.3	-20.461	-106.8	-51.661	4.6	-1.077	-158.5
22	-4.493	-144.4	-20.767	-166.1	-50.166	-19.8	-1.144	176.5
23	-5.047	-160.8	-24.635	131.9	-50.208	-29.2	-1.232	148.6
24	-5.677	-179.4	-32.559	105.5	-46.109	-60.2	-1.343	119.5
25	-6.576	160.5	-34.751	146.0	-48.584	-95.9	-1.382	87.0
26	-7.611	138.2	-25.865	142.4	-48.804	-111.0	-1.533	51.9
27	-9.026	114.2	-18.211	110.4	-53.102	-97.9	-1.697	13.5
28	-10.432	84.8	-11.171	67.0	-48.146	-83.4	-2.076	-26.6
29	-11.462	52.8	-4.033	16.9	-43.460	-105.3	-2.614	-68.4
30	-12.151	18.0	3.183	-42.0	-40.803	-128.6	-3.767	-112.1
31	-12.392	-17.8	10.493	-114.2	-39.522	-155.6	-6.784	-154.8
32	-14.074	-74.7	16.821	158.0	-41.853	163.5	-11.689	-165.5
33	-20.113	-163.1	20.193	59.6	-48.557	126.2	-8.740	-176.8
34	-16.515	103.7	21.637	-32.6	-58.779	157.1	-8.201	141.5
35	-11.630	56.4	22.299	-120.9	-51.625	-130.7	-9.119	109.3
36	-8.811	16.2	22.904	150.2	-40.404	-141.2	-8.759	73.3
37	-9.518	-17.5	22.591	63.2	-36.969	-172.4	-10.012	29.4
38	-14.804	-37.3	22.190	-26.3	-35.717	154.6	-14.730	-20.6
39	-21.807	8.8	21.602	-118.3	-35.336	136.7	-24.035	-108.2
40	-13.007	22.7	20.100	150.4	-33.514	117.5	-15.182	116.8
41	-16.168	-79.4	20.158	56.2	-29.583	95.2	-13.109	104.6
42	-2.320	96.3	16.630	-84.0	-29.616	21.5	-2.140	83.2
43	-1.587	44.0	5.452	175.1	-36.809	1.0	-1.539	39.6
44	-1.476	23.4	-4.040	99.2	-41.728	-3.1	-1.423	16.0
45	-1.113	7.6	-12.822	32.2	-41.809	10.1	-1.120	-2.7

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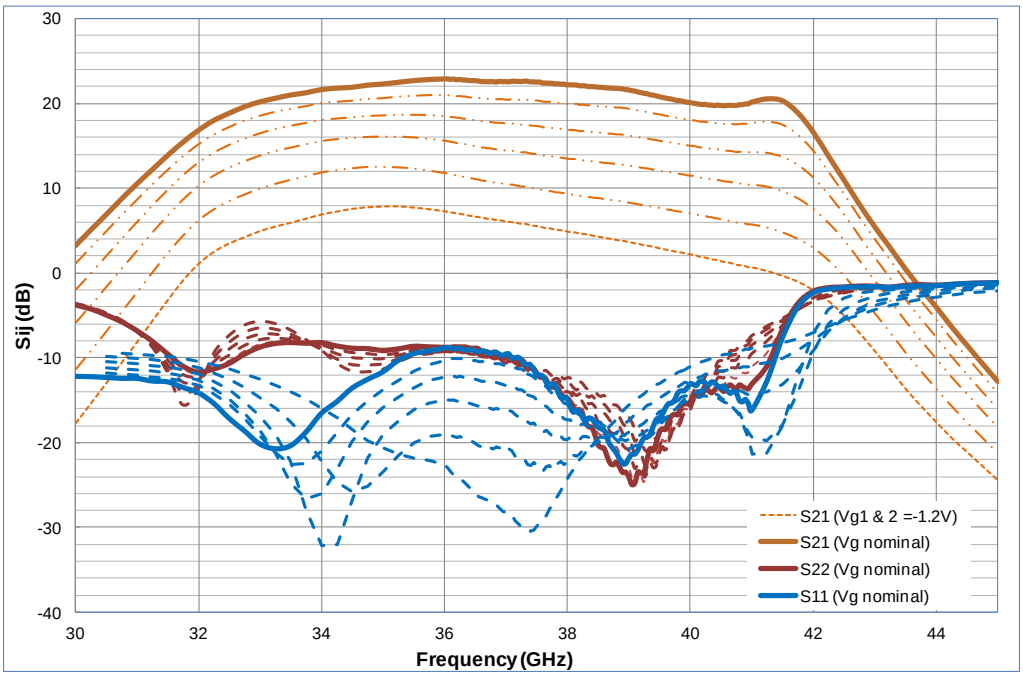
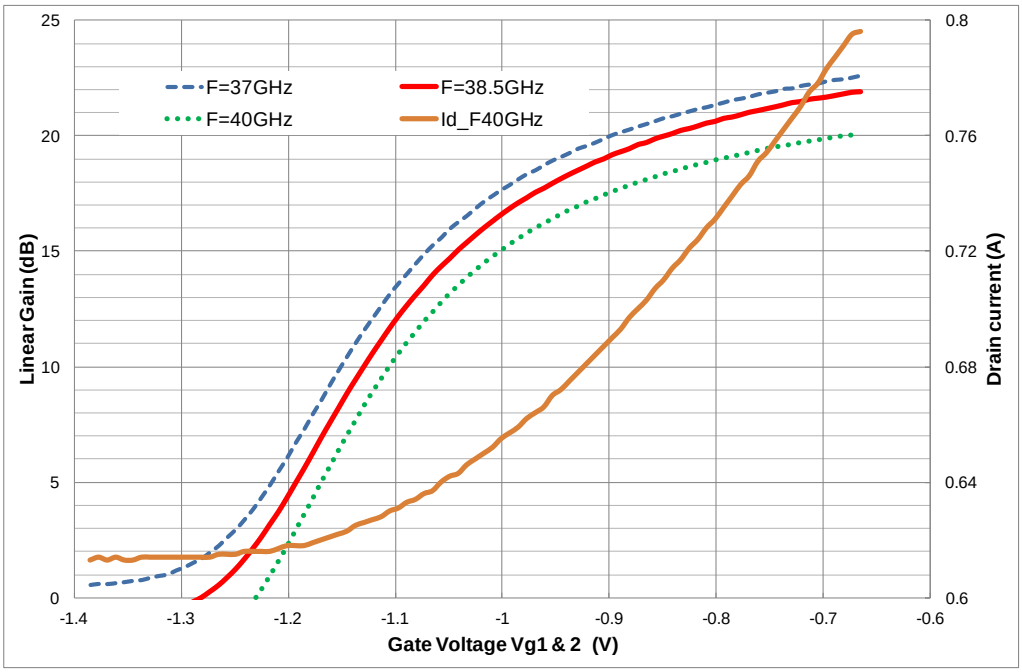
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 800mA
Measurement performed in the access plans of the QFN, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

Gain & Return Loss versus Frequency & Gate Voltage (Vg1 & 2)



Gain control & current versus Gate Voltage (Vg1 & 2)



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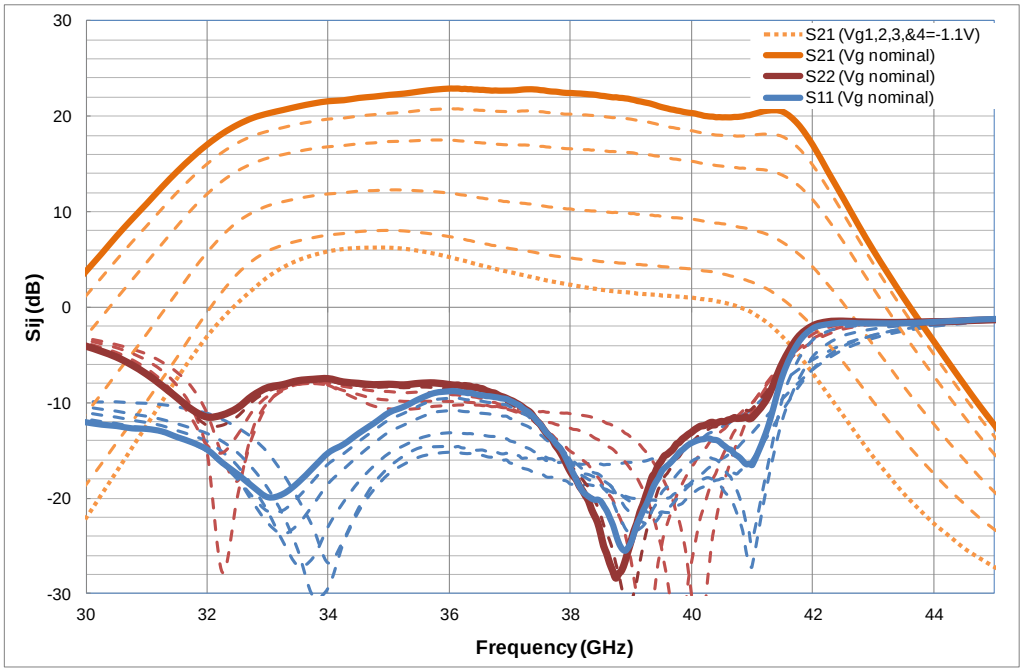
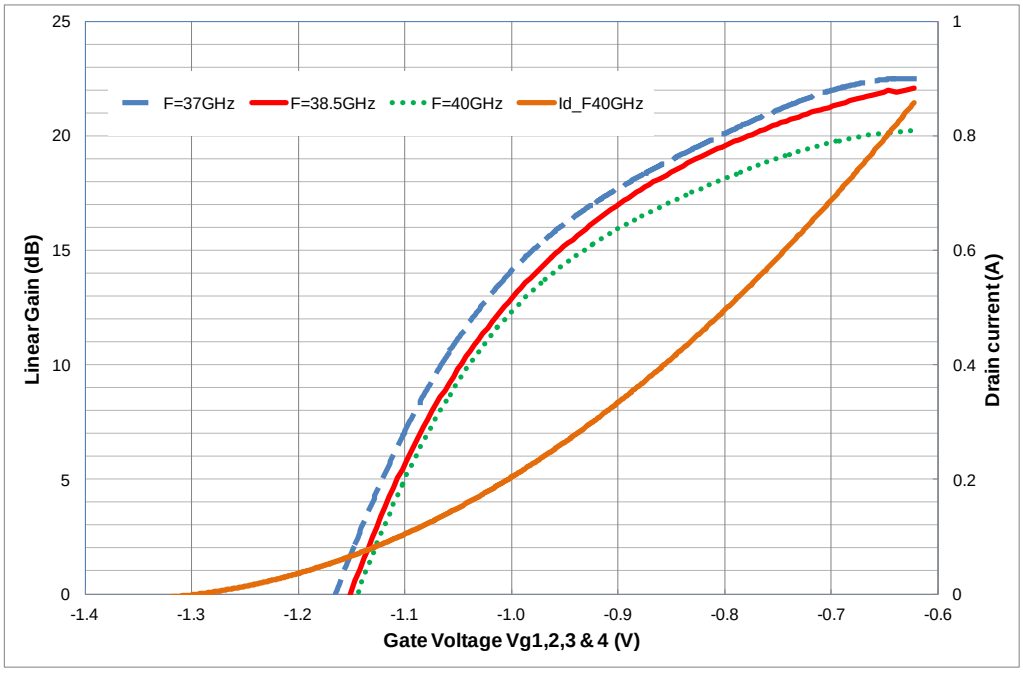
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 800mA

Gain & Return Loss versus Frequency & Gate Voltage (Vg1,2,3,4)



Gain control & current versus Gate Voltage (Vg1,2,3,4)



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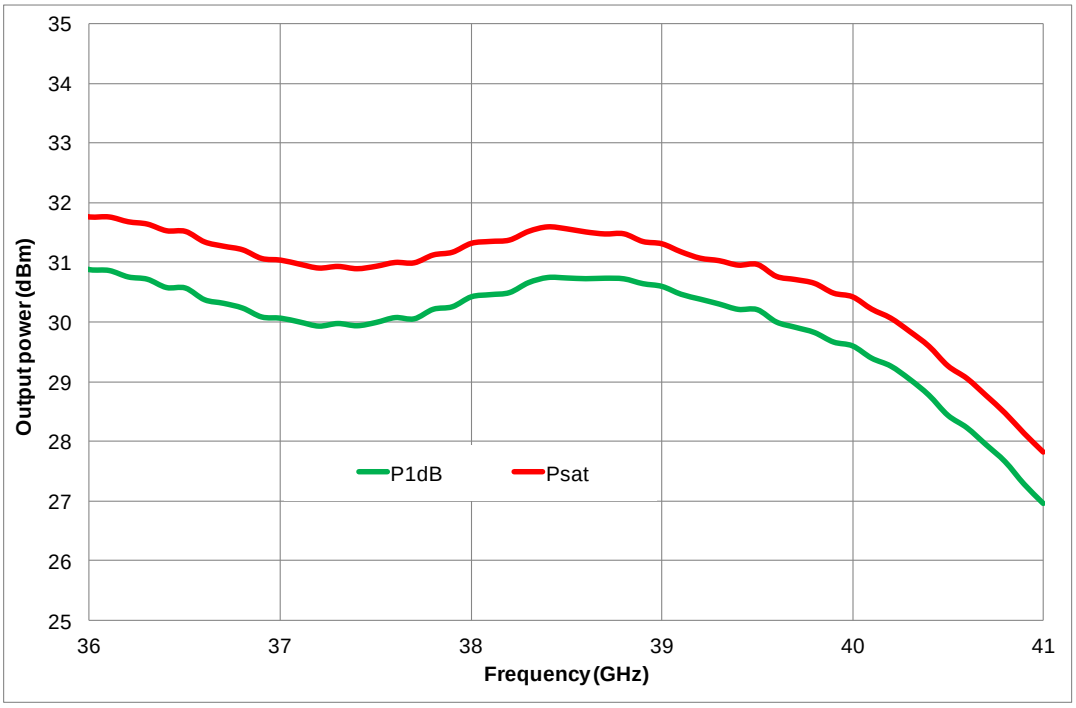
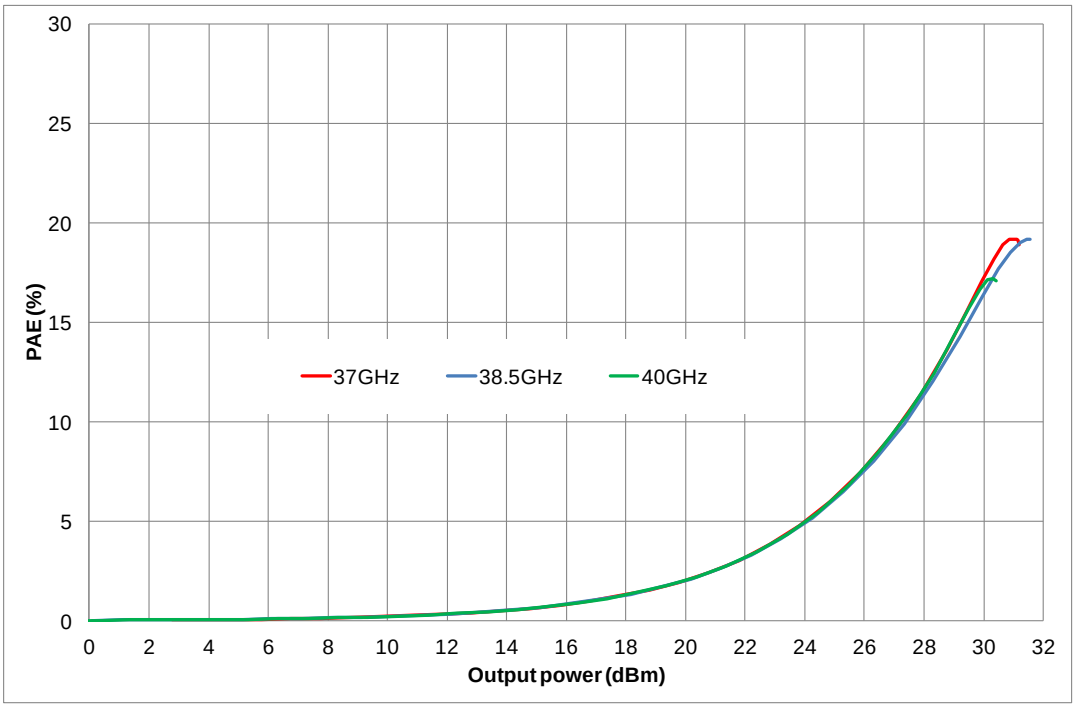
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 800mA

Output Power versus Frequency



PAE versus Output power



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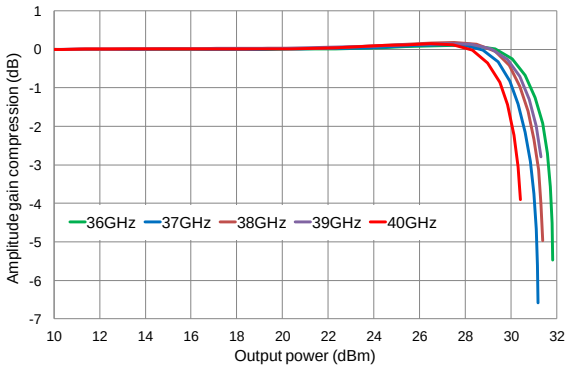
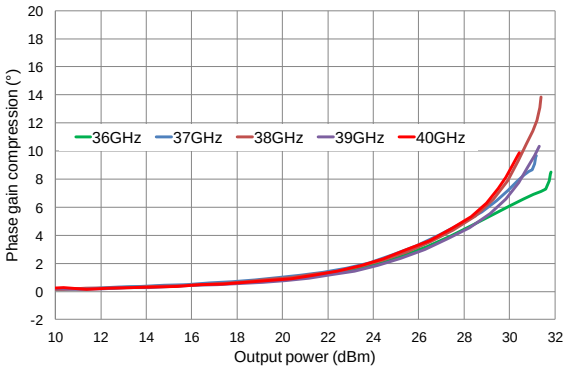
Typical Board Measurements

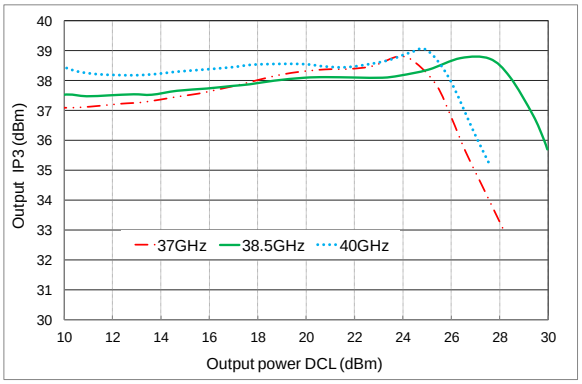
Tamb.= +25°C, Vd = +6.0V, Id = 800mA

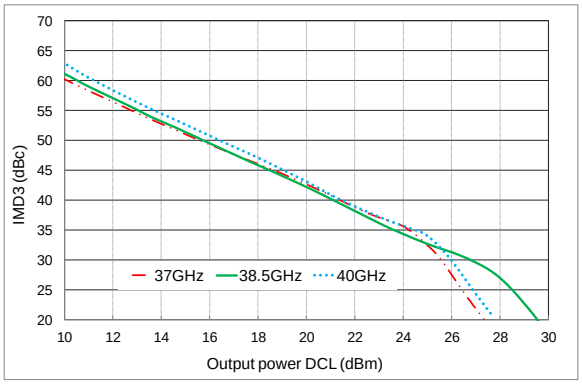
Amplitude & Phase variation versus Output Power



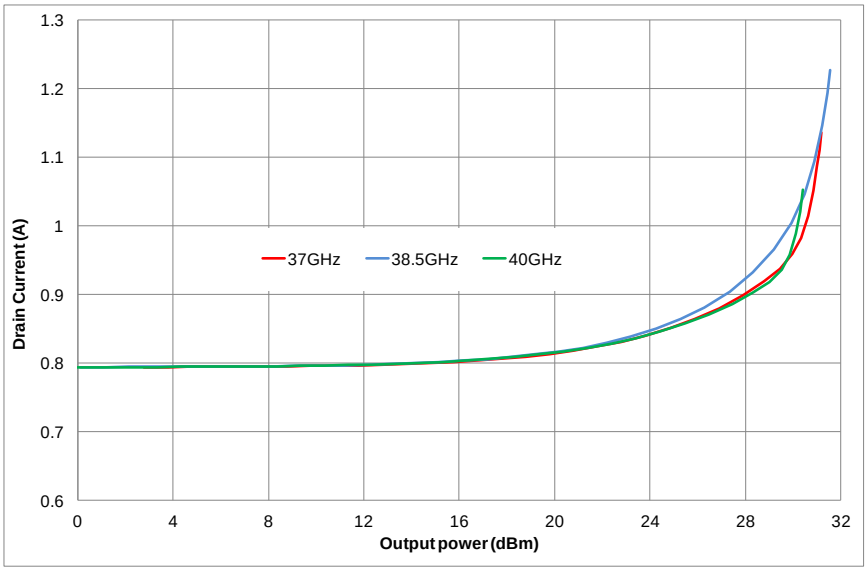


Output IP3 & IMD3 versus Output Power





Total Drain Current versus Output Power



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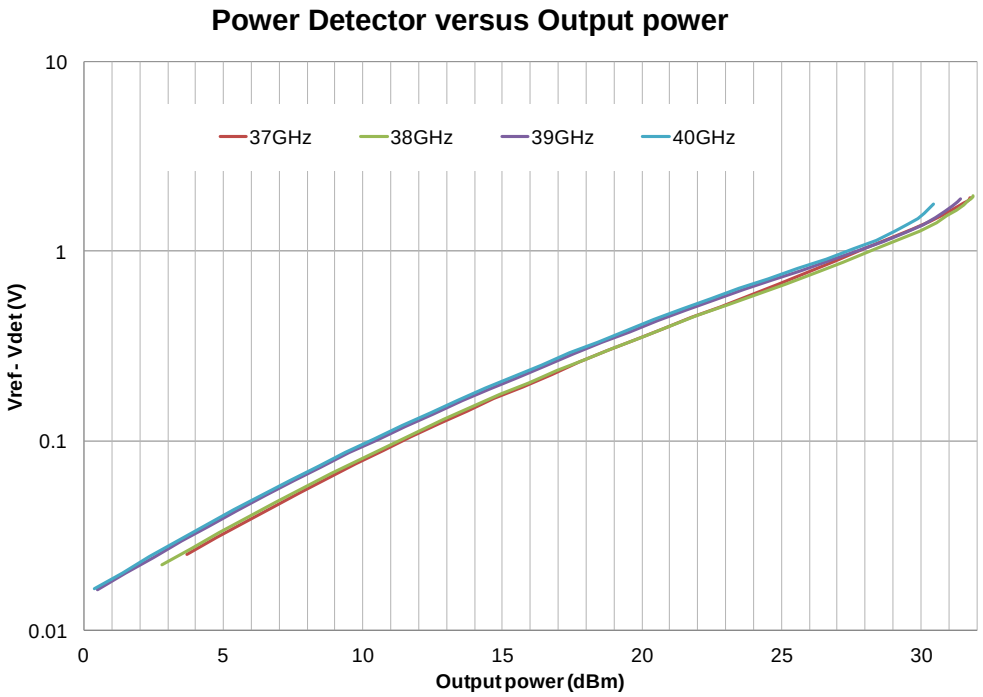
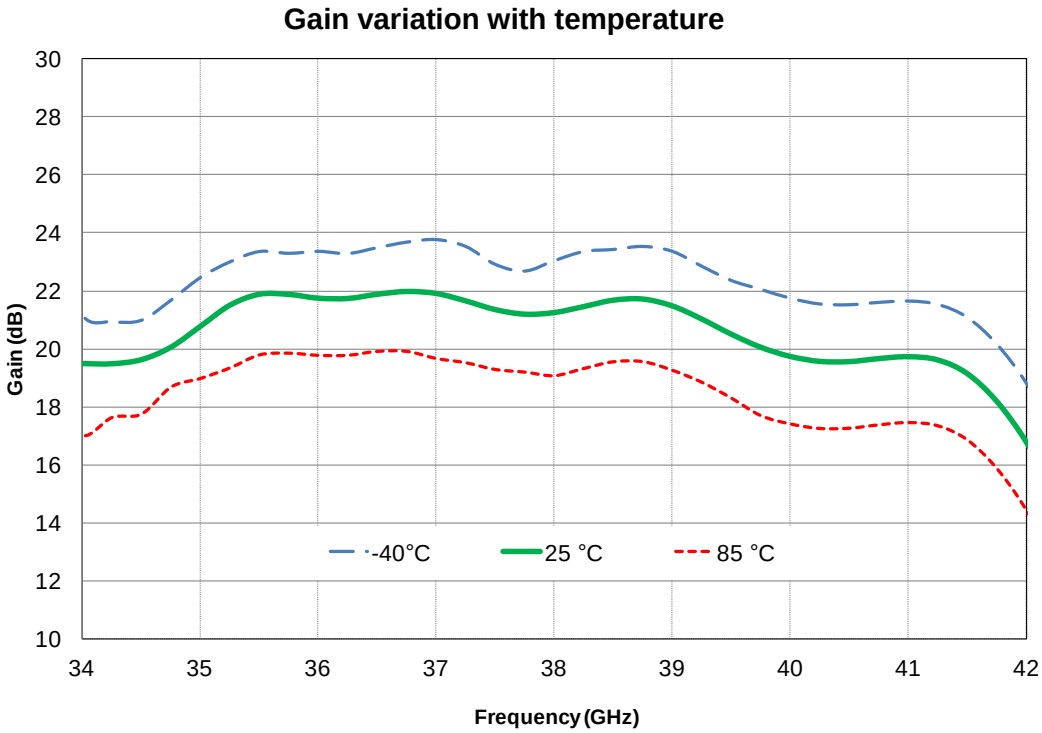
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 800mA





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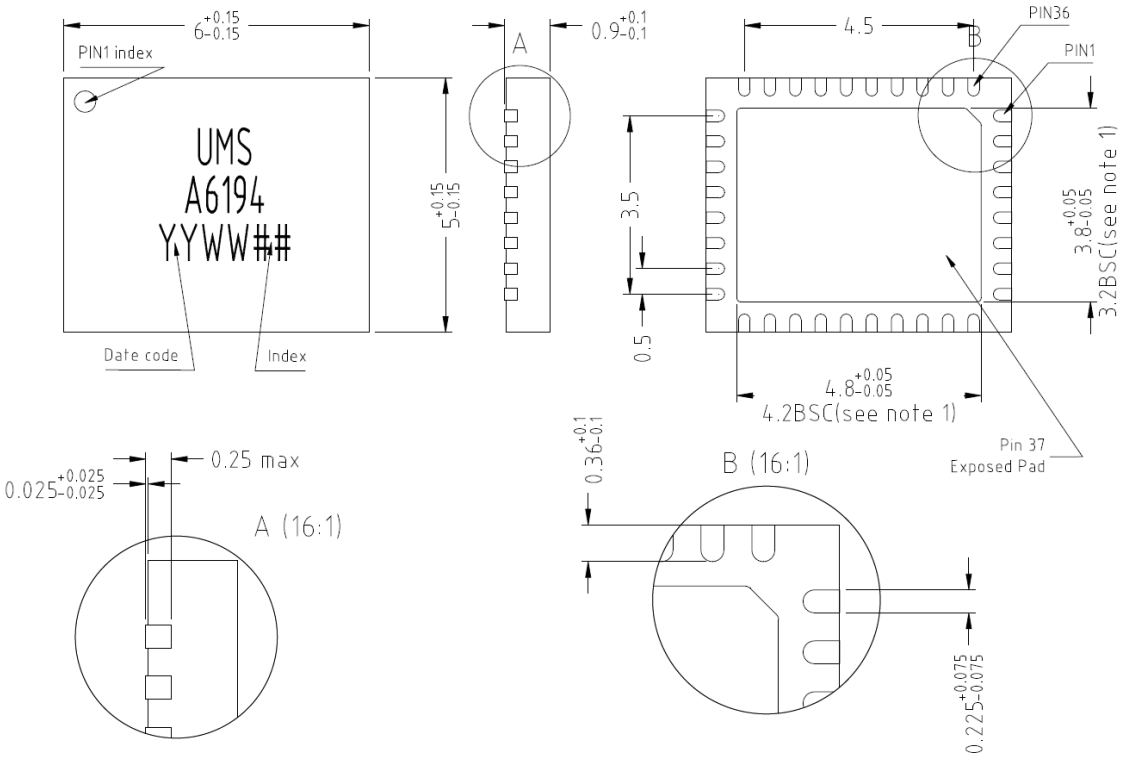
Package outline (1)



Matte tin, Lead Free (Green)		1- DET	13- Gnd(2)	25- Vd4
Units :	mm	2- Vd4	14- RF in	26- NC
From the standard :	JEDEC MO-220 (VGGD)	3- Vg4	15- Gnd(2)	27- Gnd(2)
		4- Vd3	16- NC	28- NC
37- GND		5- Vg3	17- NC	29- NC
		6- Vd2	18- NC	30- Gnd(2)
		7- Vd1	19- Vg1	31- RF out
		8- NC	20- NC	32- Gnd(2)
		9- NC	21- Vg2	33- NC
		10- NC	22- Vg3	34- NC
		11- NC	23- Vd3	35- NC
		12- NC	24- Vg4	36- REF

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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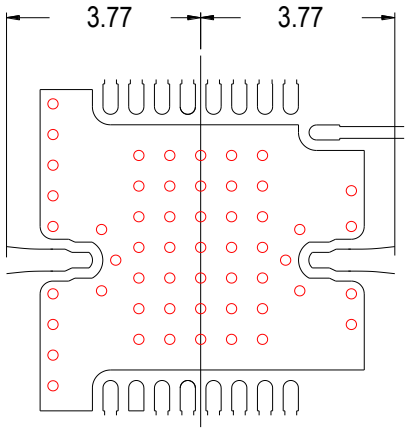
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.77mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



ESD sensitivity

Standard	Value
JEDEC JESD22 A114D	HBM Class 0 (200V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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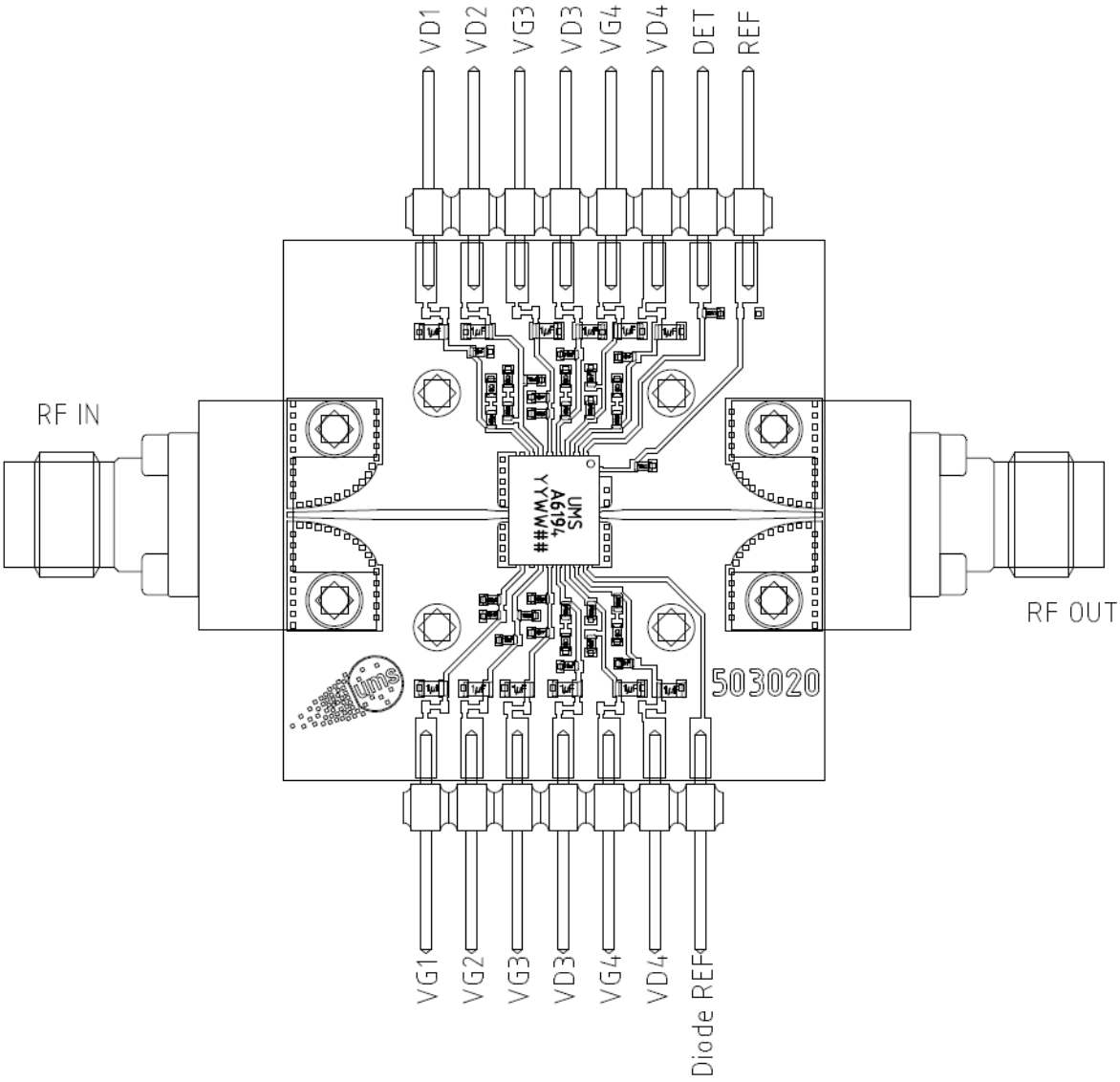
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350B / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



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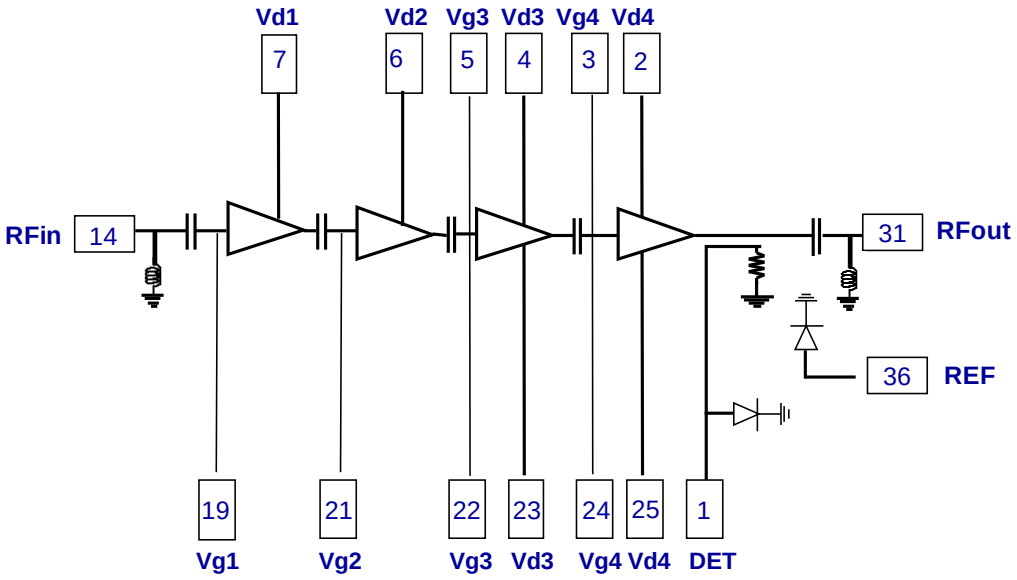
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1µF) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

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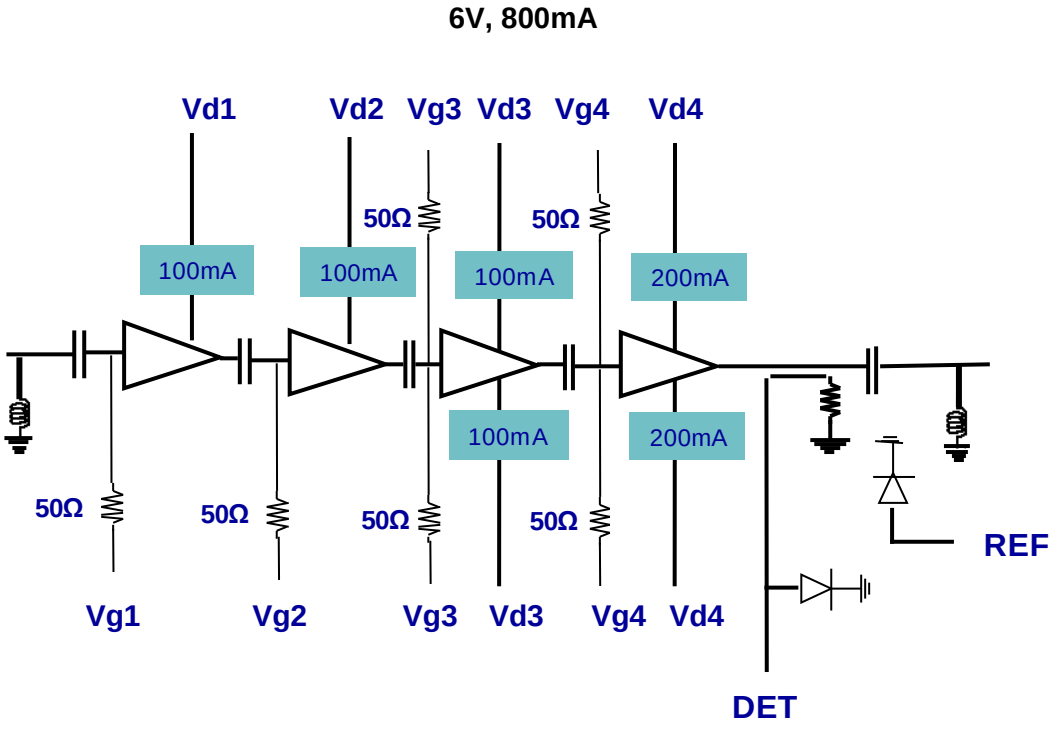
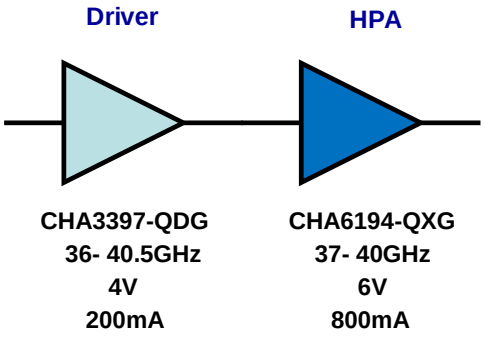
DC Schematic



Recommended UMS Power chain

The CHA6194-QXG is recommended with the CHA3397-QDG as driver.
Total Gain: 41dB
Gain control: 30dB for the two amplifiers.
For more information about CHA3397-QDG, see our web site.



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x5 package:	CHA6194-QXG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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