PRELIMINARY DATASHEET

CGY2130UH

500mW 37-41 GHz Power Amplifier

DESCRIPTION

The CGY2130UH is a GaAs PHEMT Power Amplifier with output power of 27dBm (500mW) and more than 22dB of gain over the frequency range 37 to 41 GHz.

The 1dB Compression point is 26 dBm with excellent linearity delivering an OIP3 of 34.5 dBm. DC power supply is typically 4.5V and PAE is above 15%

The CGY2130UH is manufactured using the D01PH GaAs PHEMT power process from OMMIC. This process has a 130nm gate length with a Ft of 110GHz and a Fmax of 180GHz.

The D01PH process used to manufacture the MMIC has been evaluated by ESA and is in the EPPL (European Preferred Part List). This very reliable process is suitable to manufacture power amplifiers dedicated to flight models in aerospace applications as well as high performance power amplifiers for terrestrial applications.

APPLICATIONS

- High performance GaAs Power Amplifier
- Earth-to-space or point-to-point radiolinks
- Backhaul networks
- Telecommunications
- RF Driver for High Power Amplifiers

FEATURES

- Usable frequency range from 37 to 41 GHz
- Psat > 500mW (27dBm)
- P1dB ~ + 26dBm
- Gain ~ + 22dB
- 50 Ohm input and output matched
- Delivered as 100 % on-wafer RF tested dies
- Samples and Evaluation Boards available
- Die size is 3.07 x 1.86 mm

The MMIC is available in the die form, OMMIC can deliver packaged version of the component.

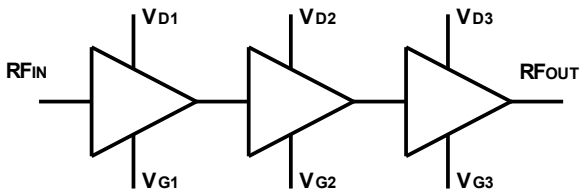

Figure 1: CGY2130 Power Amplifier block diagram

RoHS Compliant

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MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside, backside grounded; unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1}, V_{G2}, V_{G3}	Gate voltage		- 2.5	0	V
V_{D1}, V_{D2}, V_{D3}	Drain voltage		0	+ 6	V
I_{D1}	Drain current			200	mA
I_{D2}				350	
I_{D3}				500	
I_{G1}, I_{G2}, I_{G3}	Gate current		- 1	+ 1	mA
P_{IN}	Input power			+ 10	dBm
T_{amb}	Ambient temperature		- 40	+ 85	° C
T_j	Junction temperature			+ 175	° C
T_{stg}	Storage temperature		- 55	+ 85	° C

Operation of this device outside the parameter ranges given above may cause permanent damage.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j-a)}$	Thermal resistance from junction to ambient (DC at T_{amb} max)	TBD	° C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RF_{in}	Input frequency		37		41	GHz
Performances on Reference Board at f in = 39 GHz						
$V_{D1,2,3}$	Supply voltage			4.5		V
I_{DD}	Total Supply current @Psat	$V_{G1,2,3}$ = - 0,3V		820		mA
G	Gain	$V_{G1,2,3}$ = - 0,3V		22		dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point	$V_{G1,2,3}$ = - 0,3V		26		dBm
Psat	Saturated power	$V_{G1,2,3}$ = - 0,3V		27.2		dBm
PAE	Power Added Efficiency	$V_{G1,2,3}$ = - 0,3V RF_{IN} = + 10 dBm		17		%
OIP3	Output third order intercept point	I_{D3} = 350 mA		+ 34.5		dBm
IMD3	2 Carriers 14 dB below P1dB			- 44		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT} / RF_{IN}		- 43		dB
S_{11}	Input reflection coefficient	50 Ohms		- 6		dB
S_{22}	Output reflection coefficient	50 Ohms		- 12		dB
P_{OFF}	Leakage when HPA off	RF_{IN} = + 10 dBm $V_{G1,G2,G3}$ = - 2.5V		-32		dBm

(*) Measurement reference planes are the INPUT and OUTPUT coaxial connectors.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

On-Wafer measurements is the standard way of performing device testing but have inherently poor thermal conditions. Tests are performed under full biasing conditions and CW operation which combined with poor thermal conditions give a lower gain and P1dB compared to the MMIC's real performances with a good thermal heatsink.

S-PARAMETERS (SMITH CHARTS)

Conditions : V_{D1} = V_{D2} = V_{D3} = 4.5 V, V_{G1} = V_{G2} = V_{G3} = -0.3V, (I_{DQ1} = 100 mA, I_{DQ2} = 220 mA, I_{DQ3} = 310 mA), T_{amb} = + 25 °C (On-Wafer measurements)

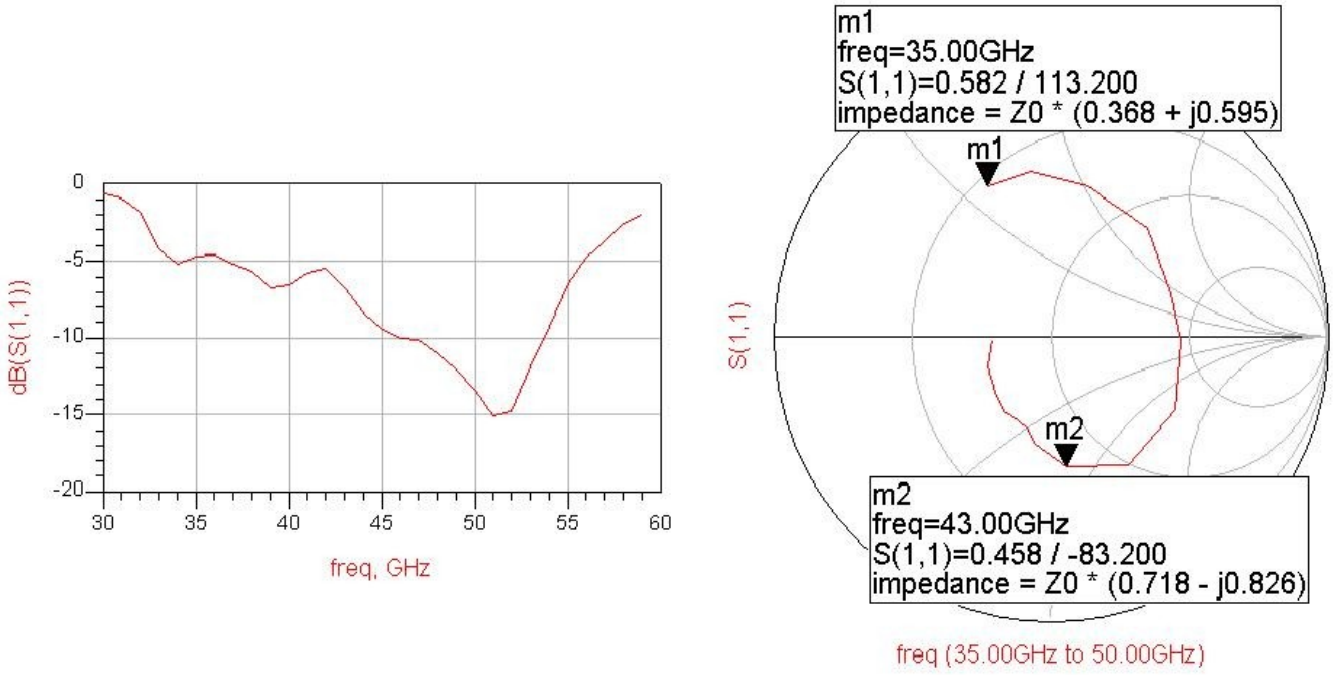


Figure 2: S11 parameter

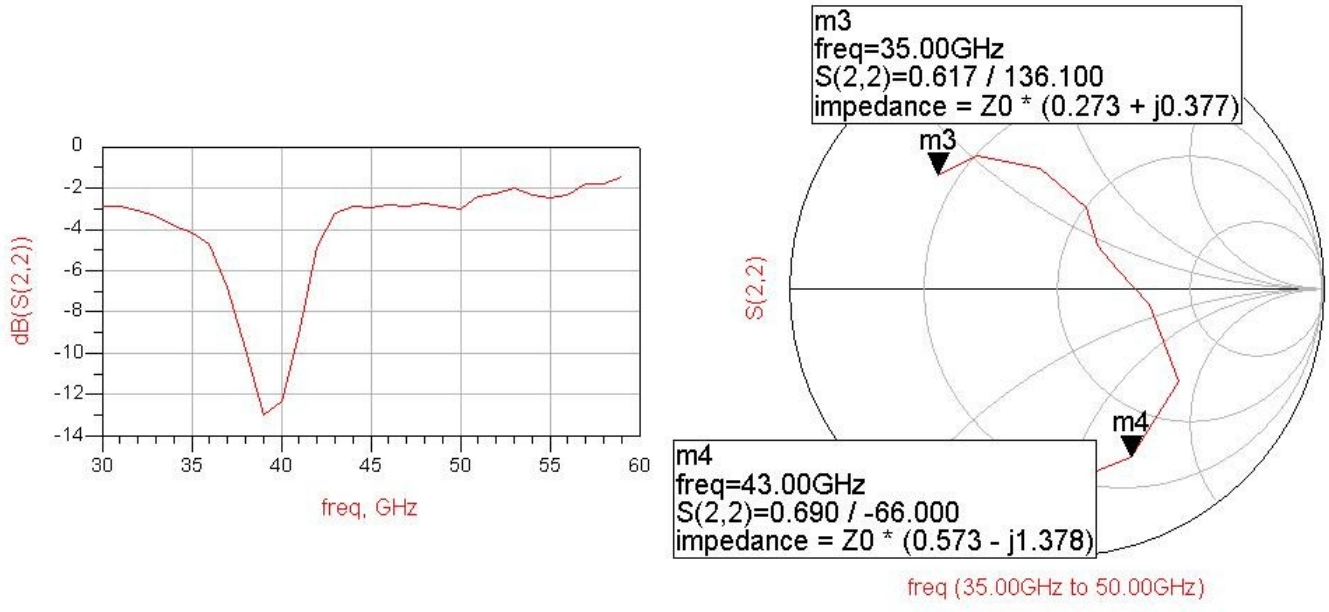


Figure 3: S22 parameter

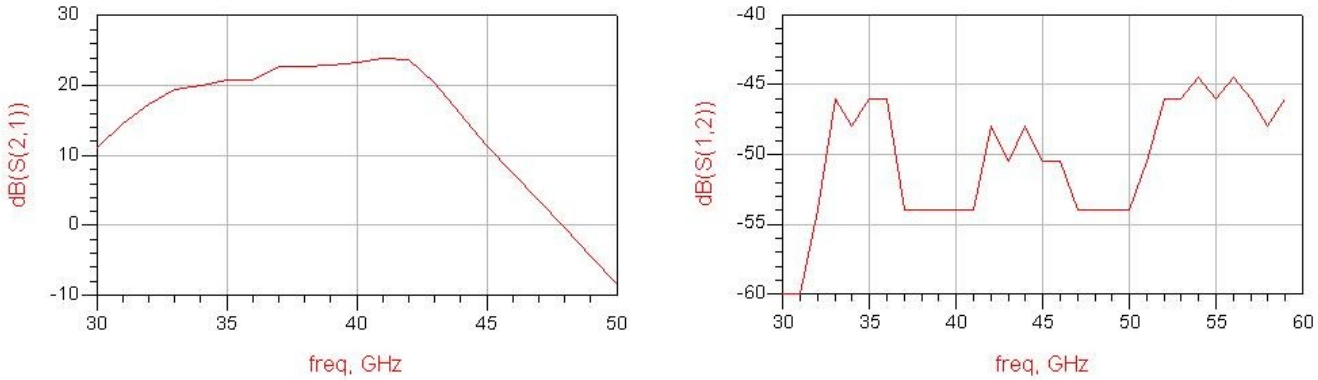


Figure 4: S21 and S12 parameters

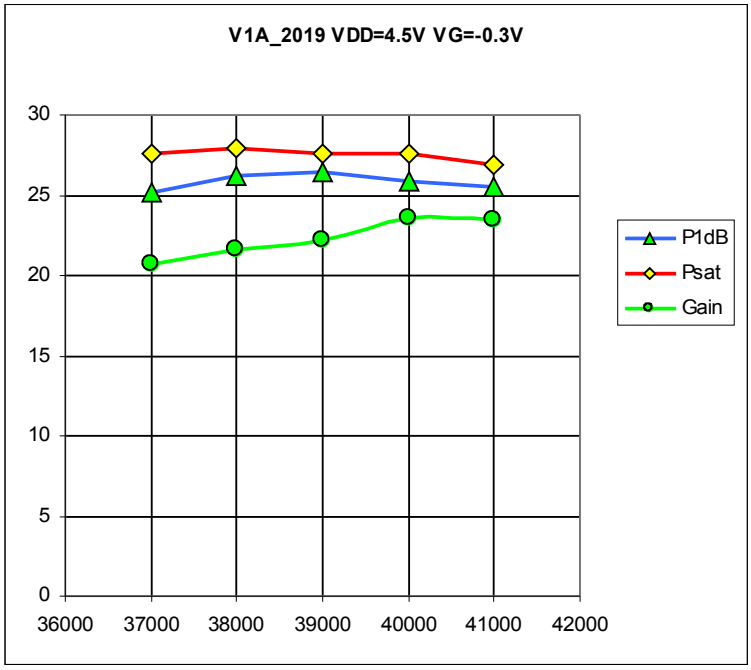
S-PARAMETERS (TABLE)

Conditions : $V_{D1} = V_{D2} = V_{D3} = 4.5$ V, $V_{G1} = V_{G2} = V_{G3} = -0.3$V, ($I_{DQ1}$ = 100 mA, I_{DQ2} = 220 mA, I_{DQ3} = 310 mA), T_{amb} = + 25 °C (On-Wafer measurements)

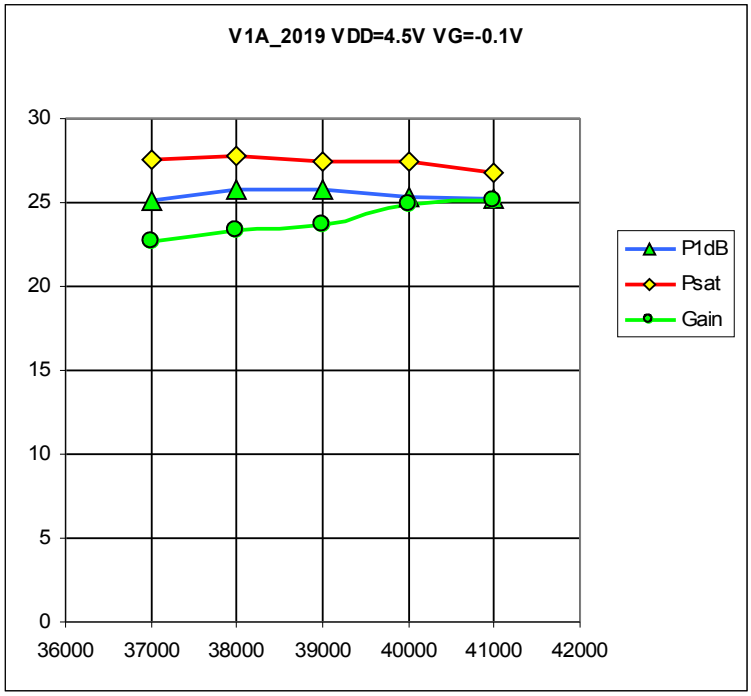
GHz	|S11|	S11 Phase	|S21|	S21 Phase	|S12|	S12 Phase	|S22|	S22 Phase
30.0	0.933	152.4	3.622	14.8	0.001	41.7	0.717	171.8
31.0	0.896	142.8	5.352	-17.5	0.001	94.3	0.717	167.6
32.0	0.809	129.3	7.320	-57.1	0.002	98.2	0.702	161.1
33.0	0.617	121.4	9.386	-101.4	0.005	84.8	0.678	154.9
34.0	0.550	119.8	9.920	-140.7	0.004	51.7	0.646	146.1
35.0	0.582	113.2	11.041	174.5	0.005	4.9	0.617	136.1
36.0	0.590	97.1	11.041	137.4	0.005	-13.7	0.581	120.9
37.0	0.548	75.7	13.788	93.9	0.002	-7.4	0.456	97.7
38.0	0.521	47.9	13.740	47.6	0.002	-71.7	0.323	70.4
39.0	0.461	19.6	13.916	5.4	0.002	-14.5	0.224	46.2
40.0	0.469	-1.9	14.605	-38.0	0.002	-60.9	0.243	17.0
41.0	0.516	-29.6	15.668	-89.0	0.002	80.6	0.350	-8.9
42.0	0.529	-57.7	15.293	-146.0	0.004	36.4	0.573	-37.1
43.0	0.458	-83.2	10.375	146.7	0.003	-15.7	0.690	-66.0
44.0	0.382	-98.6	6.339	99.8	0.004	-43.1	0.719	-85.4
45.0	0.335	-104.2	3.707	54.0	0.003	-57.1	0.711	-96.8
46.0	0.316	-112.1	2.354	20.8	0.003	-95.5	0.726	-105.1
47.0	0.312	-122.8	1.486	-16.1	0.002	-146.3	0.718	-111.1
48.0	0.282	-136.6	0.952	-40.8	0.002	143.1	0.728	-116.2
49.0	0.250	-155.8	0.584	-70.6	0.002	97.0	0.720	-119.3
50.0	0.214	-177	0.377	-97.2	0.002	90.7	0.709	-124.4
51.0	0.176	150.5	0.289	-125.9	0.003	76.3	0.756	-121.3
52.0	0.183	103.9	0.167	-124.4	0.005	57.1	0.773	-125.6
53.0	0.255	65.1	0.217	178.8	0.005	25.4	0.792	-129.7
54.0	0.343	37.7	0.145	151.8	0.006	32.2	0.766	-133.6
55.0	0.473	18.4	0.056	58.6	0.005	26.6	0.753	-133.7
56.0	0.574	0.6	0.031	-21.7	0.006	-11.2	0.763	-135.8
57.0	0.651	-14.9	0.031	100.3	0.005	-30.9	0.816	-138.4
58.0	0.742	-25.7	0.074	-31.6	0.004	-41.0	0.814	-141.1
59.0	0.795	-35	0.028	-126.3	0.005	-16.4	0.843	-145.3

1DB COMPRESSION POINT, SATURATED POWER AND GAIN

Conditions : V_{D1} = V_{D2} = V_{D3} = 4.5 V, V_{G1} = V_{G2} = V_{G3} = -0.3V, (I_{DQ1} = 100 mA, I_{DQ2} = 220 mA, I_{DQ3} = 310 mA), T_{amb} = + 25 °C (On-Wafer measurements)



Conditions : V_{D1} = V_{D2} = V_{D3} = 4.5 V, V_{G1} = V_{G2} = V_{G3} = -0.1V, (I_{DQ1} = 150 mA, I_{DQ2} = 300 mA, I_{DQ3} = 420 mA), T_{amb} = + 25 °C (On-Wafer measurements)



APPLICATION SCHEMATIC

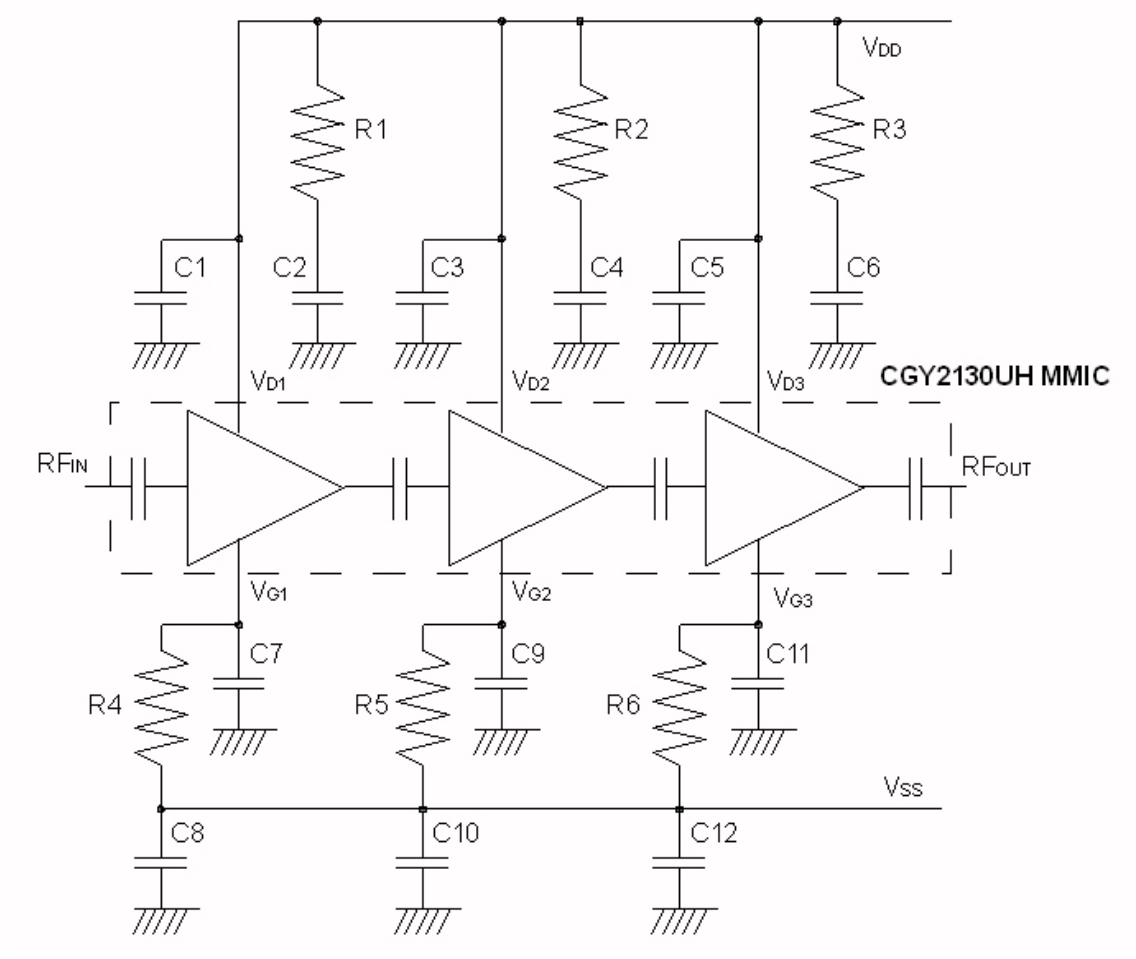


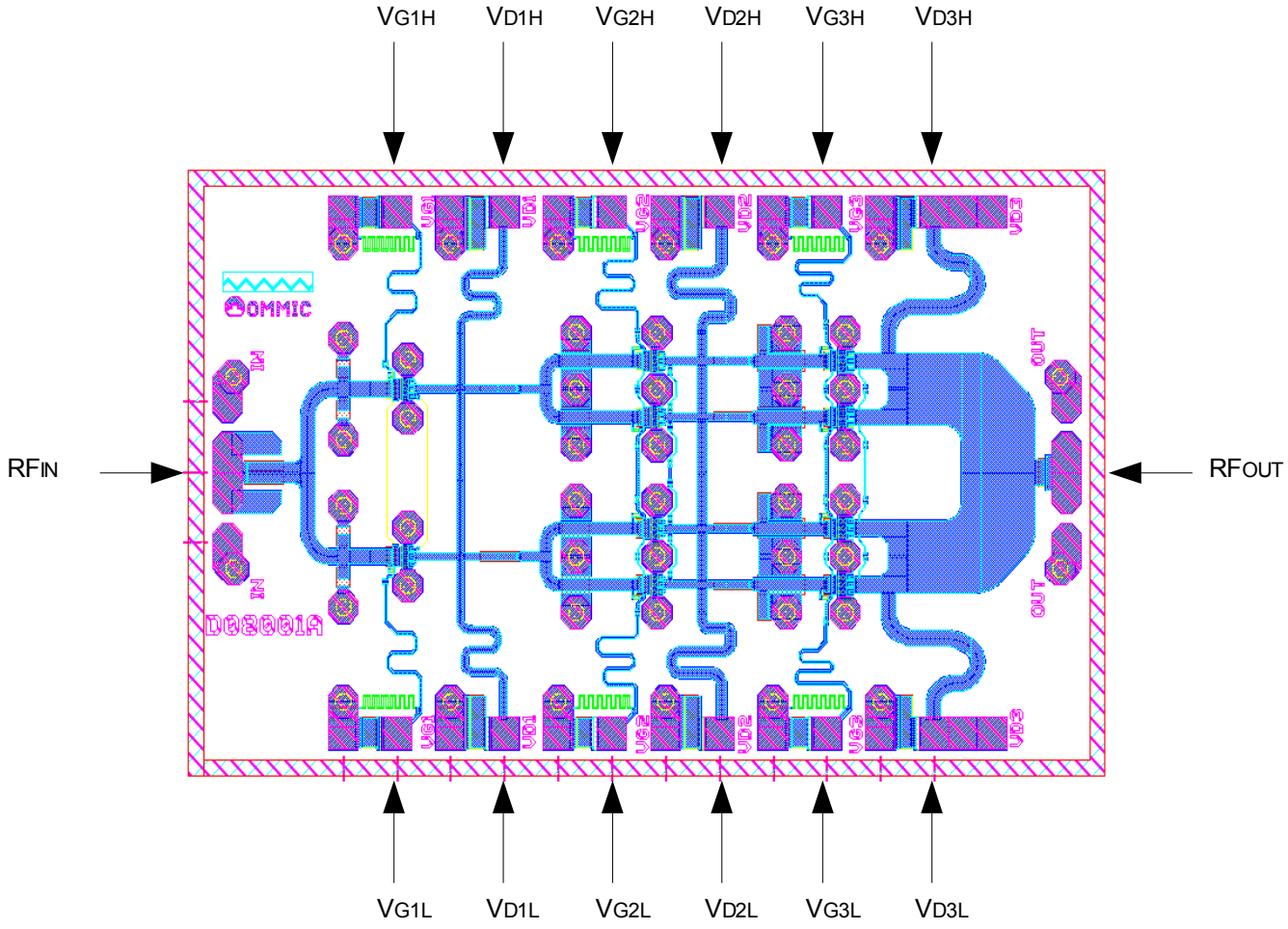
Figure 6 : APPLICATION SCHEMATICS

Component NAME	Value	Type	Comment
C1 to C6 C13 to C18	47p	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die, bonding as short as possible
R2,R4,R6 R8,R10,R12	39	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-0739RL
R1,R3,R5 R7,R9,R11	100	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-07100RL
C7 to C12 C19 to C24	100n	SMD 0603 Capacitor	MURATA GRM188R71H104KA93D

In order to save DC power consumption and improve PAE each gate can be individually driven at a different bias voltage. In this case, when using the targeted RF signal (modulated carrier), the distortion is monitored while adjusting V_{G1}, V_{G2} and V_{G3}. The global strategy is to introduce all the distortion allowed by the targeted standard in the last stage of the amplifier by adjusting V_{G3} while V_{G2} and V_{G1} are positioned in such a way that the I_{D2}, I_{D1} are kept at the minimum value corresponding to a neglectable contribution to the global distortion.

In order to validate each stage of the amplifier, with respect to the DC, it is recommended to set V_{GN} to -1.5V, then to set V_{DN} to +1V checking that the current is not too high, after that, V_{DN} can be set to +4.5V. When V_{GN} is changed from -1.5 to -0.3V, the drain current I_{DN} increases slowly in a controlled manner to reach the typical targeted value.

DIE LAYOUT AND PIN CONFIGURATION



It is highly recommended to place 47pF RF decoupling chip capacitors C1, C3, C5, C7, C9, C11 at each DC terminal with as short as possible bonding wires. Additionnaly for power up, prior to applying the drain voltage, gates voltages should be set to -1.5 volt. On shut down, reverse order operation should be performed.

The gate voltage of each stage, starting from the output stage should be adjusted to obtain the desired drain quiescent current.

PINOUT

Symbol	Pad	Description
RF_{OUT}	OUT	RF output
RF_{IN}	IN	RF input
V_{D1H}	VD1	First stage Drain (Higher Line-up)
V_{D2H}	VD2	Second stage Drain (Higher Line-up)
V_{D3H}	VD3	Third stage Drain (Higher Line-up)
V_{G1H}	VG1	First stage Gate (Higher Line-up)
V_{G2H}	VG2	Second stage Gate (Higher Line-up)
V_{G3H}	VG3	Third stage Gate (Higher Line-up)
V_{D1L}	VD1 (internally connected to V_{D1H})	First stage Drain (Lower Line-up)
V_{D2L}	VD2 (internally connected to V_{D2H})	Second stage Drain (Lower Line-up)
V_{D3L}	VD3 (internally connected to V_{D3H})	Third stage Drain (Lower Line-up)
V_{G1L}	VG1 (internally connected to V_{G1H})	First stage Gate (Lower Line-up)
V_{G2L}	VG2 (internally connected to V_{G2H})	Second stage Gate (Lower Line-up)
V_{G3L}	VG3 (internally connected to V_{G3H})	Third stage Gate (Lower Line-up)
GND	BACKSIDE	Ground

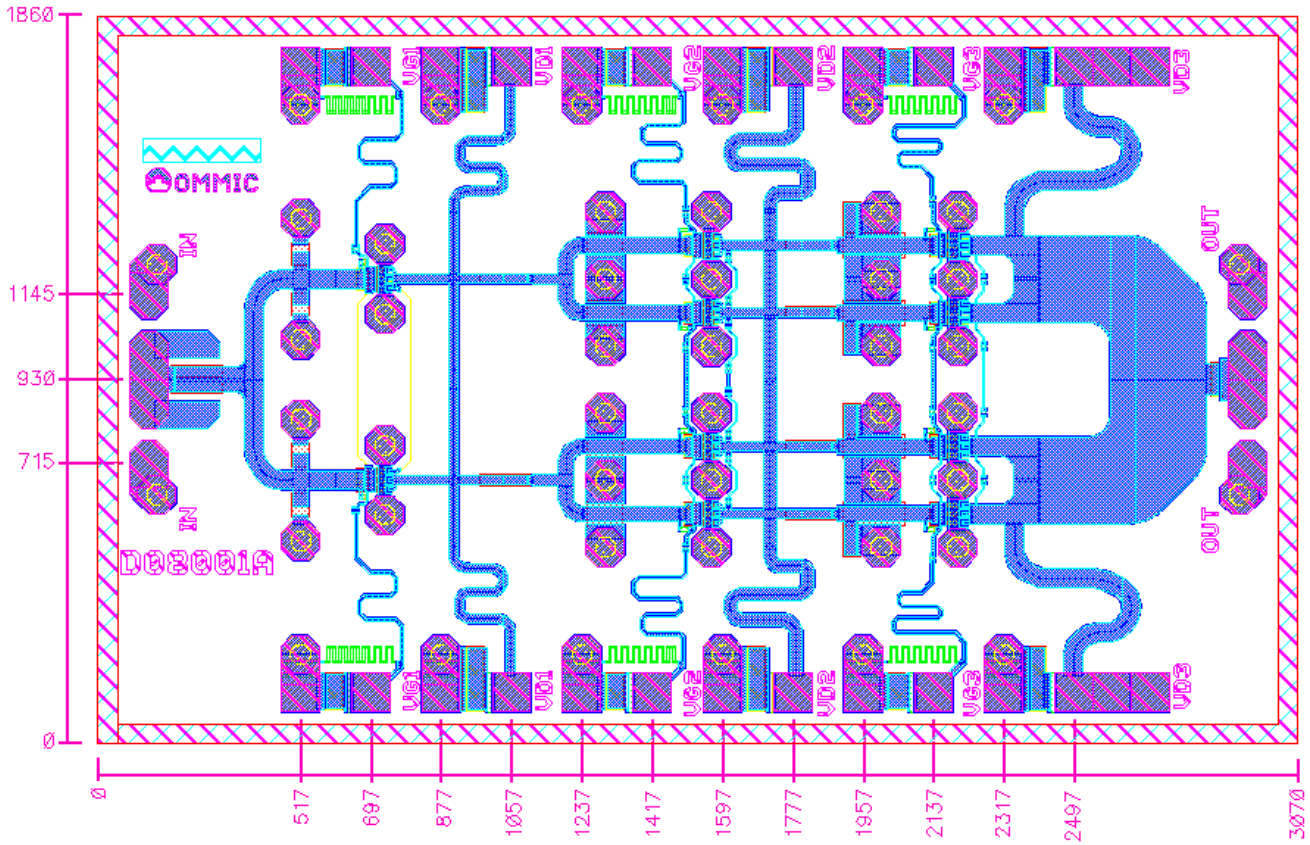
Note :

It is key in order to ensure good performance and stability that the backside of the die is suitably connected to the ground.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Die size (mm)
DIE	100% RF and DC on wafer tested	14	-	3.07 x 1.86 x 0.1

BONDING PAD COORDINATES



SOLDERING

During soldering process, to avoid permanent damages or to impact on the reliability, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400°C

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2130	UH	C1		On-Wafer measured Die

RoHS Compliant

Document History :
Version 1.0, Last Update 26/07/2010
Version 1.1, Demo Board update 14/09/2011

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