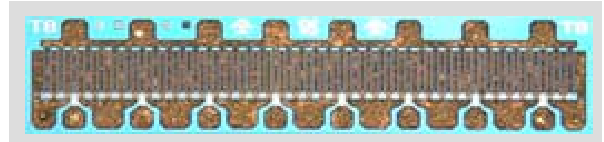
5W High Linearity and High Efficiency GaAs Power FETs

FEATURES

- 5W Typical Power at 6 GHz
- Linear Power Gain: G_L = 10 dB Typical at 6 GHz
- High Linearity: IP3 = 47 dBm Typical at 6 GHz
- Via Holes Source Ground
- Suitable for High Reliability Application
- Breakdown Voltage: $BV_{DGO} \geq 18$ V
- Lg = 0.6 µm, Wg = 12 mm
- High Power Added Efficiency: Nominal PAE of 40 % at 6 GHz
- Tight Vp ranges control
- High RF input power handling capability
- 100 % DC Tested

PHOTO ENLARGEMENT



DESCRIPTION

The TC1806 is a GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) which has high linearity and high Power Added Efficiency. The device is processed with a propriety via-hole process, which provides low thermal resistance and low inductance. The long gate length makes the device to have high breakdown voltage. All devices are 100% DC tested to assure consistent quality. Bond pads are gold plated for either thermo-compression or thermo-sonic wire bonding. Backside gold plating is compatible with standard AuSn die-attach. Typical application include commercial and military high performance power amplifiers.

ELECTRICAL SPECIFICATIONS (T_A=25 °C)

Symbol	Conditions	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point, f = 6 GHz V_{DS} = 8 V, I_{DS} = 1200 mA	36	36.5		dBm
G_L	Linear Power Gain, f = 6 GHz V_{DS} = 8 V, I_{DS} = 1200 mA	9	10		dB
IP3	Intercept Point of the 3rd-order Intermodulation, f = 6 GHz V_{DS} =8V, I_{DS} =1200mA,*P_{SCL}= 23dBm		47		dBm
PAE	Power Added Efficiency at 1dB Compression Power, f = 6 GHz		40		%
I_{DSS}	Saturated Drain-Source Current at V_{DS} = 2 V, V_{GS} = 0 V		3		A
g_m	Transconductance at V_{DS} = 2 V, V_{GS} = 0 V		2000		mS
V_P	Pinch-off Voltage at V_{DS} = 2 V, I_D = 24 mA		-1.7**		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at I_{DGO} = 6 mA	18	22		Volts
R_{th}	Thermal Resistance		2		°C/W

Note:

*** P_{SCL}: Output Power of Single Carrier Level.**

* *For the tight control of the pinch-off voltage . TC1806's are divided into 3 groups:
(1)**TC1806P1519** : Vp = -1.5V to -1.9V (2) **TC1806P1620** : Vp = -1.6V to -2.0V
(3)**TC1806P1721** : Vp = -1.7V to -2.1V In addition, the customers may specify their requirements.

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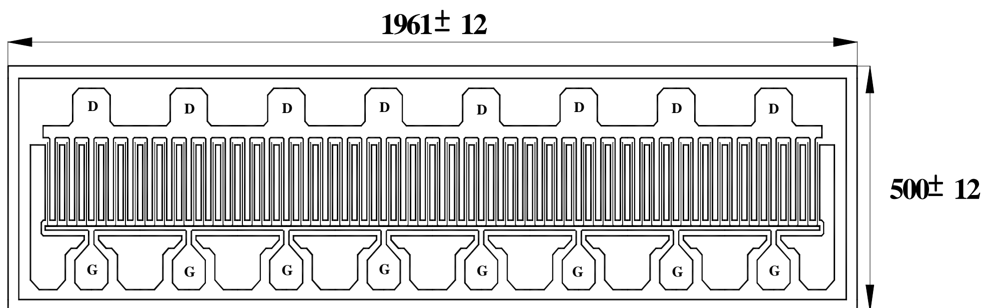
ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Symbol	Parameter	Rating
V_{DS}	Drain-Source Voltage	12 V
V_{GS}	Gate-Source Voltage	-5 V
I_{DS}	Drain Current	I_{DSS}
P_{in}	RF Input Power, CW	33 dBm
P_T	Continuous Dissipation	12 W
T_{CH}	Channel Temperature	175 °C
T_{STG}	Storage Temperature	- 65 °C to +175 °C

CHIP DIMENSIONS



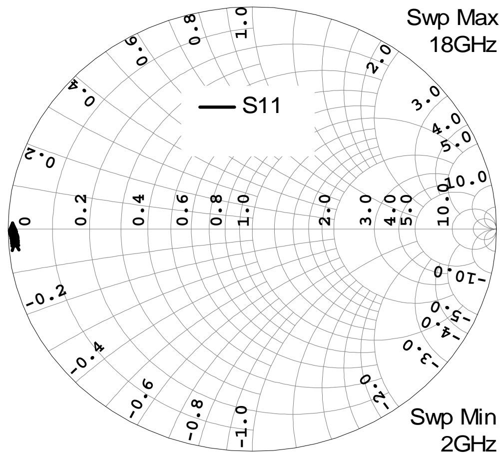
Units: Micrometers

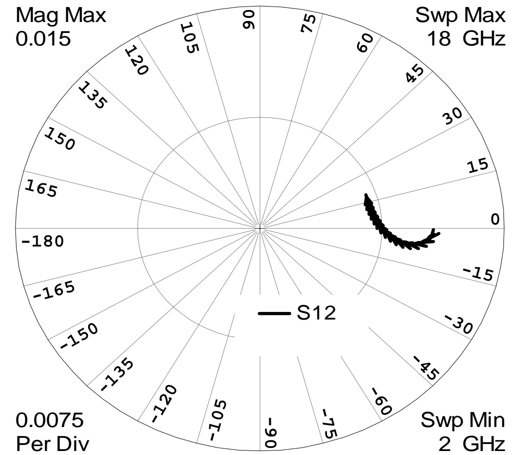
Chip Thickness: 50

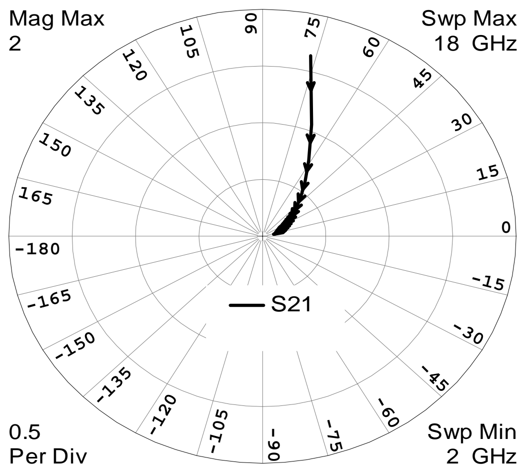
Gate Pad: 76.0 x 59.5

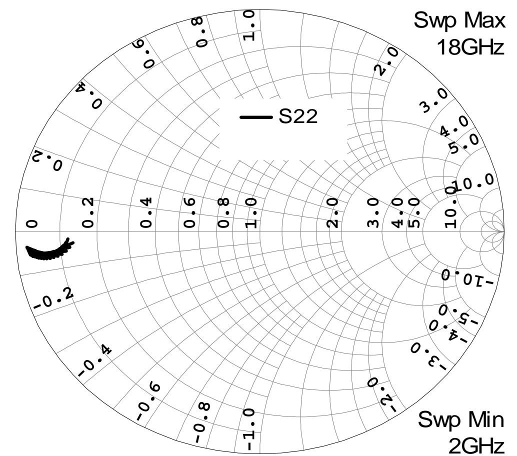
Drain Pad: 86.0 x 76.0

TYPICAL SCATTERING PARAMETERS (T$_A$=25 °C) V_{DS} = 8 V, I_{DS} = 1200 mA







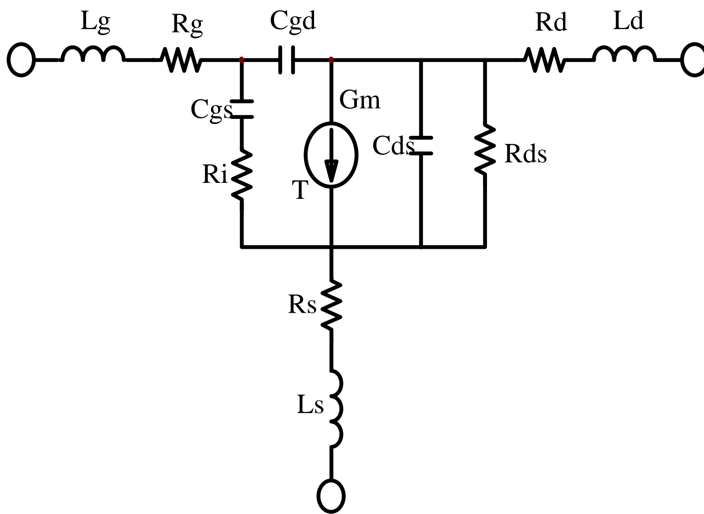


FREQUENCY	S11		S21		S12		S22	
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2	0.9738	-175.53	1.6351	76.59	0.0107	-2.09	0.7913	-175.80
3	0.9746	-177.12	1.0563	68.50	0.0104	-4.49	0.8063	-174.74
4	0.9754	-177.96	0.7606	61.30	0.0100	-5.99	0.8237	-173.94
5	0.9764	-178.52	0.5805	54.82	0.0095	-6.75	0.8416	-173.45
6	0.9773	-178.94	0.4597	49.01	0.0091	-6.82	0.8588	-173.23
7	0.9781	-179.27	0.3739	43.79	0.0087	-6.29	0.8745	-173.19
8	0.9789	-179.57	0.3103	39.12	0.0083	-5.21	0.8885	-173.29
9	0.9796	-179.83	0.2619	34.92	0.0080	-3.67	0.9006	-173.47
10	0.9802	179.94	0.2242	31.16	0.0077	-1.75	0.9111	-173.71
11	0.9807	179.71	0.1942	27.76	0.0074	0.49	0.9201	-173.97
12	0.9811	179.50	0.1701	24.68	0.0072	2.95	0.9278	-174.25
13	0.9815	179.30	0.1504	21.89	0.0071	5.58	0.9345	-174.53
14	0.9818	179.11	0.1341	19.35	0.0070	8.31	0.9401	-174.80
15	0.9821	178.93	0.1205	17.02	0.0069	11.09	0.9451	-175.06
16	0.9823	178.75	0.1091	14.89	0.0069	13.87	0.9493	-175.32
17	0.9826	178.57	0.0993	12.92	0.0069	16.62	0.9530	-175.56
18	0.9827	178.40	0.0909	11.11	0.0069	19.31	0.9562	-175.79

* The data does not include gate and drain bond wires.

SMALL SIGNAL MODEL, V_{DS} = 8 V, I_{DS} = 1200 mA

SCHEMATI



PARAMETERS

Lg	0.008 nH	Rs	0.106 Ohm
Rg	0.093 Ohm	Ls	0.001 nH
Cgs	22.9 pF	Cds	2.977 pF
Ri	0.185 Ohm	Rds	11.9 Ohm
Cgd	0.803 pF	Rd	0.14 Ohm
Gm	2335 mS	Ld	0.0014 nH
T	3.9 psec		

CHIP HANDLING

DIE ATTACHMENT: Conductive epoxy or eutectic die attach is recommended. Eutectic die attach can be accomplished with Au-Sn (80%Au-20%Sn) perform at stage temperature: 290°C ± 5°C; Handling Tool: Tweezers; Time: less than 1min.

WIRE BONDING: The recommended wire bond method is thermocompression bonding with 0.7 to 1.0 mil (0.018 to 0.025 mm) gold wire. Stage temperature: 220°C to 250°C; Bond Tip Temperature: 150°C; Bond Force: 20 to 30 gms depending on size of wire and Bond Tip Temperature.

HANDLING PRECAUTIONS: The user must operate in a clean, dry environment. Care should be exercised during handling avoid damage to the devices. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.

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