ARM®-based 32-bit Cortex®-M4 MCU with 32 to 64 KB Flash, sLib, 1 CAN, 1 OTGFS, 13 timers, 1 ADC, 12 communication interfaces

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 96 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - DSP instructions
- **Memories**
  - 32 to 64 Kbytes of internal Flash memory
  - 4 Kbytes of boot code area used as a Bootloader or as a general instruction/data memory (one-time-configured)
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 20 Kbytes of SRAM
- **Power control (PWC)**
  - 2.4 to 3.6 V supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes, 6 WKUP pins can wake up Standby mode
  - 5 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK), accuracy 1 % at T_A = 25 °C and 2.5 % at T_A = -40 to +105 °C, with automatic clock calibration (ACC)
  - PLL flexible multiplication and division factor
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1 x 12-bit 2 MSPS A/D converter, up to 16 input channels, hardware over-sampling up to equivalent 16-bit resolution
  - Internal reference voltage (V_{INTRV})
- **DMA**
  - 1 x DMA controller for flexible mapping support
  - Total 7 channels
- **Up to 55 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 13 timers (TMR)**
  - 1 x 16-bit 7-channel advanced timer, 6-channel PWM output with dead-time generator and emergency stop
  - Up to 6 x 16-bit and 1 x 32-bit general-purpose timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Advanced and general-purpose timers provide up to 24-channel PWM
  - 2 x 16-bit basic timers
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarms, subsecond accuracy, and hardware calendar; supports calibration**
- **Up to 12 communication interfaces**
  - 2 x I^2C interfaces for SMBus/PMBus support
  - 4 x USARTs, support master synchronous SPI and modem control, with ISO7816 interface, LIN, IrDA and RS485 driver enable; support TX/RX swap
  - 3 x SPIs (36 Mbit/s), all with I^2S interface multiplexed, any combination of two interfaces supports full-duplex
  - CAN interface (2.0B Active), with 256 bytes of dedicated SRAM
  - OTG full speed interface, with 1280 bytes of dedicated SRAM, supporting crystal-less when device mode
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug modes**
  - Serial wire debug (SWD) and serial wire output (SWO)
- **Operating temperatures: -40 to +105 °C**

- **Packages**
  - LQFP64 10 x 10 mm
  - LQFP64 7 x 7 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - LQFP32 7 x 7 mm
  - QFN32 4 x 4 mm
  - TSSOP20 6.5 x 4.4 mm

Table 1. AT32F425 device summary

Flash	Part numbers
64 KBytes	AT32F425R8T7, AT32F425R8T7 -7, AT32F425C8T7, AT32F425C8U7, AT32F425K8T7, AT32F425K8U7-4, AT32F425F8P7
32 KBytes	AT32F425R6T7, AT32F425R6T7 -7, AT32F425C6T7, AT32F425C6U7, AT32F425K6T7, AT32F425K6U7-4, AT32F425F6P7

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1 Descriptions

The AT32F425 is based on the high-performance ARM® Cortex®-M4 32-bit RISC core running up to 96 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F425 incorporates high-speed embedded memories (up to 64 KBytes of internal Flash memory and 20 KBytes of SRAM), enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only.

The AT32F425 offers one 12-bit ADC, six general-purpose 16-bit timers, one 32-bit general-purpose timer, two basic timers, and one advanced timer. It supports standard and advanced communication interfaces: up to two I^2Cs, three SPIs (all multiplexed as I^2Ss), four USARTs, one infrared transmitter, one OTGFS interface and one CAN.

The AT32F425 operates in the -40 to +105 °C temperature range, with a power supply from 2.4 to 3.6 V. A comprehensive set of power-saving modes meet the requirements of low-power applications.

The AT32F425 offers devices in various packages. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included.

Table 2. AT32F425 features and peripheral counts

Part Number		AT32F425xxP7		AT32F425xxU7-4		AT32F425xxT7		AT32F425xxU7		AT32F425xxT7		AT32F425xxT7-7		AT32F425xxT7	
		F6	F8	K6	K8	K6	K8	C6	C8	C6	C8	R6	R8	R6	R8
Frequency (MHz)		96													
Int.Flash (KBytes)		32	64	32	64	32	64	32	64	32	64	32	64	32	64
SRAM (KBytes)		20	20	20	20	20	20	20	20	20	20	20	20	20	20
Timers	Advanced	1		1		1		1		1		1		1	
	32-bit general-purpose	1		1		1		1		1		1		1	
	16-bit general-purpose	6		6		6		6		6		6		6	
	Basic	2		2		2		2		2		2		2	
	SysTick	1		1		1		1		1		1		1	
	WDT	1		1		1		1		1		1		1	
	WWDT	1		1		1		1		1		1		1	
	ERTC	1		1		1		1		1		1		1	
Communication interfaces	I^2C	2		2		2		2		2		2		2	
	SPI/I^2S	2/2(1)		3/3		3/3		3/3		3/3		3/3		3/3	
	USART	4(2)		4(3)		4		4		4		4		4	
	CAN	1		1		1		1		1		1		1	
	OTGFS	1		1		1		1		1		1		1	
	IRTMR	1		1		1		1		1		1		1	

Part Number		AT32F425xxP7		AT32F425xxU7-4		AT32F425xxT7		AT32F425xxU7		AT32F425xxT7		AT32F425xxT7-7		AT32F425xxT7	
		F6	F8	K6	K8	K6	K8	C6	C8	C6	C8	R6	R8	R6	R8
Analog	12-bit ADC numbers/channels	1		1		1		1		1		1		1	
		9		10		10		10		10		16		16	
GPIO		15		27		25		39		39		55		55	
Operating temperatures		-40 °C 至+105 °C													
Packages		TSSOP20 6.5 x 4.4 mm		QFN32 4 x 4 mm		LQFP32 7 x 7 mm		QFN48 6 x 6 mm		LQFP48 7 x 7 mm		LQFP64 7 x 7 mm		LQFP64 10 x 10 mm	

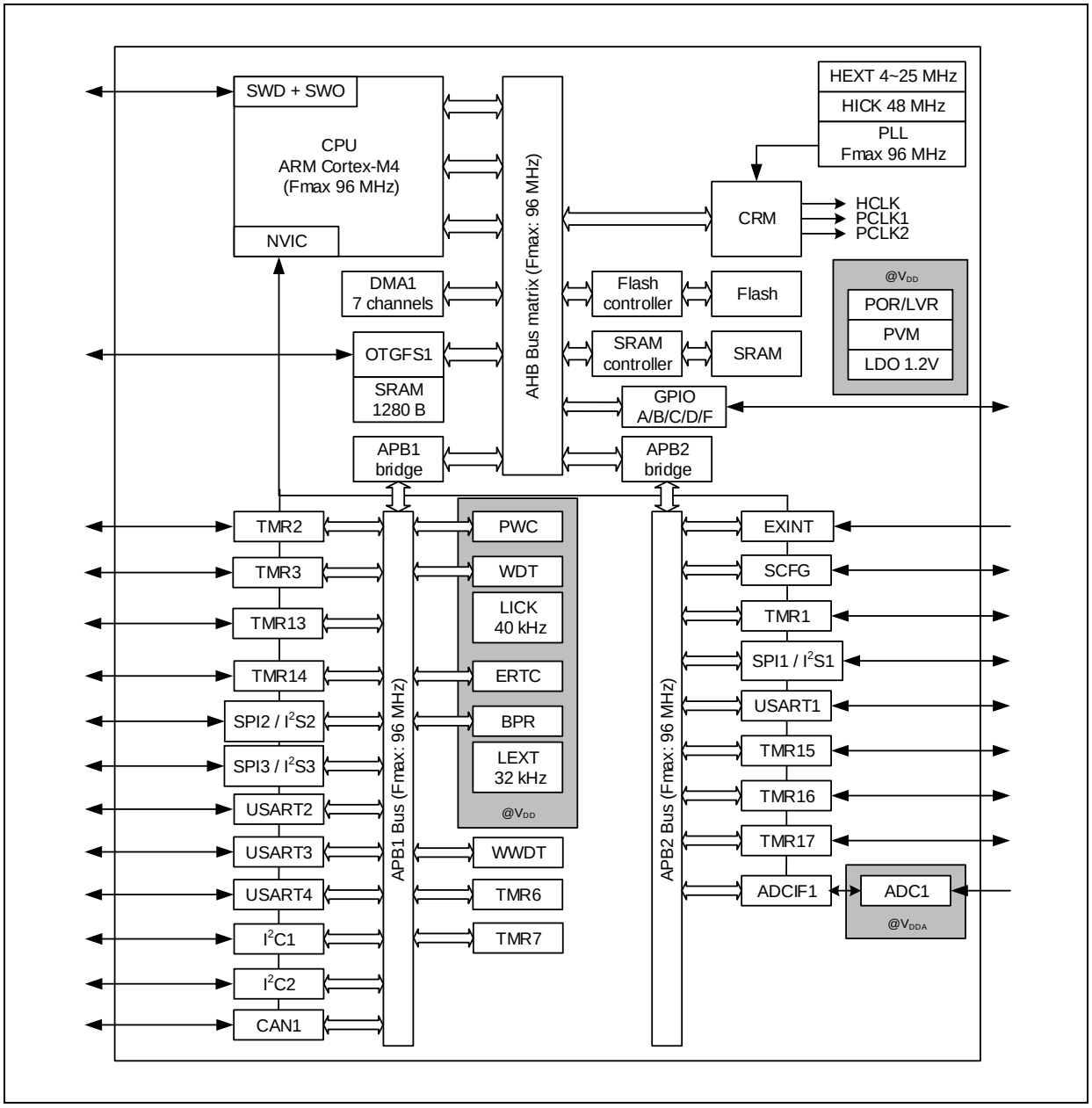
(1) For the TSSOP20 package, only SPI1/I^2S1 and SPI2/I^2S2 are available.
(2) For the TSSOP20 package, USART3 cannot provide all functional pins at the same time; USART1 and USART4 are used as UART since they can only offer TX and RX pins.
(3) For the QFN32 package, four USART pins cannot be used simultaneously despite the fact that they are present.

2 Functionality overview

2.1 ARM® Cortex®-M4

The ARM Cortex®-M4 processor is the latest generation of ARM processor for embedded systems. It is a 32-bit RISC processor that features exceptional code efficiency, outstanding computational performance and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. *Figure 1* shows the general block diagram of the AT32F425.

Figure 1. AT32F425 block diagram



2.2 Memory

2.2.1 Internal Flash memory

Up to 64 KBytes of embedded Flash is available for storing programs and data. User can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. “sLib” is a mechanism that protects the intelligence of solution vendors and facilitates the second-level development by customers. The HalfCycle bit in the FLASH_PSR register, once enabled, will help improve overall code efficiency, but the maximum AHB clock frequency is lower than when the HalfCycle bit is disabled. Thus the general operating conditions listed in *Table 11*Table 11 must be respected when in use.

There is another 4-KByte boot code area in which the bootloader is stored. If it’s not needed, this area can be used as a general instruction/data memory (one-time-configured) instead.

A User’s System Data block is included, which is used as configuration of the hardware behaviors such as read/erase/write protection and watchdog self-enable. User’s System Data allows to set erase/write and read protection individually, with the latter supporting low-level and high-level protection.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 Embedded SRAM

Up to 20 KBytes of embedded SRAM (read/write) is accessible at CPU clock speed with 0 wait states.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F425 embeds a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 21 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.4～3.6 V: used as an external power supply for GPIOs and the internal block such as ERTC, external 32 kHz oscillator (LEXT), battery powered register (BPR) and the internal regulator (LDO), etc..
- V_{DDA} = 2.4～3.6 V: used as an external analog power supply for ADC. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (PDR) circuitry. It is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode is used in Run mode and in Deepsleep mode;
- Low-power mode can be used in Deepsleep mode;
- Power down mode is used in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO operates always in its normal mode after reset.

2.4.4 Low-power modes

The AT32F425 supports three low-power modes:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep** mode

  Deepsleep mode achieves the lowest power consumption while holding the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm/wakeup/tamper/time stamp event, and the OTG wakeup.

- **Standby** mode

  The Standby mode is used to acquire the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the BPR domain and Standby circuitry. The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/time stamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User's System Data setting.

2.5 Boot modes

At startup, the BOOT0 pin and the nBOOT1 bit of User's System Data are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot code area;
- Boot from embedded SRAM.

The bootloader is stored in boot code area. It is used to reprogram the Flash memory through USART1 or USART2. *Table 3* provides the pin configurations for Bootloader.

Table 3. Pin configurations for Bootloader

Interface	Pins
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX PA3: USART2_RX

2.6 Clocks

The internal 48 MHz clock (HICK) through a divided-by-6 divider (8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system take the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB and APB domains is 96 MHz.

The AT32F425 embeds an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK clock. This assures the most precise accuracy of the HICK in the full range of the operating temperatures.

2.7 General-purpose inputs / outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiple function. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO's configuration can be locked, if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

2.8 Direct Memory Access Controller (DMA)

AT32F425 features a general-purpose 7-channel DMA controller that is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals for the purpose of flexible mapping.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI and I^2S, I^2C, USART, advanced, general-purpose, and basic timers TMRx (except TMR13/14), and ADC.

2.9 Timers (TMR)

The AT32F425 device includes an advanced timer, up to 7 general-purpose timers, 2 basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 4. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR13 TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
General-purpose	TMR15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TMR16 TMR17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.9.1 Advanced timers (TMR1)

The advanced timer (TMR1) can be seen a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMRs which have the same architecture. Thus the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

2.9.2 General-purpose timers (TMR2~3)

Up to 7 synchronizable general-purpose timers are available in the AT32F425.

- **TMR2 and TMR3**

  The TMR2 timer is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 timer is based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode outputs.

  These general-purpose timers can work with the advanced timers via the link feature for synchronization or event chaining. In debug mode, their counters can be frozen. Any of these general-purpose timers can be used for the generation of PWM output. Each timer has its individual DMA request mechanism.

  They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR13 and TMR14**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases.

- **TMR15, TMR16 and TMR17**

  These three timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The TMR15 offers two channels and one complementary channel, whereas TMR16 and TMR17 have one channel and one complementary channel for input capture/output compare, PWM, or one-cycle mode output.

  They can work together via the link feature for synchronization or event chaining.

  In debug mode, their counters can be frozen. Each timer has its individual DMA request mechanism.

2.9.3 Basic timers (TMR6 and TMR7)

These two timers are used as a generic 16-bit time base.

2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. Its features include:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabling or not configurable through the User's System Data. The counter can be frozen in debug mode.

2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- Five 32-bit battery powered registers

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic wakeup from Deepsleep or Standby mode
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output

The alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A 20-bit prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 20 bytes of user application data. Battery powered registers are not reset by a system, or when the device wakes up from the Standby mode.

2.13 Communication interfaces

2.13.1 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

There are up to three SPIs able to communicate at up to 36 Mbits/s in slave and master modes in full-duplex and half-duplex modes. The 3-bit prescaler generates eight master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master and slave modes.

Three standard I^2S interfaces (multiplexed with SPI) are available, which can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When I^2S configured in master mode, the master clock can be output to the external 256 times sampling frequency.

In addition, any two of these I²S interfaces in half-duplex mode can be combined to achieve full-duplex communication function, while the remaining interface can still be operated independently or used as a SPI.

All I²Ss can use the DMA controller.

2.13.2 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F425 embeds four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3, and USART4).

These four interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. They also offer hardware management of the CTS and RTS signals, RS485 drive enable, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller, with TX/RX swap support.

All interfaces are able to communicate at a speed of up to 6 Mbit/s.

2.13.3 Inter-integrated-circuit interface (I²C)

Two I²C bus interfaces can operate in multi-master and slave modes. They can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz). Several GPIOs provide ultra-high sink current 20 mA.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.13.4 Controller area network (CAN)

The controller area network (CAN) is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks. It also has dedicated 256 Bytes of SRAM, which is not shared with any other peripherals.

2.13.5 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32F425 embeds one OTG full-speed (12 Mb/s) device/host peripheral. The OTGFS peripheral is compliant with the USB 2.0 specification and OTG 1.3 specification. It has software-configurable endpoint setting and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock that is generated by a PLL; as a device peripheral, the HICK 48 MHz clock source can be used as the OTGFS clock directly.

OTGFS has the major features such as:

- 1280 KBytes of SRAM used exclusively by the endpoints (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (endpoint 0 included, device mode)
- 16 channels (host mode)
- SOF output
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - In Host mode: full-speed and low speed
  - In Device mode: full-speed

2.13.6 Infrared transmitter (IRTMR)

The AT32F425 device provides an infrared transmitter solution. The solution is based on the internal connection between TMR16, USART1, or USART4 and TMR17. TMR17 is used to provide the carrier frequency, and TMR16, USART1, or USART4 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR16 channel 1 and TMR17 channel 1 must be correctly configured to generate a correct waveform. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.14 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.15 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converters (ADC) is embedded into AT32F425 device. It supports conversions in single mode or sequential mode. This ADC also shares up to 16 external channels and two internal channels, with the internal channels connected to V_{SSA} and the internal reference voltage (V_{INTRV}), respectively. In sequential mode, automatic conversion is performed on a selected group of analog inputs.

The internal reference voltage (V_{INTRV}) provides a stable voltage output for the ADC. V_{INTRV} is internally connected to the ADC1_IN17 channel.

This ADC can be served by the DMA controller.

A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is above the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and advanced timers (TMR1) can be cascaded to the regular conversion and preempted conversion of ADC, respectively. ADC conversion can be synchronized with clocks through the application program.

2.16 Serial wire debugger (SWD) and serial wire output (SWO) interfaces

The ARM SWD interface is embedded in the AT32F425 device. It is a serial wire debug interface that enables a serial wire debugger to be connected to the target for programming and debugging. It also offers a SWO feature for asynchronous trace in debug mode.

3 Pin functional definitions

Figure 2. AT32F425 LQFP64 pinout

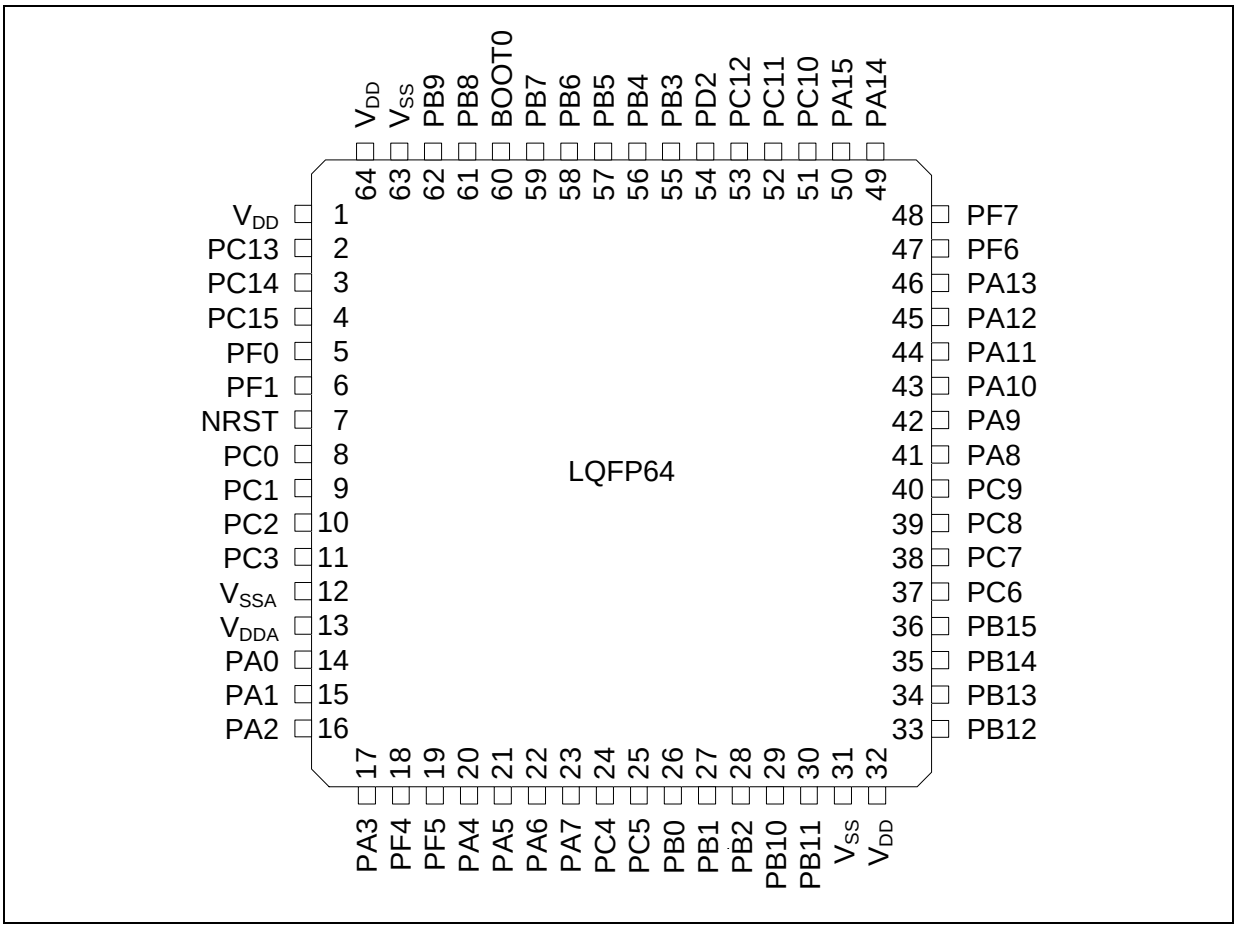


Figure 3. AT32F425 LQFP48 pinout

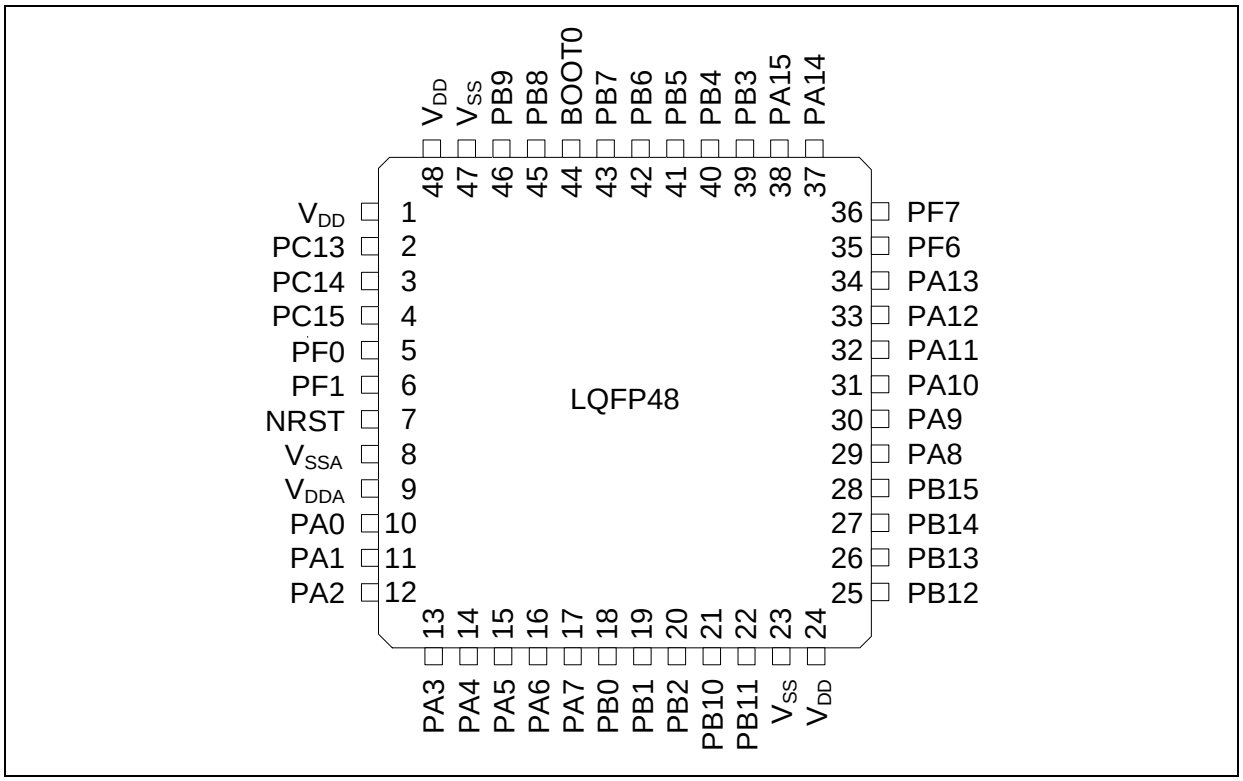


Figure 4. AT32F425 QFN48 pinout

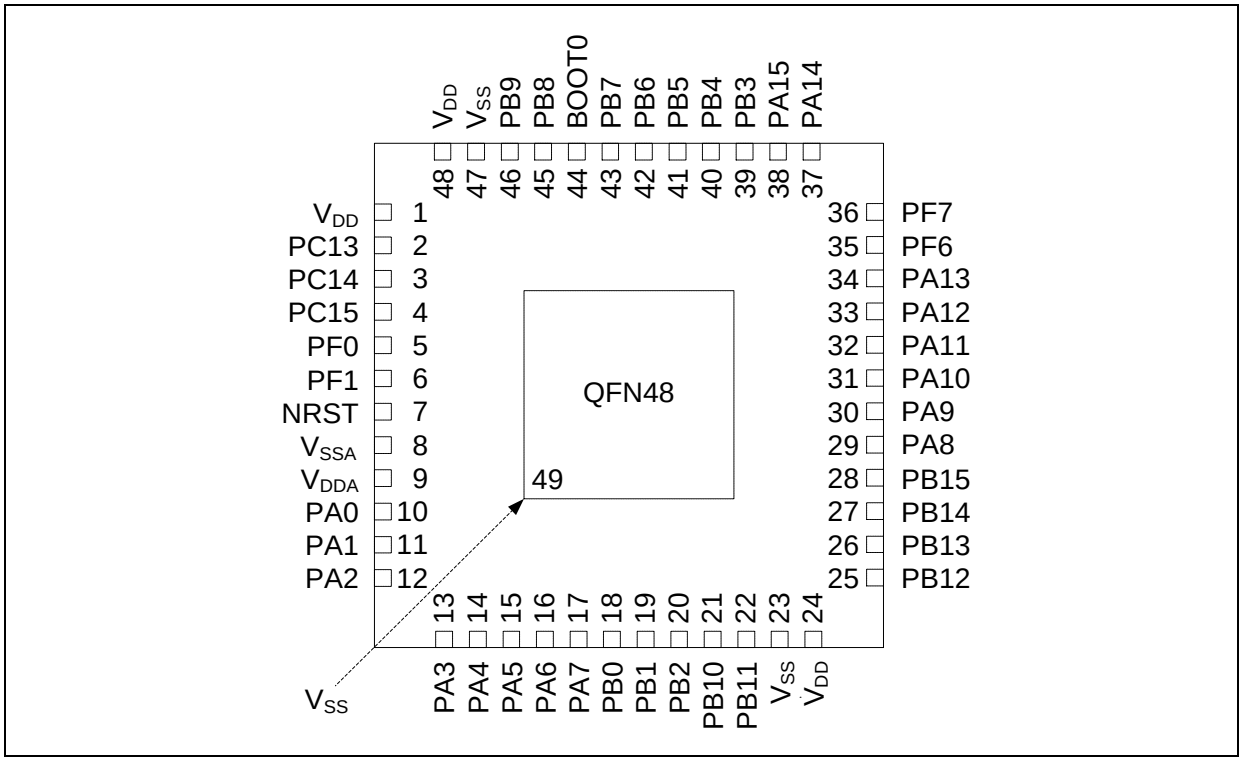


Figure 5. AT32F425 LQFP32 pinout

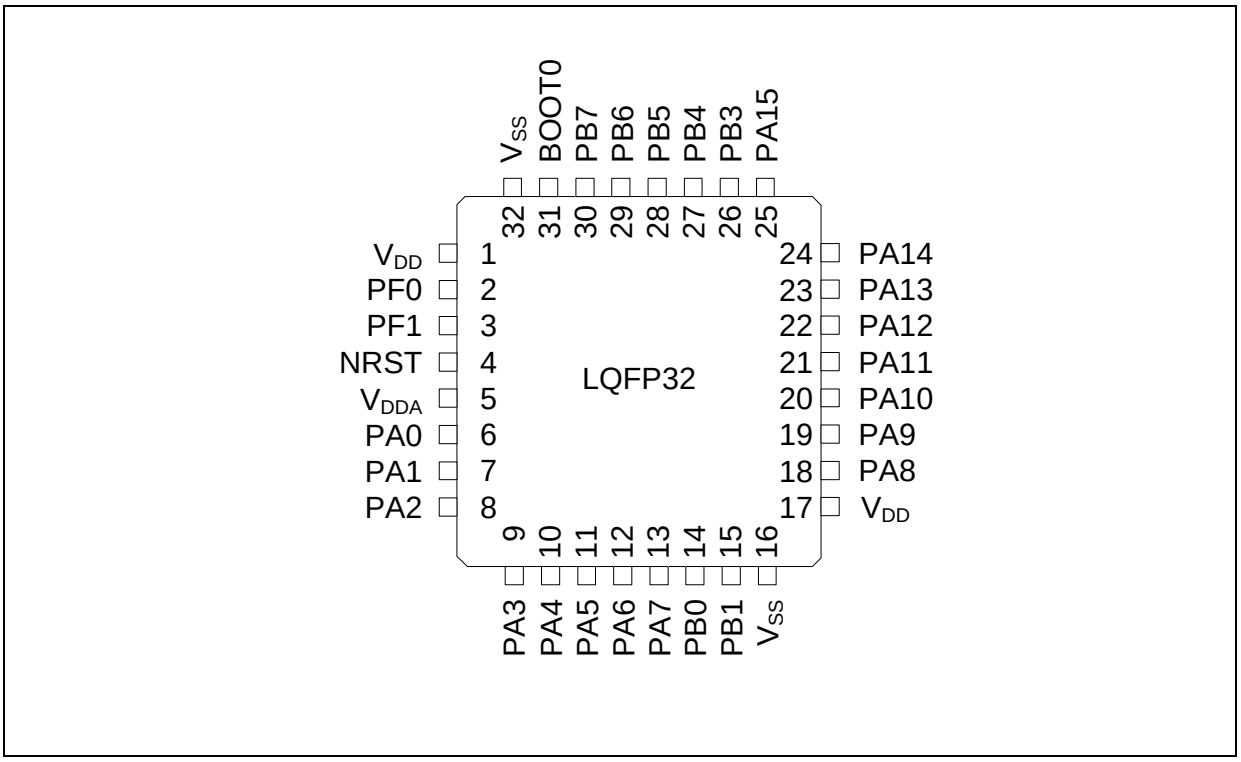


Figure 6. AT32F425 QFN32 pinout

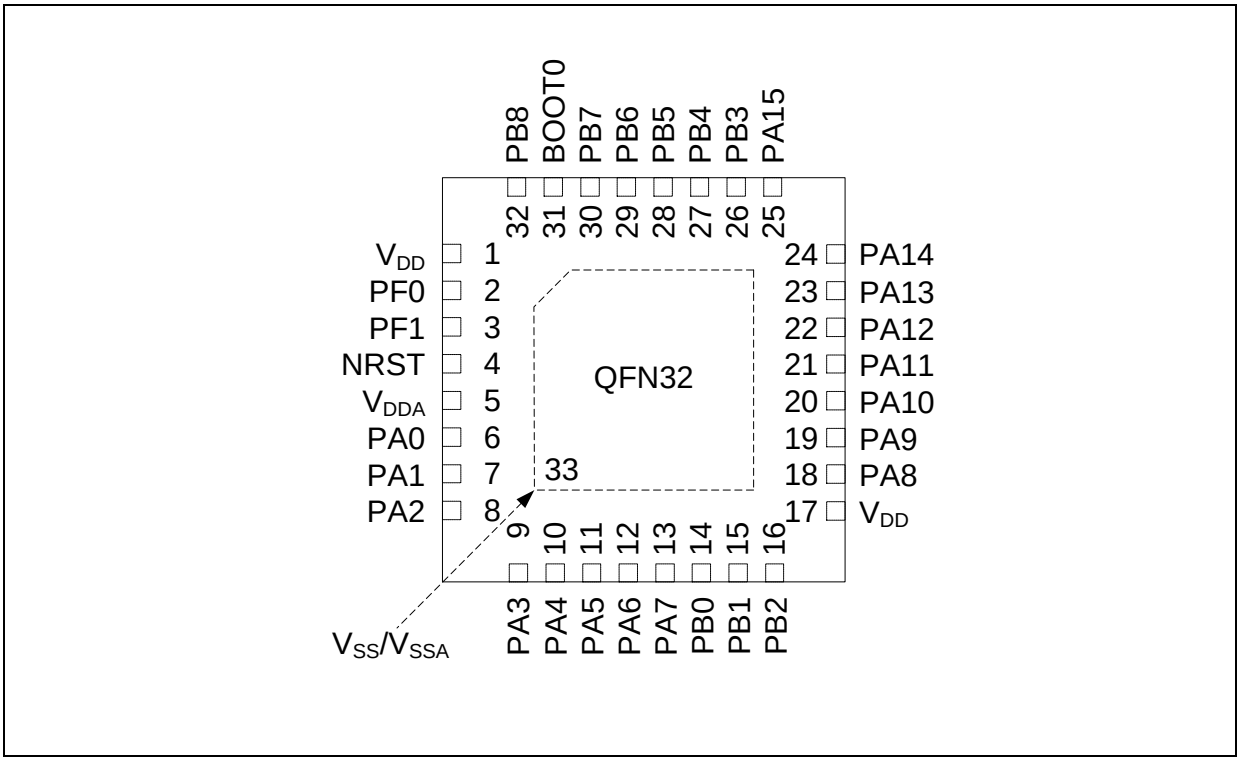
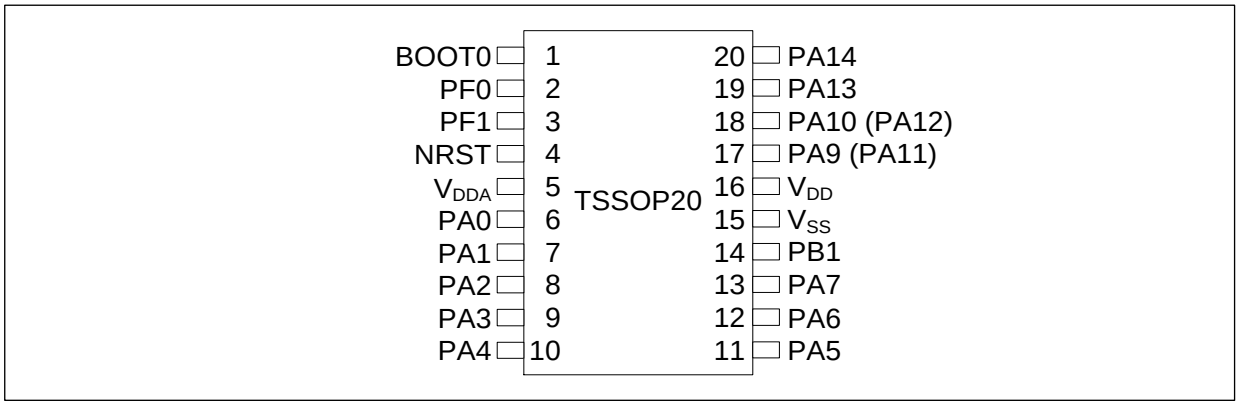


Figure 7. AT32F425 TSSOP20 pinout



The table below is the pin definition of the AT32F425. ”-” represents that there is no such pinout on the related package. Unless descriptions in () under pin name, the function during reset and after reset is the same as the actual pin name. Unless otherwise specified, all GPIOs are set as input floating during reset and after reset. Pin multi-functions are selected via GPIOx_MUXx registers and the additional functions are directly selected and enabled through peripheral registers.

Table 5. AT32F425 series pin definitions

Pin number					Pin name (function after reset)	Type(1)	GPIO level(2)	IOMUX functions	Additional functions
TSSOP20	QFN32	LQFP32	LQFP48/ QFN48	LQFP64					
-	1	1	1	1	V_{DD}	S	-	Digital power supply	
-	-	-	2	2	PC13	I/O	FT	-	ERTC_OUT / TAMP1 / WKUP2
-	-	-	3	3	PC14	I/O	TC	-	LEXT_IN
-	-	-	4	4	PC15	I/O	TC	-	LEXT_OUT
2	2	2	5	5	PF0	I/O	TC	TMR1_CH1	HEXT_IN
3	3	3	6	6	PF1	I/O	TC	TMR1_CH2C / SPI2_CS / I2S2_WS	HEXT_OUT
4	4	4	7	7	NRST	I/O	R	Device reset input / internal reset output (active low)	
-	-	-	-	8	PC0	I/O	FTa	EVENTOUT / I2C2_SCL / I2C1_SCL	ADC1_IN10
-	-	-	-	9	PC1	I/O	FTa	EVENTOUT / I2C2_SDA / SPI3_MOSI / I2S3_SD / SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / I2C1_SDA	ADC1_IN11
-	-	-	-	10	PC2	I/O	FTa	EVENTOUT / SPI2_MISO / I2S2_MCK / I2S_SDEXT	ADC1_IN12
				11	PC3	I/O	FTa	EVENTOUT / SPI2_MOSI / I2S2_SD	ADC1_IN13
-	-	-	8	12	V_{SSA}	S	-	Analog ground	
5	5	5	9	13	V_{DDA}	S	-	Analog power supply	
6	6	6	10	14	PA0	I/O	FTa	USART2_RX / USART2_CTS / TMR2_CH1 / TMR2_EXT / I2C2_SCL / USART4_TX / TMR1_EXT	ADC1_IN0 / WKUP1
7	7	7	11	15	PA1	I/O	FTa	EVENTOUT / USART2_RTS_DE / TMR2_CH2 / I2C2_SDA / USART4_RX / TMR15_CH1C / I2C1_SMBA / SPI3_MOSI / I2S3_SD	ADC1_IN1
8	8	8	12	16	PA2	I/O	FTa	TMR15_CH1 / USART2_TX / TMR2_CH3 / CAN1_RX	ADC1_IN2 / WKUP4
9	9	9	13	17	PA3	I/O	FTa	TMR15_CH2 / USART2_RX / TMR2_CH4 / CAN1_TX / I2S2_MCK	ADC1_IN3
-	-	-	-	18	PF4	I/O	FT	I2C1_SDA / TMR2_CH1	-
-	-	-	-	19	PF5	I/O	FT	I2C1_SCL / TMR2_CH2	-

Pin number					Pin name (function after reset)	Type(1)	GPIO level(2)	IOMUX functions	Additional functions
TSSOP20	QFN32	LQFP32	LQFP48/ QFN48	LQFP64					
10	10	10	14	20	PA4	I/O	FTa	SPI1_CS / I2S1_WS / USART2_CK / OTGFS1_OE / SPI3_CS / I2S3_WS / TMR14_CH1 / I2C1_SCL / SPI2_CS / I2S2_WS	ADC1_IN4
11	11	11	15	21	PA5	I/O	FTa	SPI1_SCK / I2S1_CK / TMR2_CH1 / TMR2_EXT / USART3_CK / USART3_RX	ADC1_IN5
12	12	12	16	22	PA6	I/O	FTa	SPI1_MISO / I2S1_MCK / TMR3_CH1 / TMR1_BRK / USART3_RX / USART3_CTS / TMR16_CH1 / I2S2_MCK / TMR13_CH1	ADC1_IN6
13	13	13	17	23	PA7	I/O	FTa	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR1_CH1C / USART3_TX / TMR14_CH1 / TMR17_CH1 / EVENTOUT / I2C2_SCL	ADC1_IN7
-	-	-	-	24	PC4	I/O	FTa	EVENTOUT / USART3_TX / TMR13_CH1 / I2S1_MCK	ADC1_IN14
-	-	-	-	25	PC5	I/O	FTa	USART3_RX	ADC1_IN15 / WKUP5
-	14	14	18	26	PB0	I/O	FTa	EVENTOUT / TMR3_CH3 / TMR1_CH2C / USART2_RX / USART3_CK / SPI1_MISO / I2S1_MCK	ADC1_IN8
14	15	15	19	27	PB1	I/O	FTa	TMR14_CH1 / TMR3_CH4 / TMR1_CH3C / USART2_CK / USART3_RTS_DE / SPI2_SCK / I2S2_CK / SPI1_MOSI / I2S1_SD	ADC1_IN9
-	16	-	20	28	PB2	I/O	FTa	TMR3_EXT / SPI3_MOSI / I2S3_SD / I2C1_SMBA	-
-	-	-	21	29	PB10	I/O	FT	I2C2_SCL / TMR2_CH3 / USART3_TX / SPI2_SCK / I2S2_CK	-
-	-	-	22	30	PB11	I/O	FT	EVENTOUT / I2C2_SDA / TMR2_CH4 / USART3_RX	-
15	-	16	23	31	V_{SS}	S	-	Digital ground	
16	17	17	24	32	V_{DD}	S	-	Digital power supply	
-	-	-	25	33	PB12	I/O	FT	SPI2_CS / I2S2_WS / EVENTOUT / TMR1_BRK / USART3_CK / TMR15_BRK / SPI3_CS / I2S3_WS / I2C2_SMBA	-
-	-	-	26	34	PB13	I/O	FTf	SPI2_SCK / I2S2_CK / TMR15_CH1C / TMR1_CH1C / CLKOUT / USART3_CTS / I2C2_SCL / SPI3_SCK / I2S3_CK	-

Pin number					Pin name (function after reset)	Type[1]	GPIO level[2]	IOMUX functions	Additional functions
TSSOP20	QFN32	LQFP32	LQFP48/ QFN48	LQFP64					
-	-	-	27	35	PB14	I/O	FTf	SPI2_MISO / I2S2_MCK / TMR15_CH1 / TMR1_CH2C / I2S_SDEXT / USART3_RTS_DE / I2C2_SDA / SPI3_MISO / I2S3_MCK	-
-	-	-	28	36	PB15	I/O	FT	SPI2_MOSI / I2S2_SD / TMR15_CH2 / TMR1_CH3C / TMR15_CH1C / ERTC_REFIN / SPI3_MOSI / I2S3_SD	WKUP7
-	-	-	-	37	PC6	I/O	FT	TMR3_CH1 / I2C1_SCL / TMR1_CH1 / I2S2_MCK	-
-	-	-	-	38	PC7	I/O	FT	TMR3_CH2 / I2C1_SDA / TMR1_CH2 / I2S2_MCK / SPI2_SCK / I2S2_CK	-
-	-	-	-	39	PC8	I/O	FT	TMR3_CH3 / TMR1_CH3	-
-	-	-	-	40	PC9	I/O	FT	TMR3_CH4 / I2C2_SDA / TMR1_CH4 / OTGFS1_OE / I2C1_SDA	-
-	18	18	29	41	PA8	I/O	FT	CLKOUT / USART1_CK / TMR1_CH1 / OTGFS1_SOF / USART2_TX / EVENTOUT / I2C2_SCL	-
-	19	19	30	42	PA9	I/O	FT	TMR15_BRK / USART1_TX / TMR1_CH2 / OTGFS1_VBUS / I2C1_SCL / CLKOUT / SPI3_SCK / I2S3_CK / I2C2_SMBA	-
-	20	20	31	43	PA10	I/O	FT	TMR17_BRK / USART1_RX / TMR1_CH3 / OTGFS1_ID / I2C1_SDA / ERTC_REFIN / SPI3_MOSI / I2S3_SD	-
17[3]	-	-	-	-	PA9	I/O	TC[4]	TMR15_BRK / USART1_TX / TMR1_CH2 / I2C1_SCL / CLKOUT / I2C2_SMBA	-
18[3]	-	-	-	-	PA10	I/O	TC[4]	TMR17_BRK / USART1_RX / TMR1_CH3 / I2C1_SDA / ERTC_REFIN	-
17[3]	21	21	32	44	PA11	I/O	TC	EVENTOUT / USART1_CTS / TMR1_CH4 / SPI3_CS / I2S3_WS / CAN1_RX / I2C2_SCL / I2C1_SMBA	OTGFS1_D-[3]
18[3]	22	22	33	45	PA12	I/O	TC	EVENTOUT / USART1_RTS_DE / TMR1_EXT / CAN1_TX / I2C2_SDA / SPI3_MISO / I2S3_MCK	OTGFS1_D+[3]
19	23	23	34	46	PA13 (SWDIO[5])	I/O	FT	PA13 / IR_OUT / OTGFS1_OE / I2S_SDEXT / SPI3_MISO / I2S3_MCK / I2C1_SDA / SPI2_MISO / I2S2_MCK	-
-	-	-	35	47	PF6	I/O	FT	I2C2_SCL / USART4_RX	-
-	-	-	36	48	PF7	I/O	FT	I2C2_SDA / USART4_TX	-

Pin number					Pin name (function after reset)	Type(1)	GPIO level(2)	IOMUX functions	Additional functions
TSSOP20	QFN32	LQFP32	LQFP48/ QFN48	LQFP64					
20	24	24	37	49	PA14 (SWCLK(5))	I/O	FT	PA14 / USART2_TX / SPI3_MOSI / I2S3_SD / I2C1_SMBA / SPI2_MOSI / I2S2_SD	-
-	25	25	38	50	PA15	I/O	FT	SPI1_CS / I2S1_WS / USART2_RX / TMR2_CH1 / TMR2_EXT / EVENTOUT / USART4_RTS_DE / OTGFS1_OE / SPI2_CS / I2S2_WS / SPI3_CS / I2S3_WS	-
-	-	-	-	51	PC10	I/O	FT	USART4_TX / USART3_TX / SPI3_SCK / I2S3_CK	-
-	-	-	-	52	PC11	I/O	FT	USART4_RX / USART3_RX / I2S_SDEXT / SPI3_MISO / I2S3_MCK	-
-	-	-	-	53	PC12	I/O	FT	USART4_CK / USART3_CK / SPI3_MOSI / I2S3_SD	-
-	-	-	-	54	PD2(6)	I/O	FT	TMR3_EXT / USART3_RTS_DE	-
-	26	26	39	55	PB3	I/O	FT	SPI1_SCK / I2S1_CK / EVENTOUT / TMR2_CH2 / USART1_RTS_DE / USART2_CTS / SPI2_SCK / I2S2_CK / SWO	-
-	27	27	40	56	PB4	I/O	FT	SPI1_MISO / I2S1_MCK / TMR3_CH1 / EVENTOUT / I2S_SDEXT / USART1_CTS / TMR17_BRK / SPI2_MISO / I2S2_MCK / I2C1_SDA	-
-	28	28	41	57	PB5	I/O	FT	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR16_BRK / I2C1_SMBA / USART1_CK / USART2_RTS_DE / SPI2_MOSI / I2S2_SD	WKUP6
-	29	29	42	58	PB6	I/O	FT	USART1_TX / I2C1_SCL / TMR16_CH1C / USART4_CK / I2S1_MCK / SPI3_CS / I2S3_WS	-
-	30	30	43	59	PB7	I/O	FT	USART1_RX / I2C1_SDA / TMR17_CH1C / USART4_CTS / SPI3_SCK / I2S3_CK	-
1	31	31	44	60	BOOT0	I	B	Boot mode 0	
-	32	-	45	61	PB8	I/O	FTf	USART1_TX / I2C1_SCL / TMR16_CH1 / EVENTOUT / CAN1_RX / SPI3_MISO / I2S3_MCK	-
-	-	-	46	62	PB9	I/O	FTf	IR_OUT / I2C1_SDA / TMR17_CH1 / EVENTOUT / CAN1_TX / SPI2_CS / I2S2_WS / I2S1_MCK / SPI3_MOSI / I2S3_SD	-

Pin number					Pin name (function after reset)	Type(1)	GPIO level(2)	IOMUX functions	Additional functions
TSSOP20	QFN32	LQFP32	LQFP48/ QFN48	LQFP64					
-	-	32	47	63	V_{SS}	S	-	Digital ground	
-	-	-	48	64	V_{DD}	S	-	Digital power supply	
-	-	-	-/49	-	EPAD (V_{SS})	S	-	Digital ground	
-	33	-	-	-	EPAD (V_{SS}/V_{SSA})	S	-	Digital ground / Analog ground	

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Among them, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when configured as analog mode. In this case, its input level should not higher than V_{DD} + 0.3 V.

(3) For the TSSOP20 package, if OTGFS1 is disabled, it is possible to replace PA9/PA10 and its multiplexed functions with PA11/PA12 and their multiplexed functions by means of software remapping. If OTGFS1 is enabled, PA9/PA10/PA11/PA12 and their relevant multiplexed functions will be owned by OTGFS1_D- and OTGFS1_D+. In this case, The OTGFS1_VBUS and OTGFS1_ID signals are not present, and some of OTG function are restricted when used as a host.

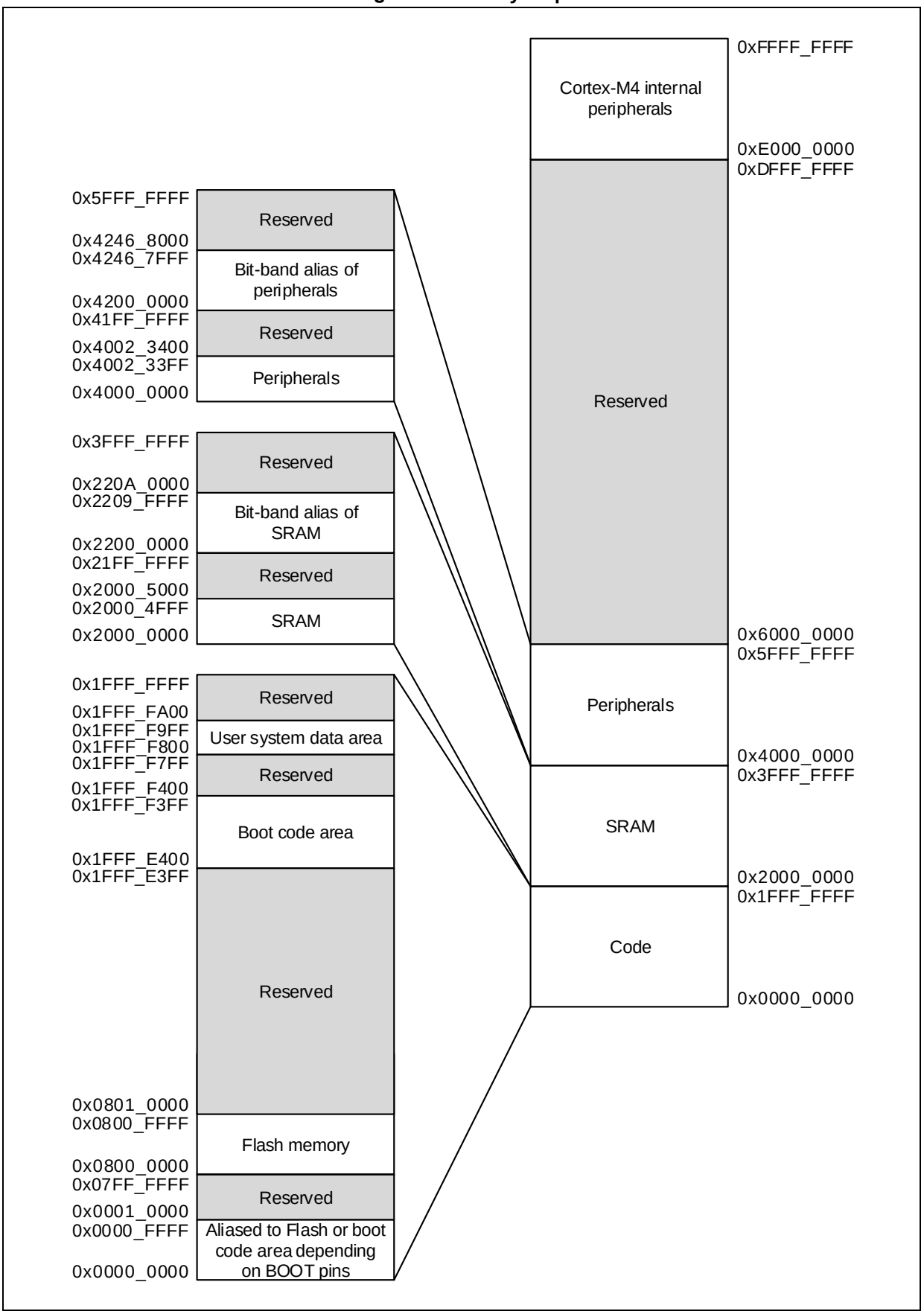
(4) PA9/PA10 in the TSSOP20 package are not FT 5 V tolerant.

(5) After any reset, PA13/PA14 is used as its multiplexed function SWDIO/SWCLK, and the internal pull-up resistor of SWDIO and the internal pull-down resistor of SWCLK are both ON.

(6) When LEXT is enabled, PD2 and its multiple functions cannot be used.

4 Memory mapping

Figure 8. Memory map



5 Electrical characteristics

5.1 Test conditions

5.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical values

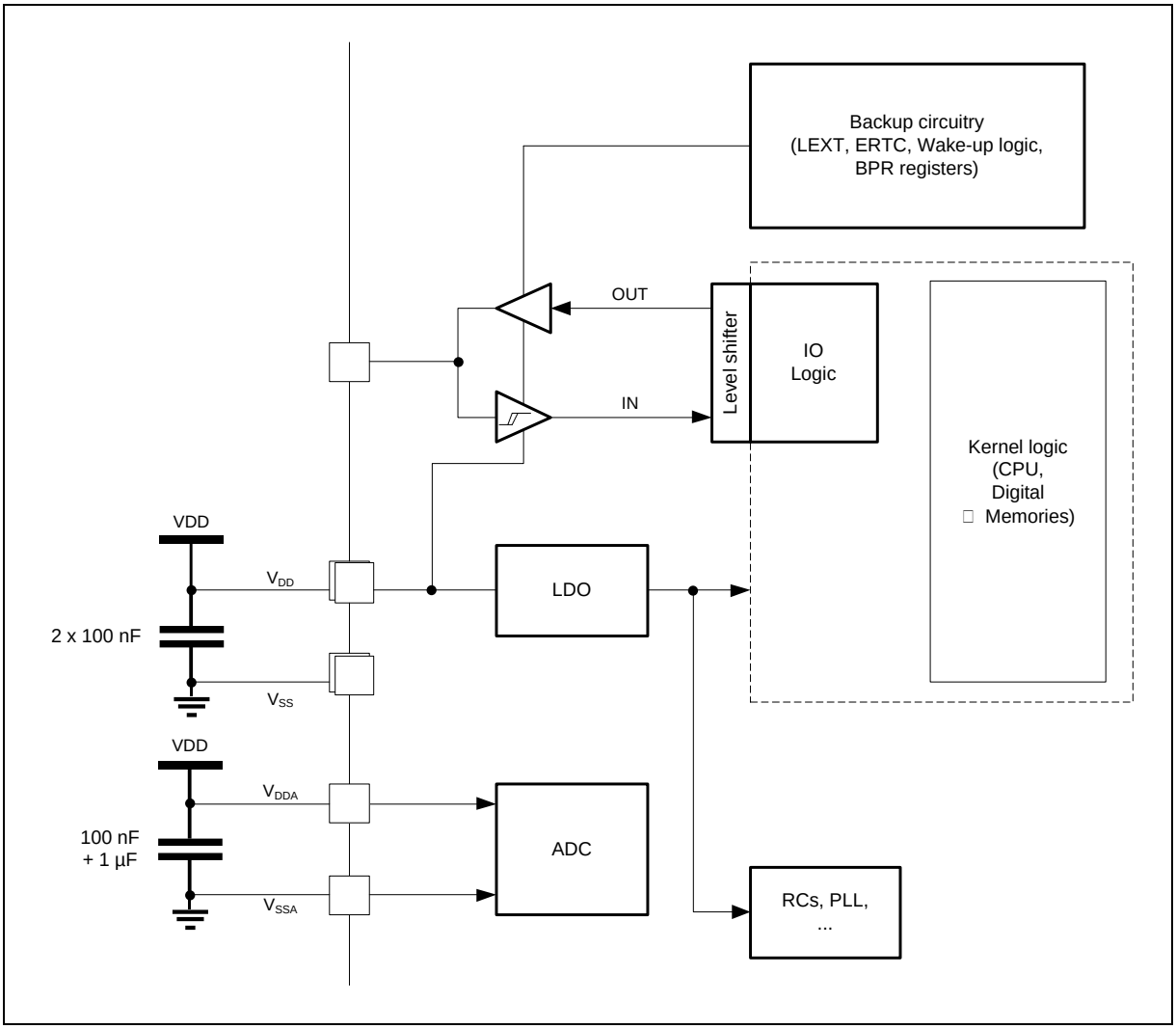
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

5.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

5.1.4 Power supply scheme

Figure 9. Power supply scheme



5.2 Absolute maximum values

5.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 6*, *Table 7*, and *Table 8,* it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 6. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	4.0	V
V_{IN}	Input voltage on FT and FTf GPIO	V_{SS}-0.3	6.0	
	Input voltage on FTa GPIO (set as input floating, input pull-up, or input pull-down mode)			
	Input voltage on TC GPIO	V_{SS}-0.3	4.0	
	Input voltage on FTa GPIO (set as analog mode)			
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 7. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	External main supply voltage (including V_{DDA} and V_{DD})	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIOs and control pin	-25	

Table 8. Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2017/JS-002-2018 standard.

Table 9. ESD values

Symbol	Parameter	Conditions	Class	Min(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2018	III	±2000	

(1) Guaranteed by characterization results, not tested in production.

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 10. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (±200 mA)

5.3 Specifications

5.3.1 General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	HalfCycle disabled	0	96	MHz
		HalfCycle enabled	0	80	
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-	0	f_{HCLK}	MHz
V_{DD}	Digital operating voltage	-	2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}	V_{DD}		V
P_D	Power dissipation: T_A = 105 °C	LQFP64 (10 x 10 mm)	-	242	mW
		LQFP64 (7 x 7 mm)	-	234	
		LQFP48 (7 x 7 mm)	-	234	
		QFN48 (6 x 6 mm)	-	585	
		LQFP32 (7 x 7 mm)	-	234	
		QFN32 (4 x 4 mm)		370	
		TSSOP20 (6.5 x 4.4 mm)		195	
T_A	Ambient temperature	-	-40	105	°C

5.3.2 Operating conditions at power-up / power-down

Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	ms/V
	V_{DD} fall time rate		20	∞	μs/V

5.3.3 Embedded reset and power control block characteristics

Table 13. Embedded reset and power management block characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}(1)	Power on reset threshold	1.91	2.11	2.4	V
V_{LVR}(1)	Low voltage reset threshold	1.78(2)	1.93	2.08	V
$V_{LVRhyst}$(1)	LVR hysteresis	-	180	-	mV
$T_{RSTTEMPO}$(1)	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	3.5	-	ms

(1) Guaranteed by design, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 10. Power on reset and low voltage reset waveform

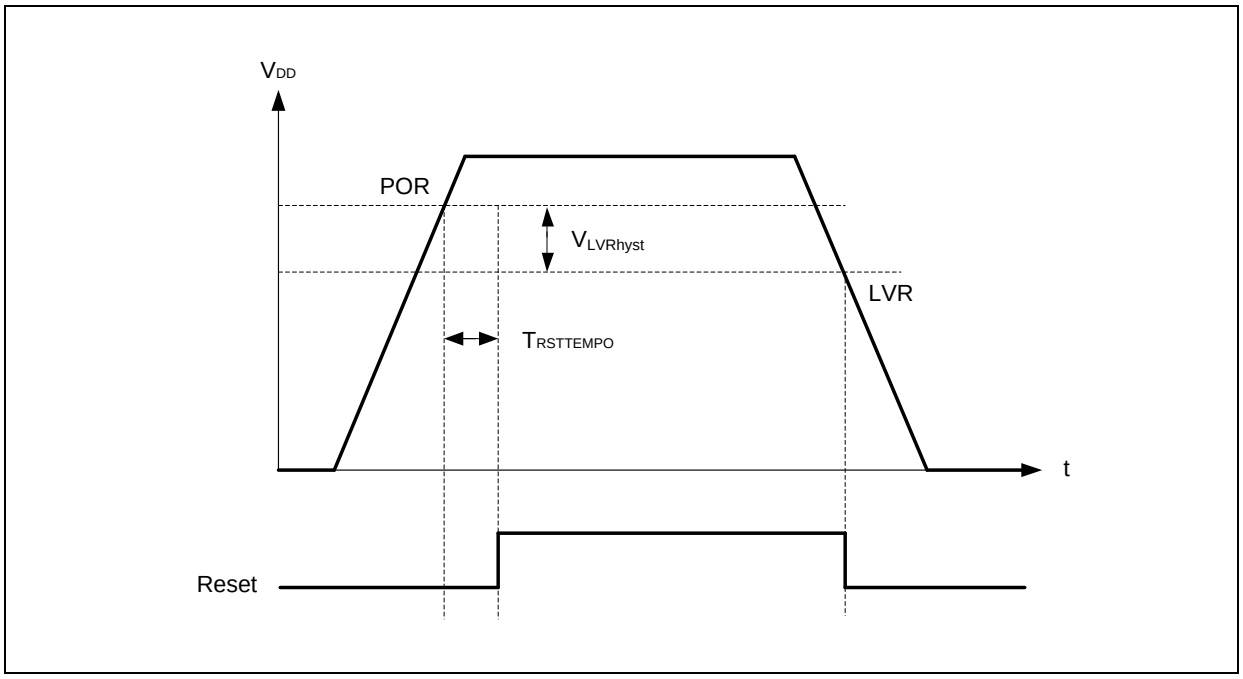


Table 14. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold1 (PLS[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PLS[2:0] = 010)	Rising edge(2)	2.28	2.38	2.48	V
		Falling edge (2)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PLS[2:0] = 011)	Rising edge (2)	2.38	2.48	2.58	V
		Falling edge (2)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PLS[2:0] = 100)	Rising edge (2)	2.47	2.58	2.69	V
		Falling edge (2)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PLS[2:0] = 101)	Rising edge (2)	2.57	2.68	2.79	V
		Falling edge (2)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PLS[2:0] = 110)	Rising edge (2)	2.66	2.78	2.9	V
		Falling edge (2)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PLS[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVMhyst}$(2)	PVM hysteresis	-	-	100	-	mV
$I_{DD\ (PVM)}$	PVM current dissipation	-	-	20	30(2)	µA

(1) PLS[2:0] = 001 level may not be used because it is lower than V_{POR}.
(2) Guaranteed by design, not tested in production.

5.3.4 Memory characteristics

Table 15. Internal Flash memory characteristics

Symbol	Parameter	Typ(1)	Max(1)	Unit
T_{PROG}	Programming time	60	65	μs
t_{SE}	Page erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 16. Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on the f_{HCLK} frequency (0 ~ 32 MHz : zero-wait state; 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states)
- Prefetch ON; HalfCycle OFF
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 17. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	96 MHz	17.7	7.88	mA
			72 MHz	13.5	6.09	
			48 MHz	9.52	4.62	
			36 MHz	7.32	3.65	
			24 MHz	5.44	2.99	
			16 MHz	3.87	2.24	
			8 MHz	1.94	1.20	
			4 MHz	1.31	0.94	
			2 MHz	1.00	0.81	
			1 MHz	0.83	0.74	
			500 kHz	0.76	0.71	
			125 kHz	0.70	0.69	
		High speed internal clock (HICK)(2)	96 MHz	17.6	7.76	mA
			72 MHz	13.4	5.96	
			48 MHz	9.41	4.48	
			36 MHz	7.20	3.50	
			24 MHz	5.30	2.83	
			16 MHz	3.72	2.08	
			8 MHz	1.78	1.03	
			4 MHz	1.15	0.78	
			2 MHz	0.82	0.64	
			1 MHz	0.67	0.58	
			500 kHz	0.59	0.54	
			125 kHz	0.53	0.52	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1)(2)	96 MHz	14.2	3.03	mA
			72 MHz	10.8	2.45	
			48 MHz	7.77	2.19	
			36 MHz	6.01	1.82	
			24 MHz	4.56	1.77	
			16 MHz	3.29	1.43	
			8 MHz	1.65	0.80	
			4 MHz	1.16	0.74	
			2 MHz	0.92	0.71	
			1 MHz	0.80	0.69	
			500 kHz	0.74	0.69	
			125 kHz	0.69	0.68	
		High speed internal clock (HICK)(2)	96 MHz	14.1	2.87	mA
			72 MHz	10.7	2.29	
			48 MHz	7.66	2.03	
			36 MHz	5.88	1.67	
			24 MHz	4.42	1.61	
			16 MHz	3.14	1.26	
			8 MHz	1.49	0.63	
			4 MHz	1.00	0.57	
			2 MHz	0.75	0.54	
			1 MHz	0.63	0.53	
			500 kHz	0.57	0.52	
			125 kHz	0.53	0.51	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 19. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	96 MHz	17.9	18.1	mA
			72 MHz	13.7	13.9	
			48 MHz	9.72	9.90	
			36 MHz	7.52	7.70	
			24 MHz	5.64	5.83	
			16 MHz	4.08	4.26	
			8 MHz	2.17	2.36	
		High speed external crystal (HEXT)(1), all peripherals disabled	96 MHz	8.08	8.25	mA
			72 MHz	6.30	6.48	
			48 MHz	4.83	5.01	
			36 MHz	3.86	4.04	
			24 MHz	3.21	3.39	
			16 MHz	2.46	2.64	
			8 MHz	1.44	1.61	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	96 MHz	14.4	14.6	mA
			72 MHz	11.1	11.3	
			48 MHz	7.99	8.17	
			36 MHz	6.22	6.40	
			24 MHz	4.78	4.96	
			16 MHz	3.51	3.69	
			8 MHz	1.89	2.07	
		High speed external crystal (HEXT)(1), all peripherals disabled	96 MHz	3.25	3.44	mA
			72 MHz	2.68	2.87	
			48 MHz	2.42	2.60	
			36 MHz	2.05	2.23	
			24 MHz	2.00	2.18	
			16 MHz	1.65	1.84	
			8 MHz	1.03	1.22	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 21. Typical and maximum current consumptions in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)		Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode (3)	LDO in normal mode, HICK and HEXT OFF, WDT OFF	243	246	468	675	µA
		LDO in low-power mode, LPDS1=1, HICK and HEXT OFF, WDT OFF	121	123	259	402	
	Supply current in Standby mode	LEXT and ERTC OFF	2.3	3.5	5.9	8.2	µA
		LEXT and ERTC ON	3.3	5.0	7.2	9.6	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) CRM_AHBEN[4] (FLASHEN) must be set before entering Deepsleep mode, otherwise, an additional power consumption of around 50 µA would be added.

Figure 11. Typical current consumption in Deepsleep mode with LDO in run mode vs. temperature at different V_{DD}

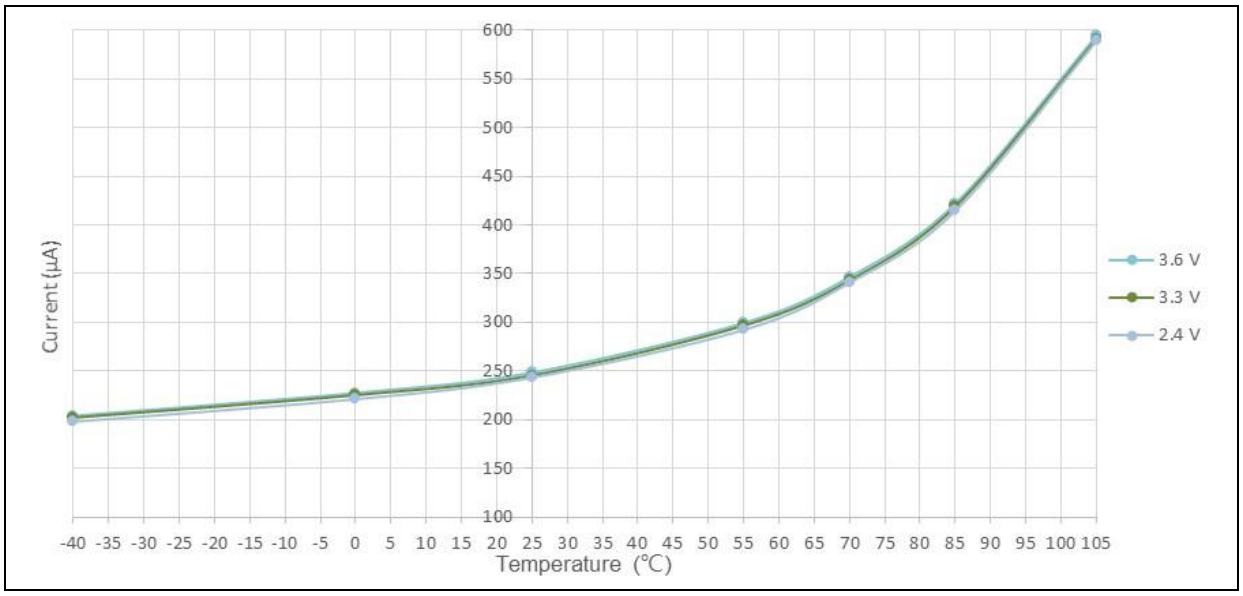


Figure 12. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

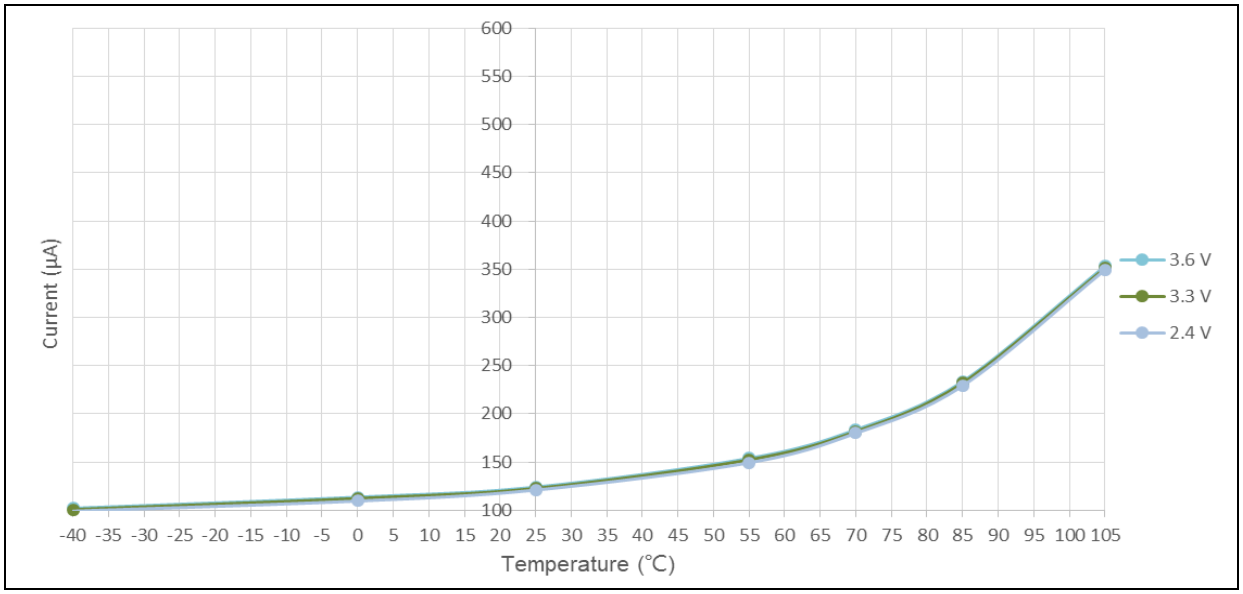
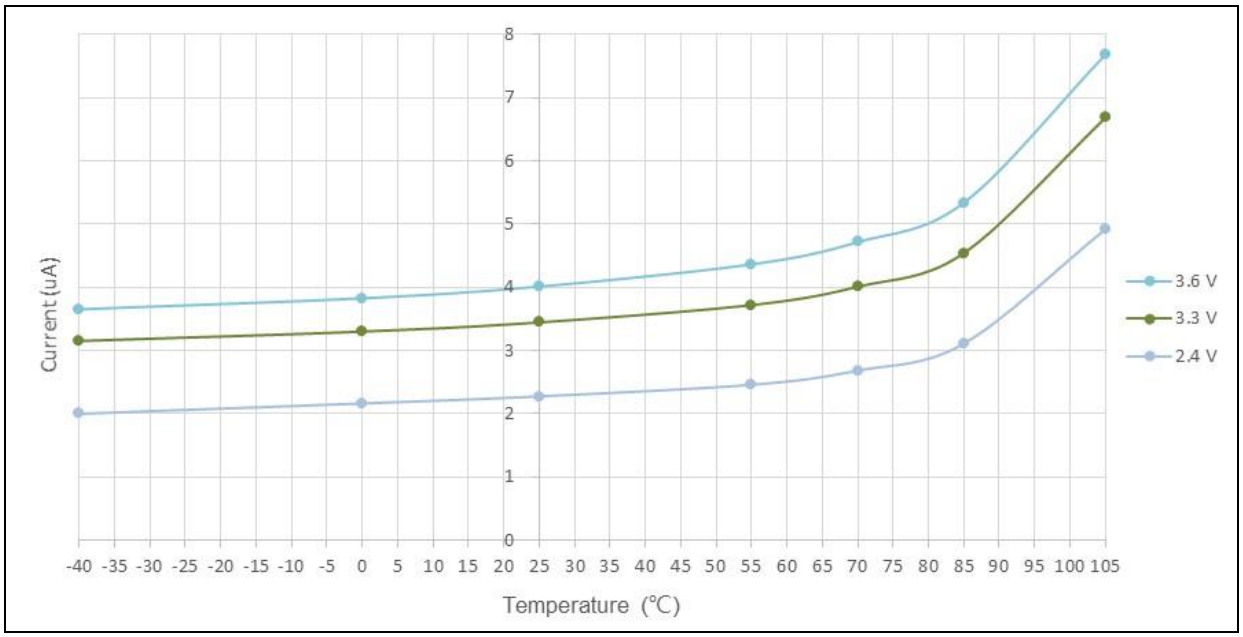


Figure 13. Typical current consumption in Standby mode vs. temperature at different V_{DD}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 22. Peripheral current consumption

Peripheral		Typ	Unit
AHB	DMA1	2.20	μA/MHz
	SRAM	0.56	
	Flash	11.6	
	CRC	0.53	
	OTGFS1	23.6	
	GPIOA	0.62	
	GPIOB	0.58	
	GPIOC	0.57	
	GPIOD	0.55	
	GPIOF	0.56	
APB1	TMR2	9.47	
	TMR3	6.71	
	TMR6	0.86	
	TMR7	0.86	
	TMR13	2.63	
	TMR14	2.58	
	WWDT	0.33	
	SPI2/I^2S2	1.91	
	SPI3/I^2S3	1.92	
	USART2	2.06	
	USART3	2.09	
	USART4	2.11	
	I^2C1	6.11	
	I^2C2	5.88	
	CAN1	2.26	
	ACC	0.26	
	PWC	6.27	
APB2	SCFG	0.17	
	ADC1	1.90	
	TMR1	9.21	
	SPI1/I^2S1	1.88	
	USART1	2.11	
	TMR15	5.16	
	TMR16	3.55	
	TMR17	3.62	

5.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

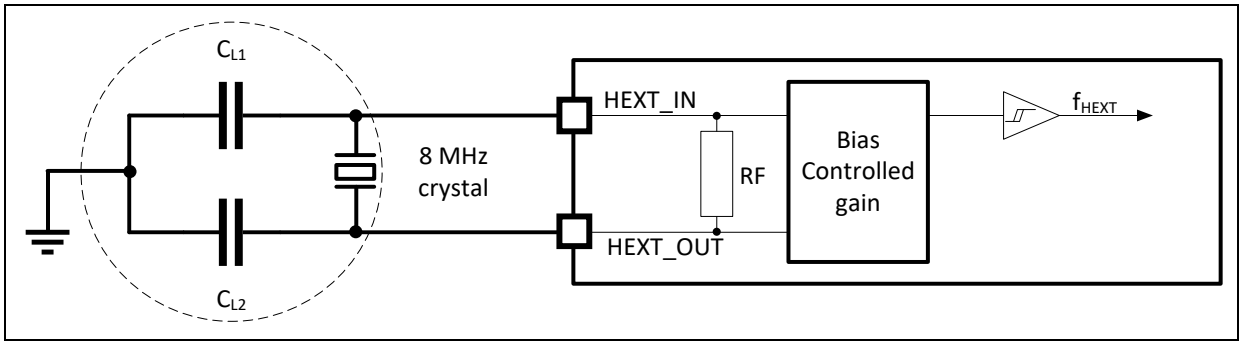
Table 23. HEXT 4-25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting C_{L1} and C_{L2}.

Figure 14. HEXT typical application with an 8 MHz crystal



High-speed external clock generated from an external source

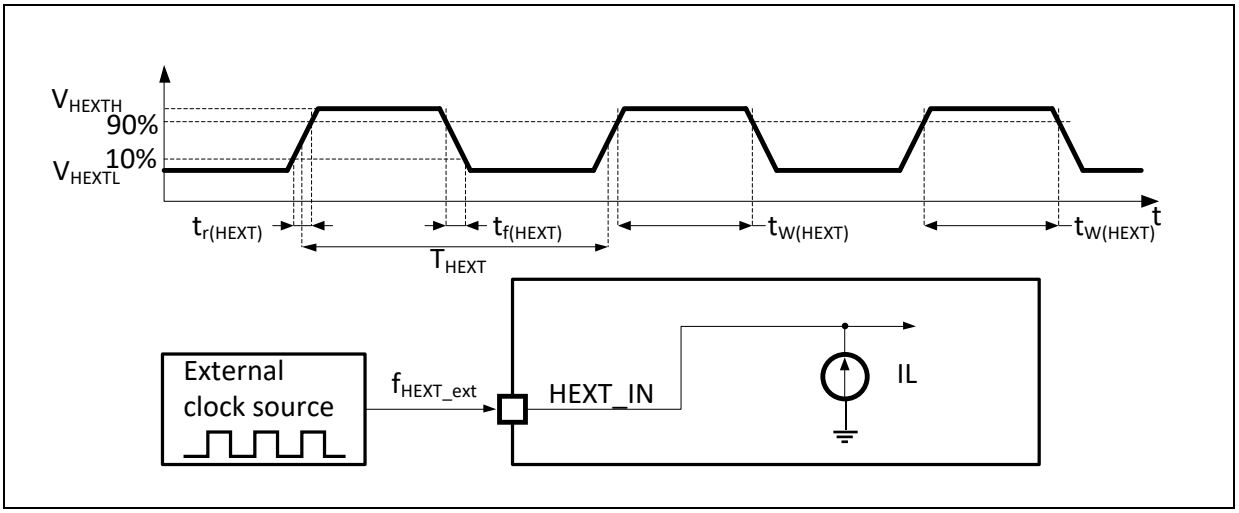
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 24. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 15. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25. LEXT 32.768 kHz crystal characteristics(1)(2)

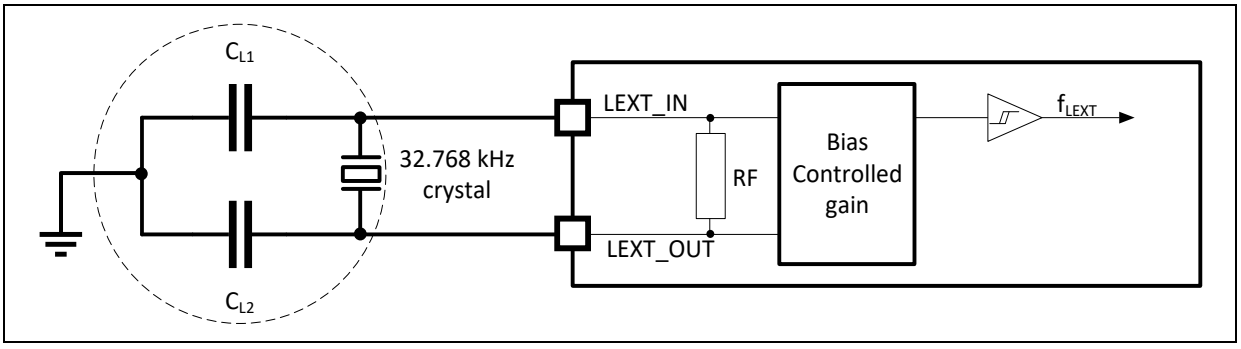
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	200	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 16. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

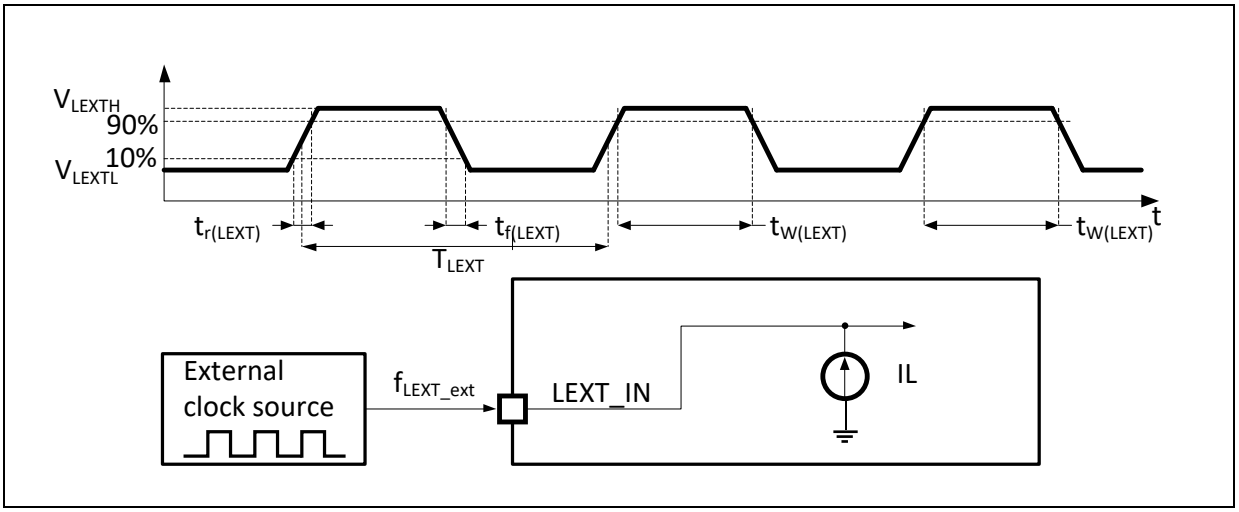
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 26. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)	-	450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)	-	-	-	50	ns
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 17. LEXT external source AC timing diagram



5.3.7 Internal clock source characteristics

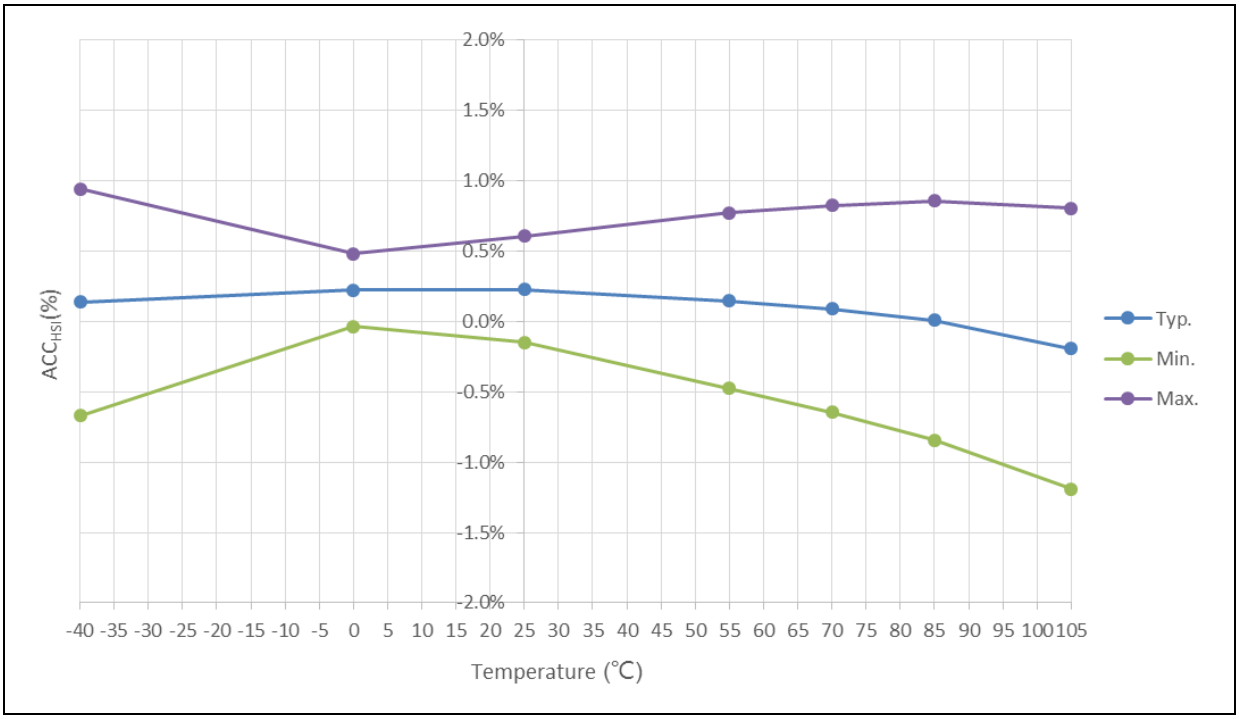
High-speed internal clock (HICK)

Table 27. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CMR_CTRL register		-	-	1(1)	%
		ACC-trimmed		-	-	0.25(1)	
		Factory-calibrated(2)	T_A = -40 ~ 105 °C	-2		2	%
			T_A = -40 ~ 85 °C	-1.5	-	1.5	
			T_A = 0 ~ 70 °C	-1	-	1	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	-	10	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	230	240	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 18. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 28. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	25	35	45	kHz

(1) Guaranteed by characterization results, not tested in production.

5.3.8 PLL characteristics

Table 29. PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	96	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by characterization results, not tested in production.
(2) Take case of using the appropriate multiplier factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

5.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

Table 30. Low-power mode wakeup time

Symbol	Parameter Conditions	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	3.3	µs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode (LDO in Run mode)	380	µs
	Wakeup from Deepsleep mode (LDO in low-power mode)	450	
$t_{WUSTDBY}$	Wakeup from Standby mode	800	µs

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error, V_{DD} and V_{SS} input has one 47 µF capacitor and each V_{DD} and V_{SS} pin pair 0.1 µF	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 96 MHz, HalfCycle = 0, conforms to IEC 61000-4-4	4A (±4 kV)
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 80 MHz, HalfCycle = 1, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

5.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 32. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	–0.3	-	0.28 * V_{DD} + 0.1	V
V_{IH}	TC GPIO input high level voltage	-	0.31 * V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa GPIO input high level voltage	Analog mode				
	FT and FTf GPIO input high level voltage	-		-	5.5	
	FTa GPIO input high level voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIOs	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5V$ FT, FTf and FTa GPIO	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	65	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = V_{DD}$	65	70	130	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in *Section 5.2.1*:

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 33. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} ≤ 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 5 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} ≤ 2.7 V	V_{DD}-0.4		
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} ≤ 2.7 V	V_{DD}-0.4	-	
Ultra high sinking strength(2)					
V_{OL}	Output low level voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA, 2.4 V ≤ V_{DD} ≤ 2.7 V			

(1) Guaranteed by characterization results.
(2) When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 34. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

5.3.12 NRST pin characteristics

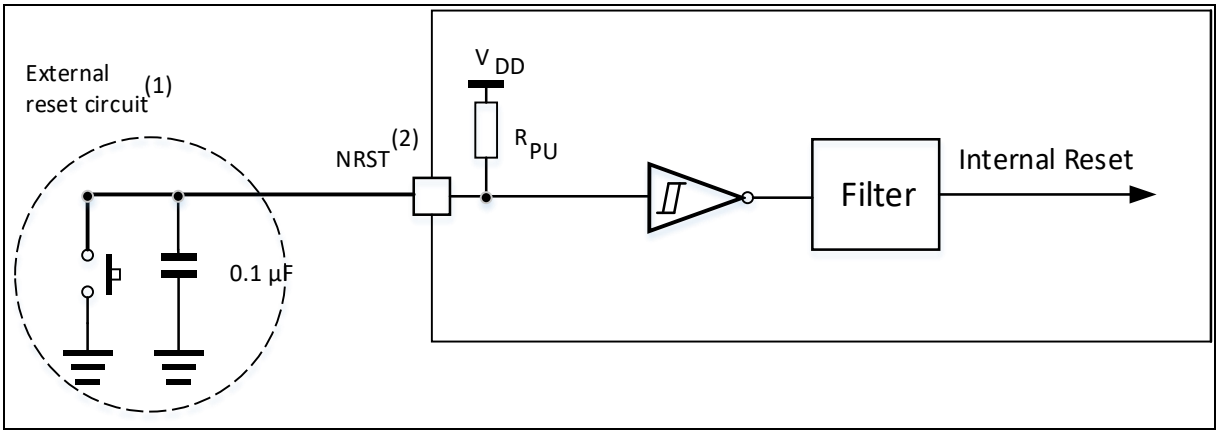
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 35. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	40	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	80	-	-	μs

(1) Guaranteed by design.

Figure 19. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in *Table 35*. Otherwise the reset will not be performed by the device.

5.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 36. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 96 MHz	10.42	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

5.3.14 SPI / I²S characteristics

The parameters are listed in *Table 37* for SPI and in *Table 38* for I²S.

Table 37. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency$^{(2)(3)}$	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	32	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, f_{PCLK} = 100 MHz, prescaler = 4	15	25	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	5	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input setup time	Master mode	5	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	4	-	
$t_{a(SO)}^{(1)(4)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	2	-	

(1) Guaranteed by characterization results, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 20. SPI timing diagram - slave mode and CPHA = 0

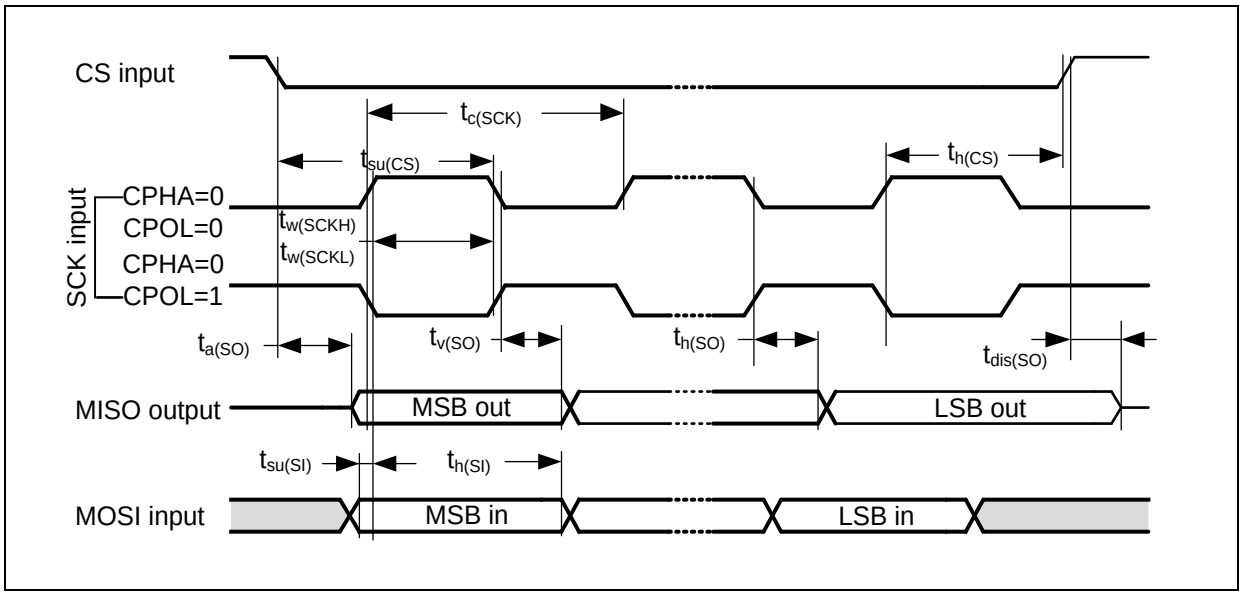


Figure 21. SPI timing diagram - slave mode and CPHA = 1

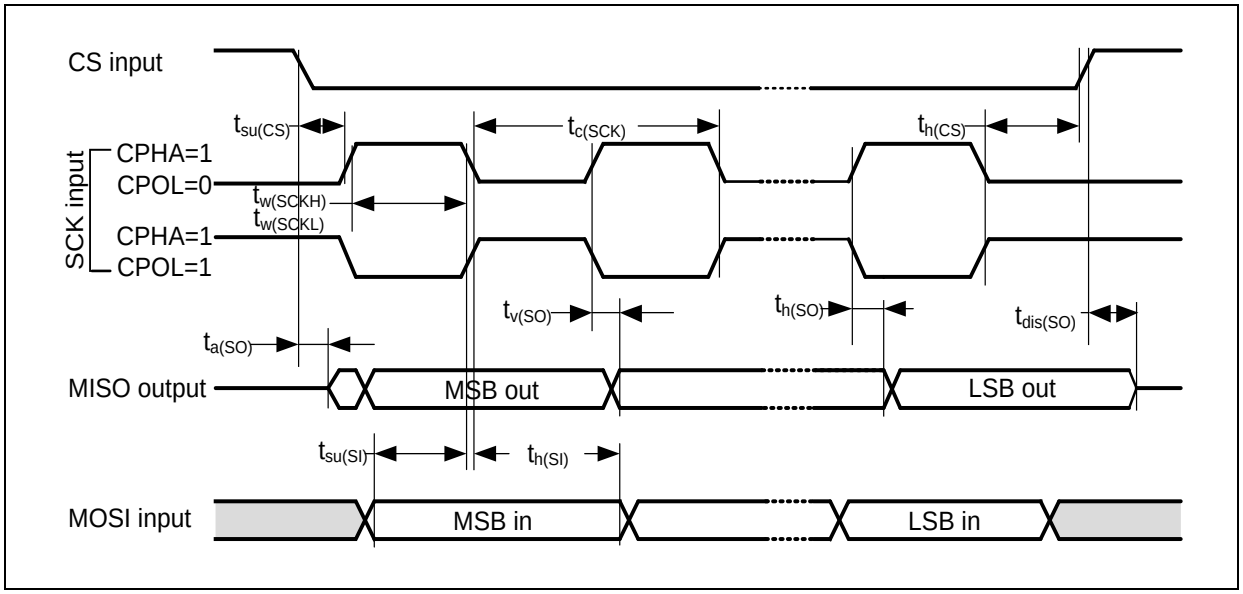


Figure 22. SPI timing diagram - master mode

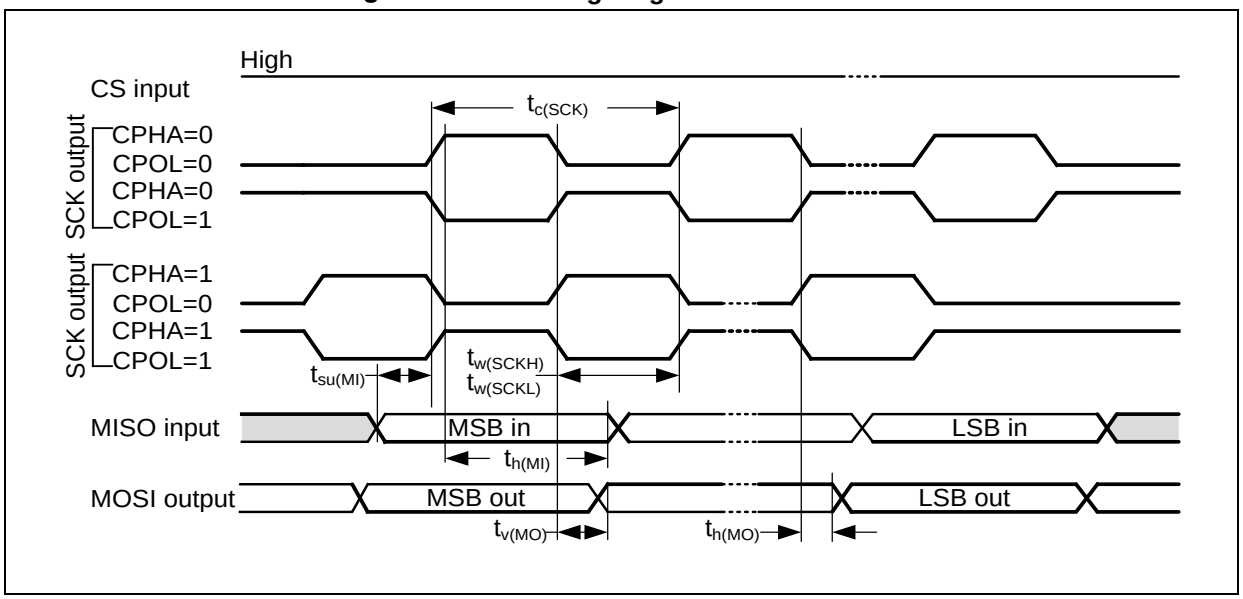
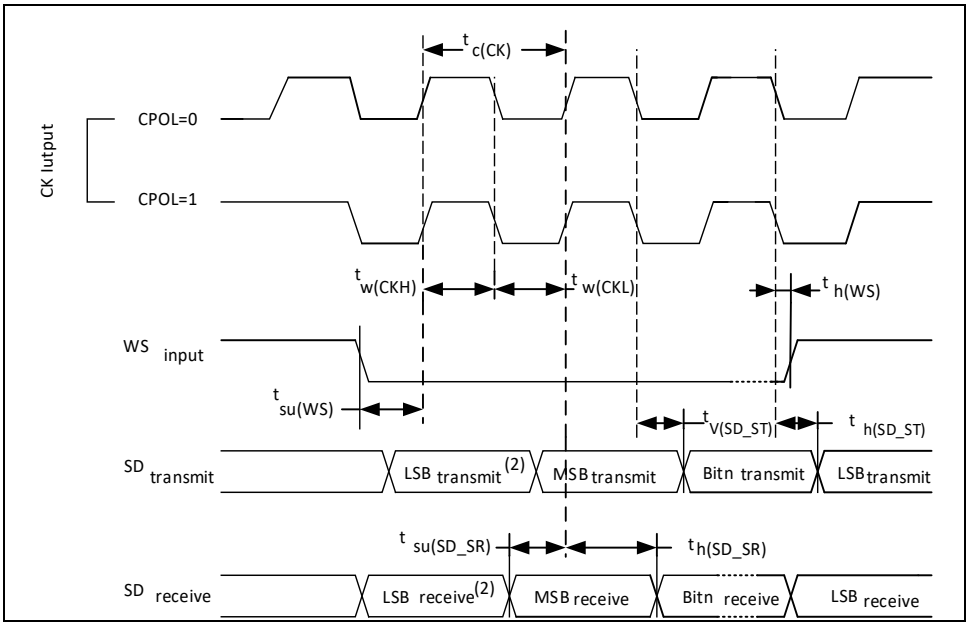


Table 38. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 50 pF	-	8	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	3	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6.5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	11	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

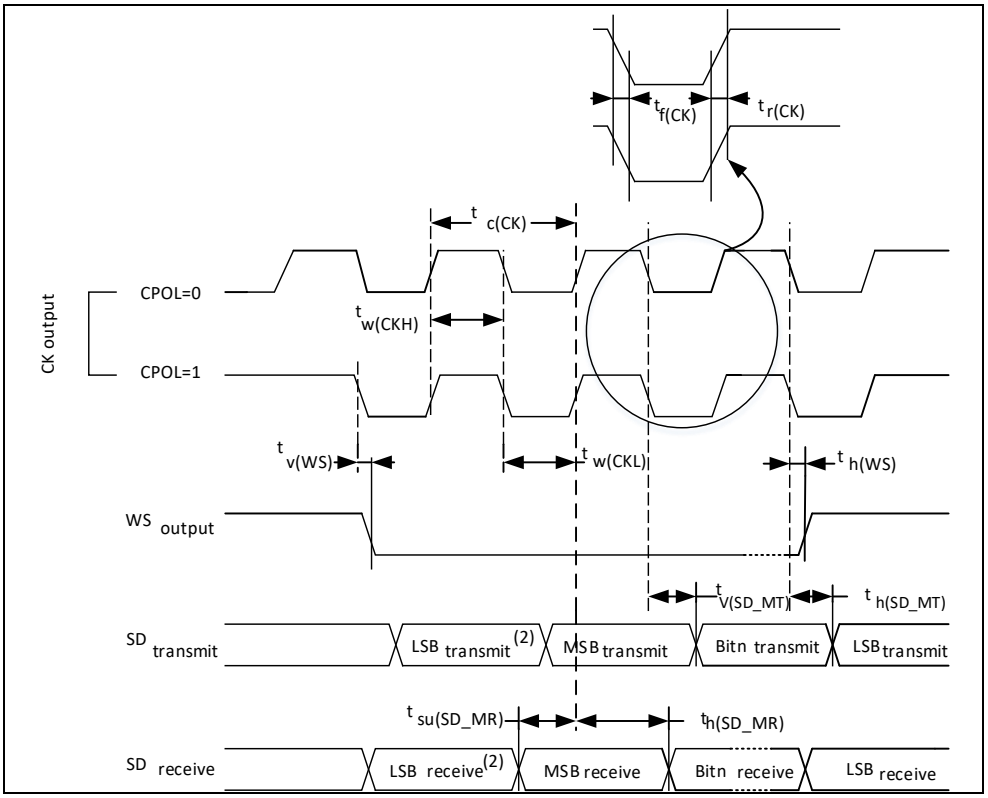
(1) Guaranteed by design and/or characterization results.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 23. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 24. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

5.3.15 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not ”true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

5.3.16 OTGFS characteristics

Table 39. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	µs

(1) Guaranteed by design, not tested in production.

Table 40. OTGFS DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I (OTGFS_D+/D-)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PU}		OTGFS_D+ internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
R_{PD}		OTGFS_D+/D- internal pull-up	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F452 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by characterization results, not tested in production.
(4) R_L is the load connected on the USB drivers.

Figure 25. OTGFS timings: definition of data signal rise and fall time

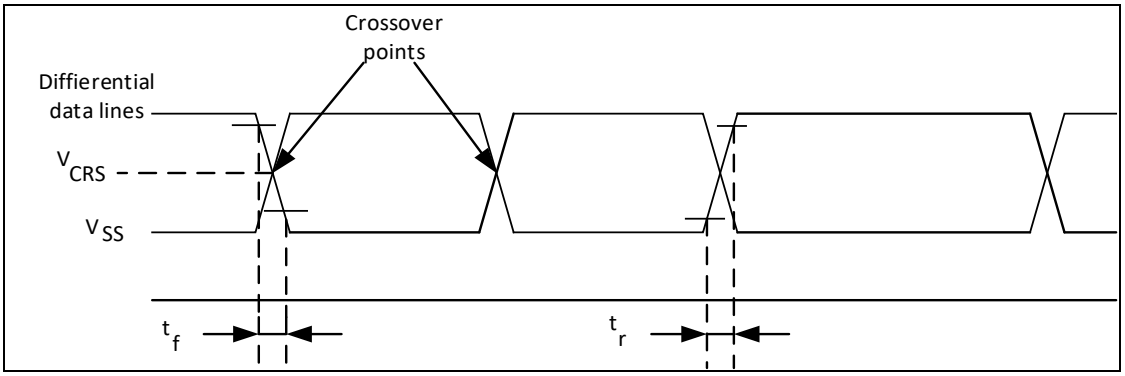


Table 41. OTGFS electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	C_L ≤ 50 pF	4	20	ns
t_f	Fall Time (2)	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	295(1)	355	μA
f_{ADC}	ADC clock frequency		0.6	-	28	MHz
f_S(2)	Sampling rate		0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} tied to ground))	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 43* and *Table 45* for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	8.5	13	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.61			μs
		-	185			$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 80 MHz	-	-	71.4	μs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 ~ 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} can be internally connected to V_{DDA} whereas V_{REF-} is internally connected to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Table 43 and *Table 45* are used to define the maximum external impedance allowed for an error below 1 of LSB in 12-bit resolution.

Table 43. R_{AIN} max for f_{ADC} = 14 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (Ω)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1) Guaranteed by design.

Table 44. R_{AIN} max for f_{ADC} = 28 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (Ω)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

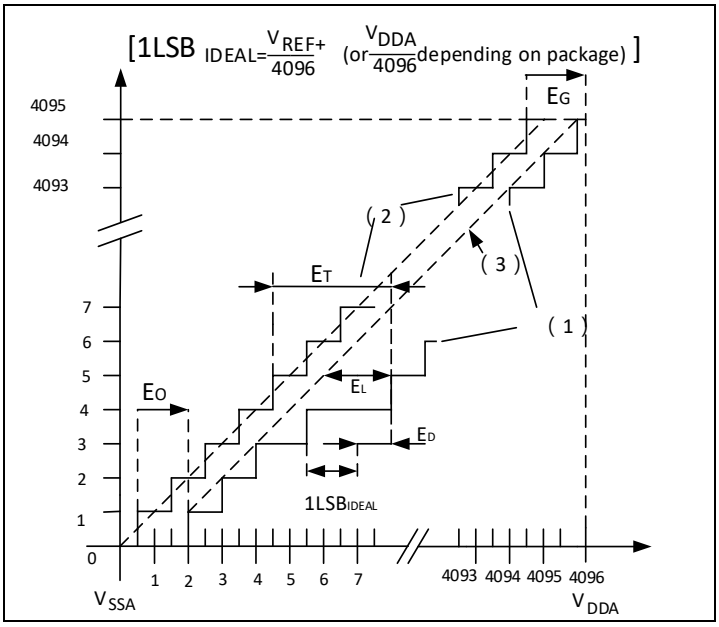
(1) Guaranteed by design.

Table 45. ADC accuracy(1)

Symbol	Parameter	Test Conditions	Typ(2)	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C	±1.5	±3	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		+1.5	-2/+2.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±1	±1.5	
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V	±2	±3	LSB
EO	Offset error		±1.5	±3	
EG	Gain error		+1.5	±2.5	
ED	Differential linearity error		±1	-1/+2	
EL	Integral linearity error		±1.5	±2.5	

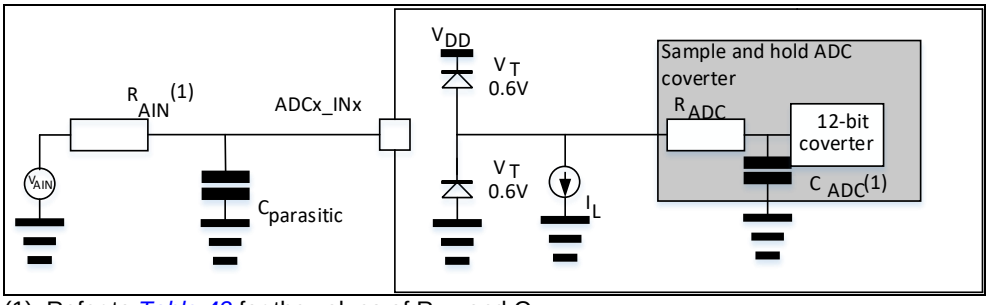
(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

Figure 26. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 27. Typical connection diagram using the ADC



(1) Refer to *Table 42* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9.* The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

If HEXT is enabled while ADC uses any input channel of ADC1_IN0~13, following PCB layout guide line below to isolate the high frequency interference from HEXT emitting to ADC input signals nearby.

- Use different PCB layers to route ADC_IN signal apart from HEXT path
- Do not route ADC_IN signals and HEXT path parallel

5.3.18 Internal reference voltage (V_{INTRV}) characteristics

Table 46. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}	Internal reference voltage	-	1.17	1.20	1.23	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Guaranteed by design, not tested in production.

6 Package information

6.1 LQFP64 – 10 x 10 mm

Figure 28. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

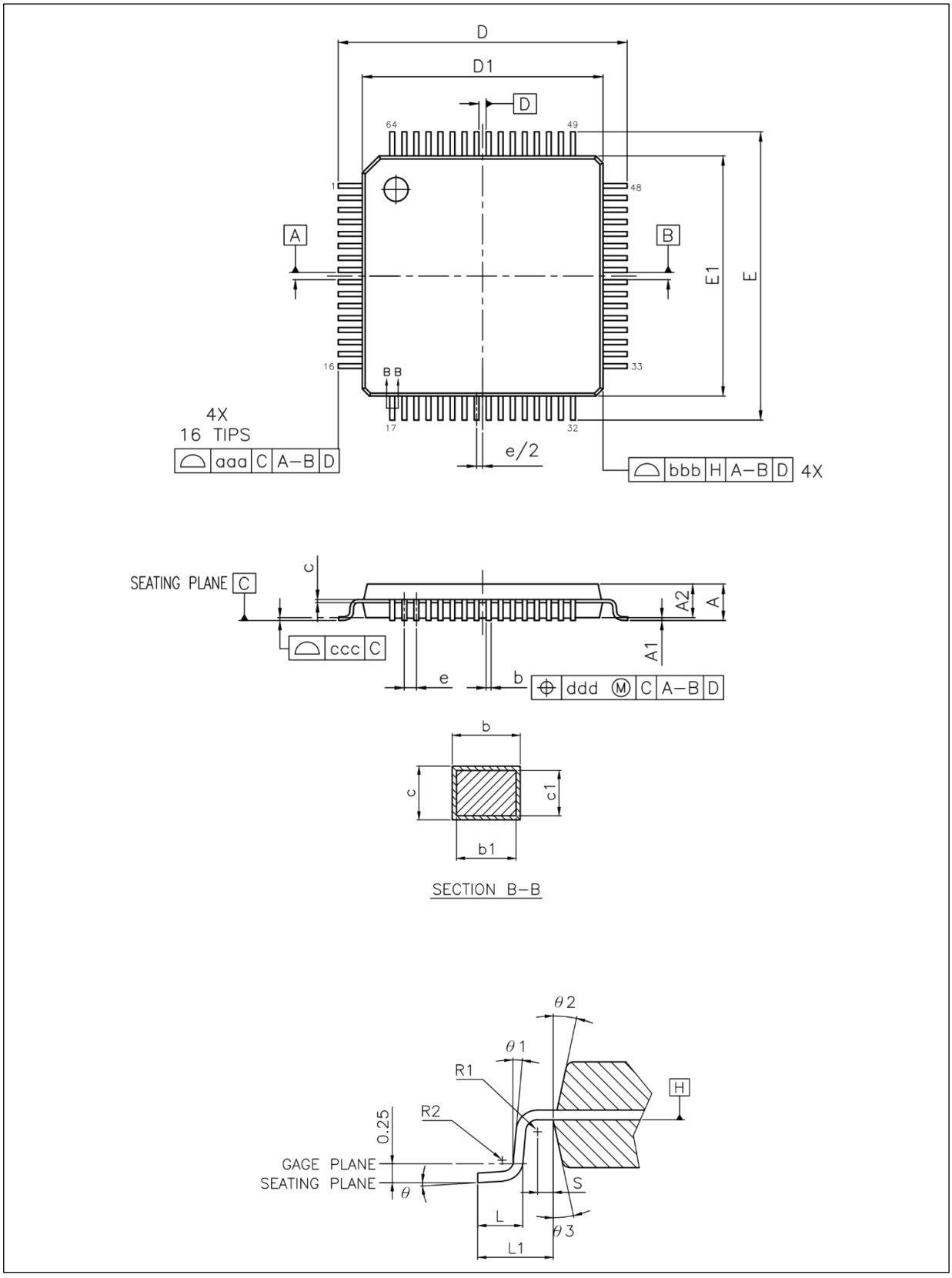


Table 47. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

6.2 LQFP64 – 7 x 7 mm

Figure 29. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package outline

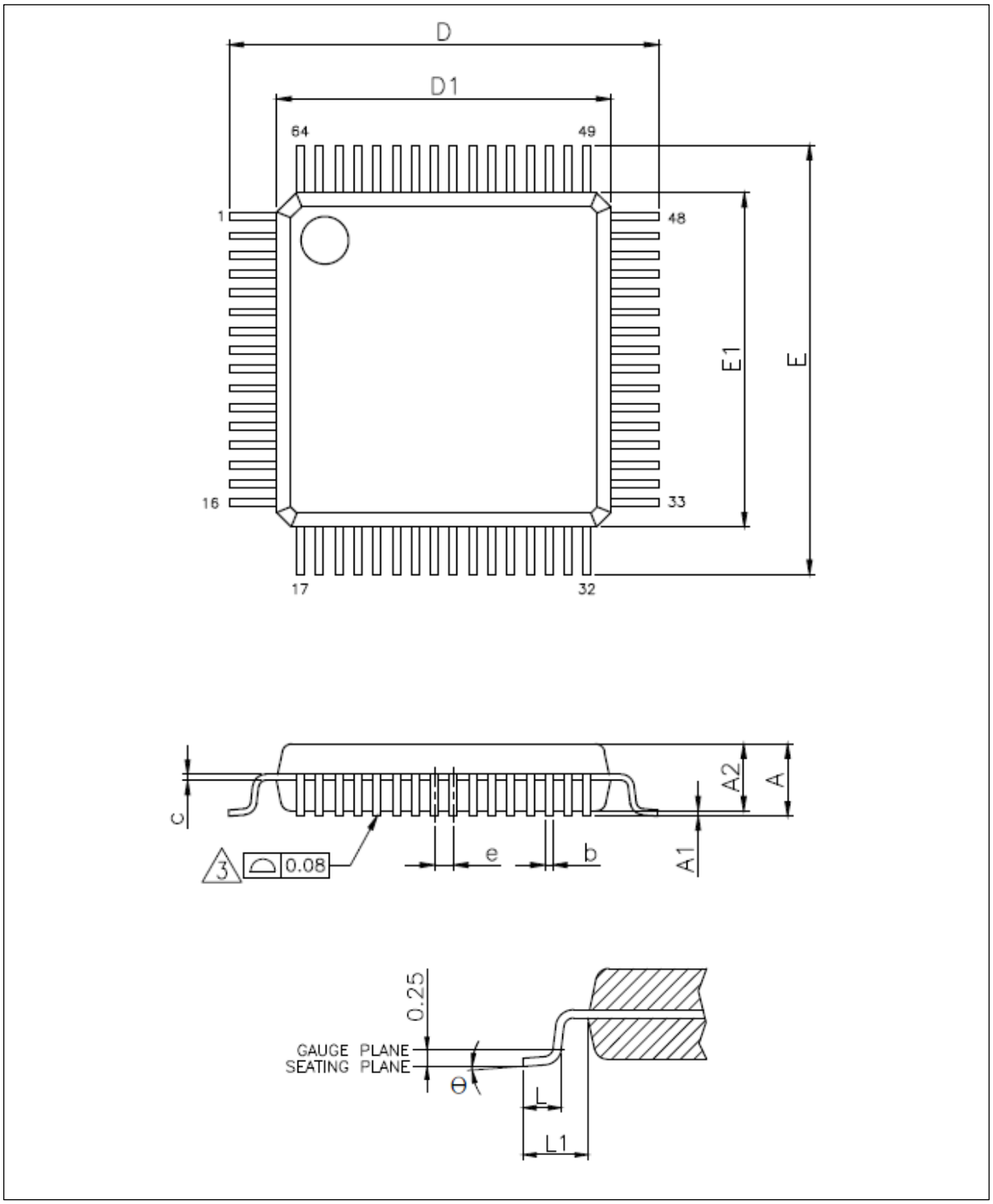


Table 48. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		
E1	7.00 BSC.		
e	0.40 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.3 LQFP48 – 7 x 7 mm

Figure 30. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

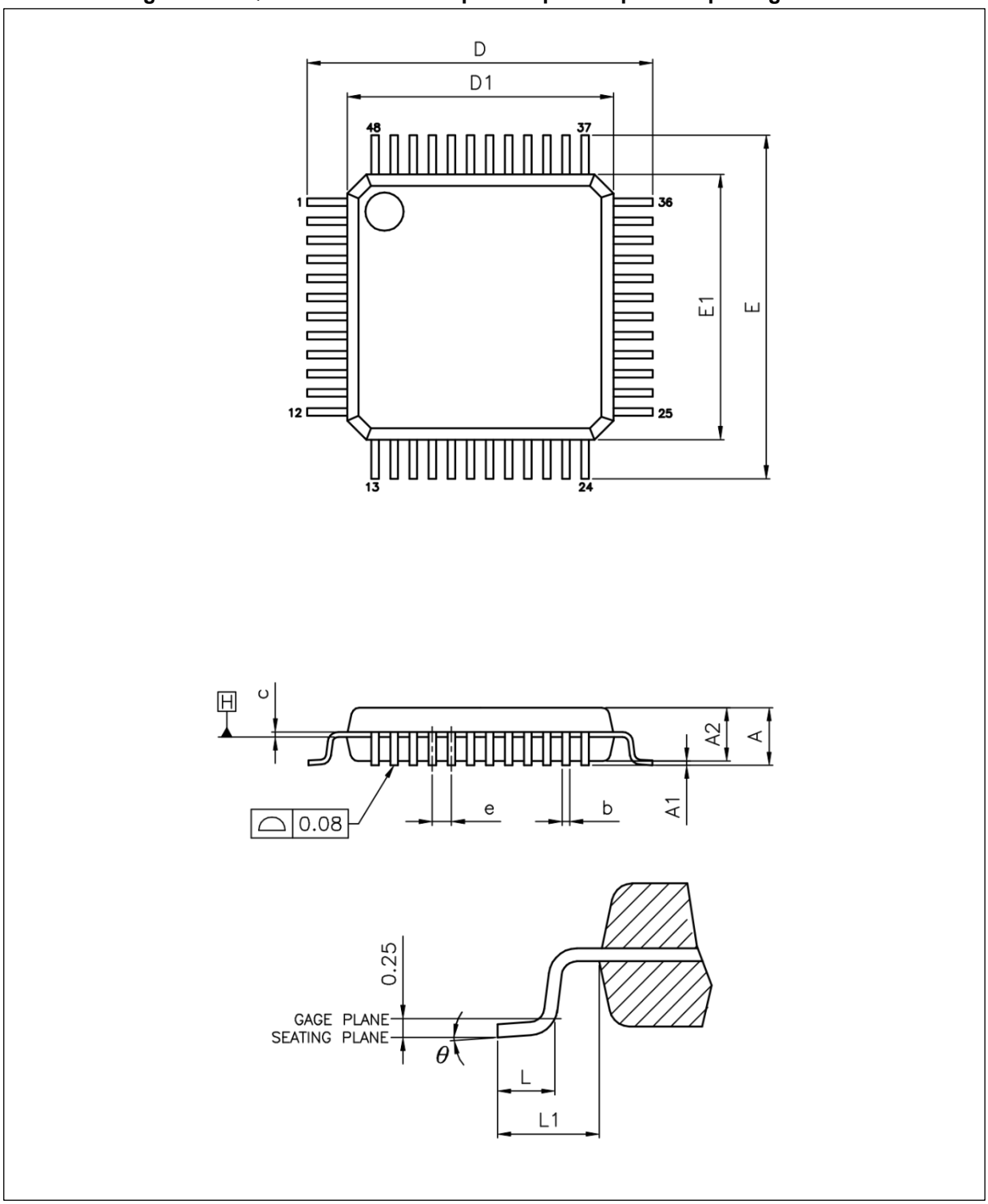


Table 49. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.4 QFN48 – 6 x 6 mm

Figure 31. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

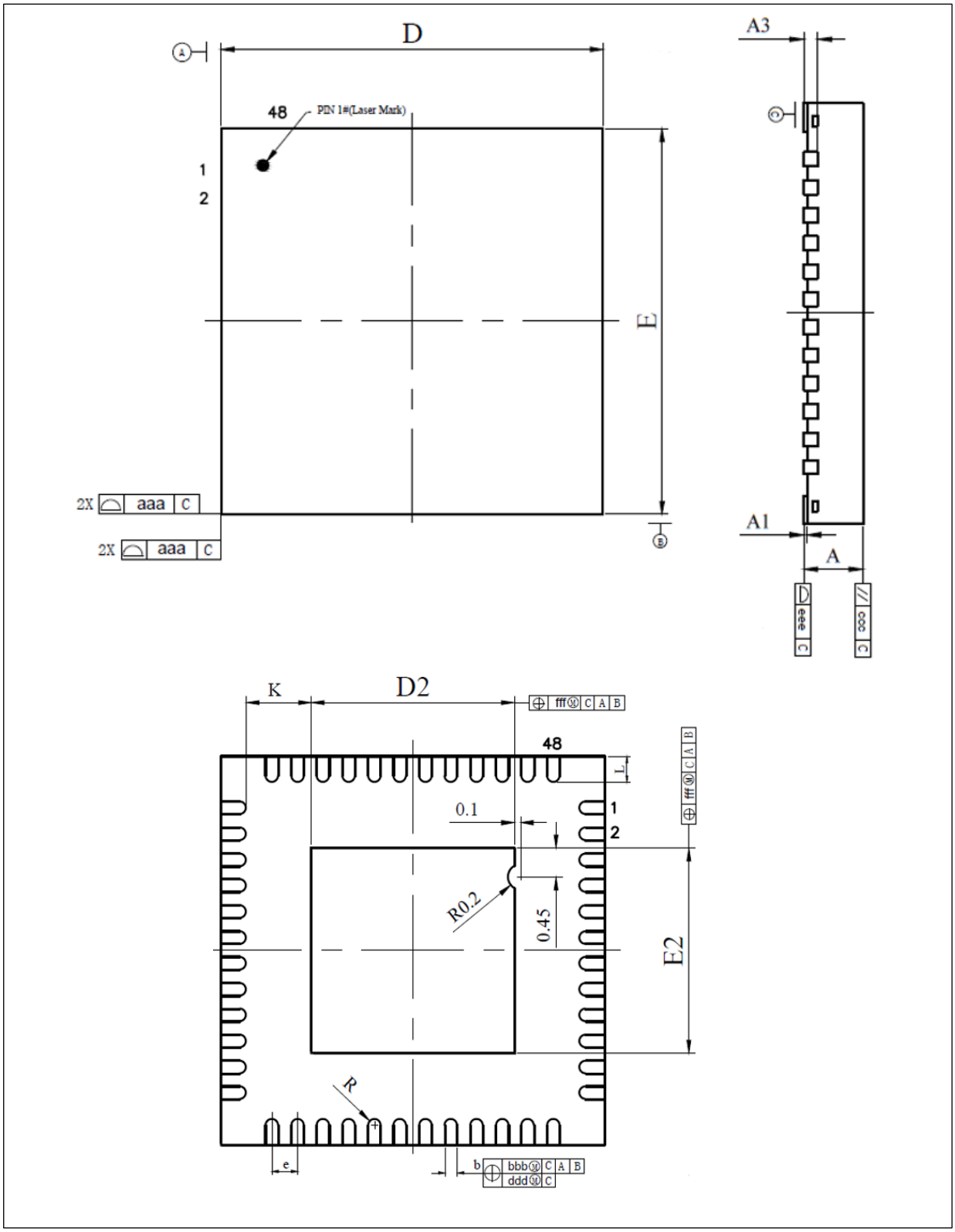


Table 50. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	3.07	3.17	3.27
E	5.90	6.00	6.10
E2	3.07	3.17	3.27
e		0.40 BSC.	
K	0.20	-	-
L	0.35	0.40	0.45

6.5 LQFP32 – 7 x 7 mm

Figure 32. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package outline

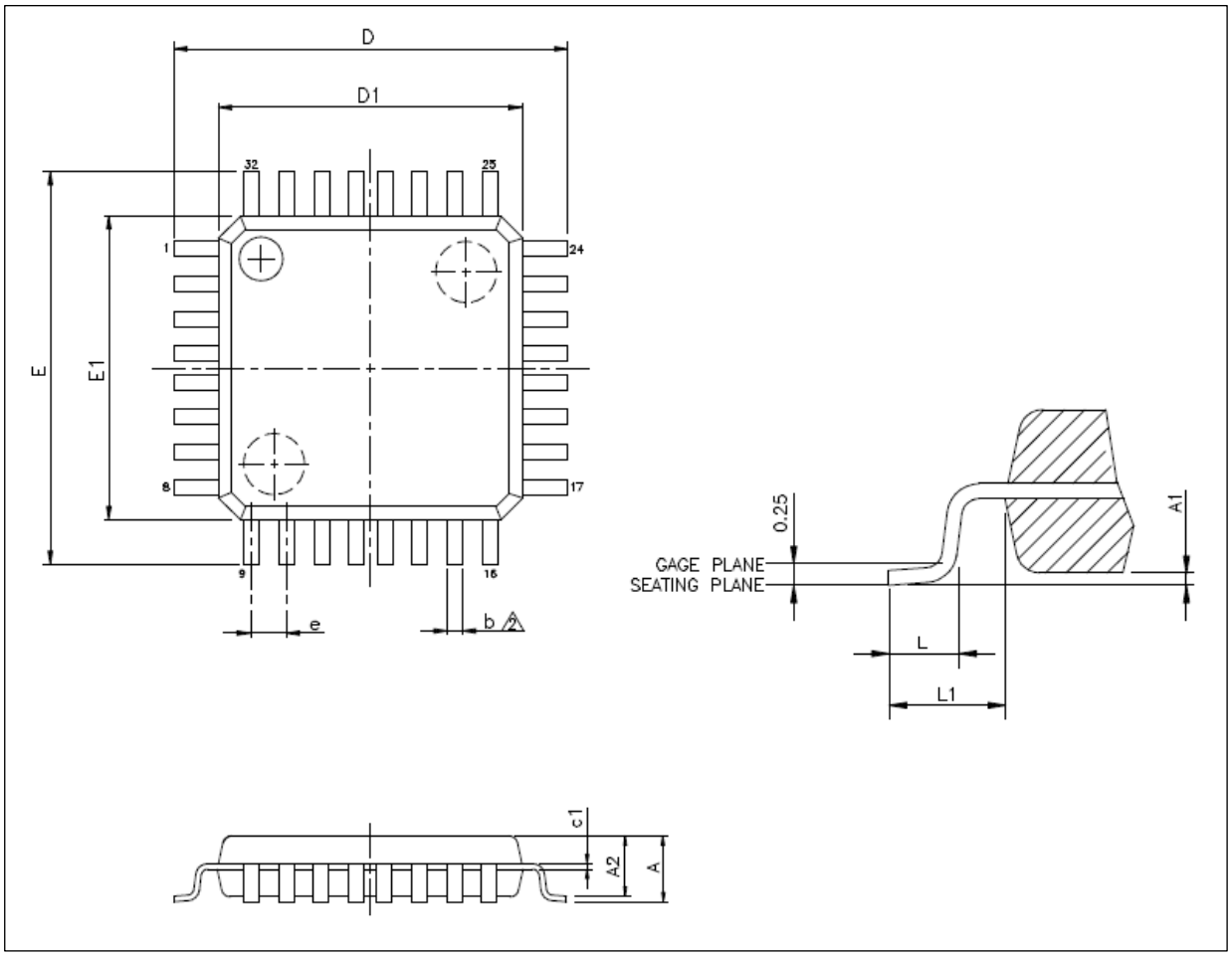


Table 51. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Min
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
b	0.30	-	0.45
c	0.09	-	0.16
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		
E1	7.00 BSC.		
e	0.80 BSC.		
L	0.45	-	0.75
L1	1.00 REF.		

6.6 QFN32 – 4 x 4 mm

Figure 33. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

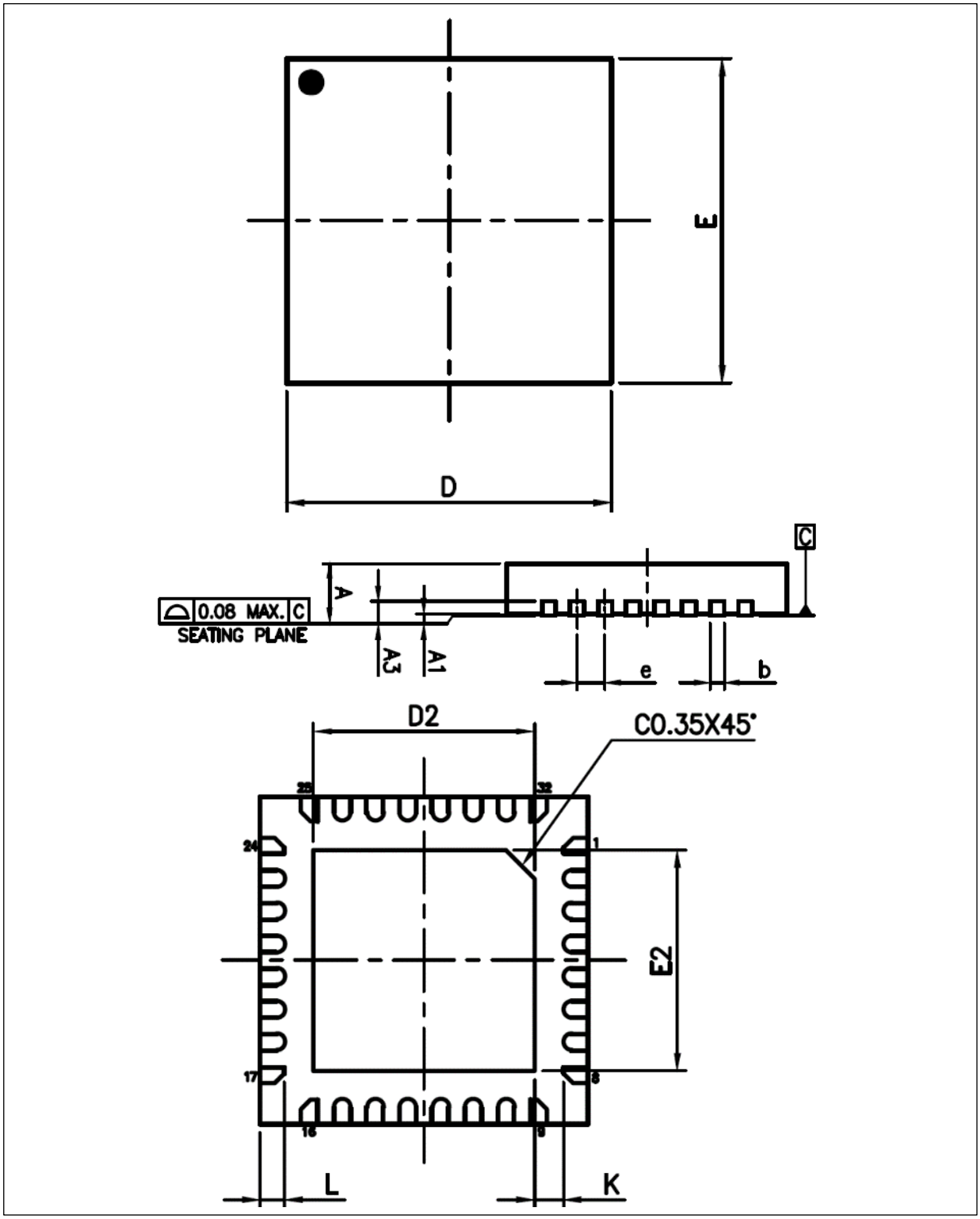


Table 52. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Min
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC.	
D2	2.65	2.70	2.75
E		4.00 BSC.	
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

6.7 TSSOP20 – 6.5 x 4.4 mm

Figure 34. TSSOP20 – 6.5 x 4.4 mm 20 pin thin shrink small package outline

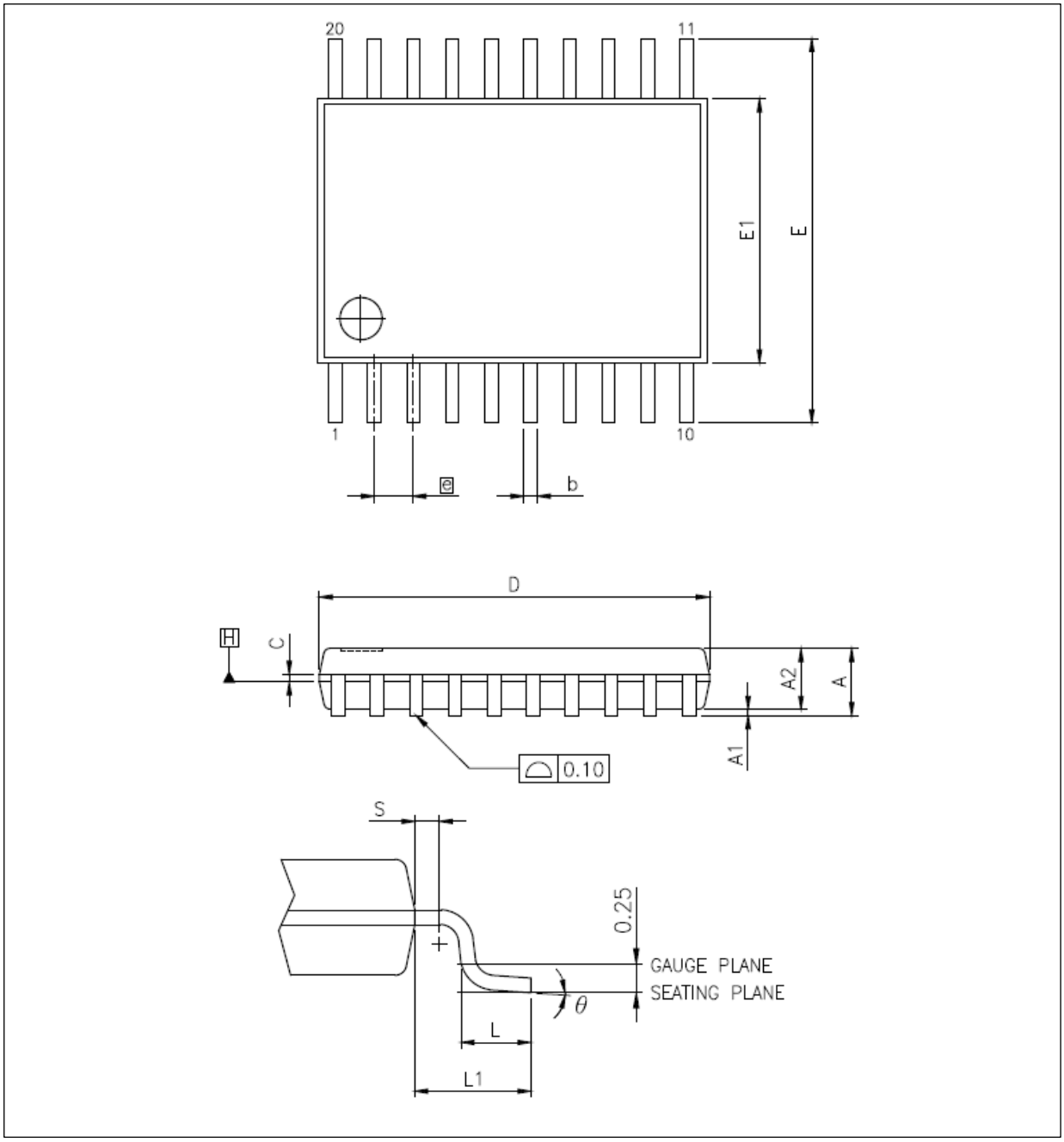


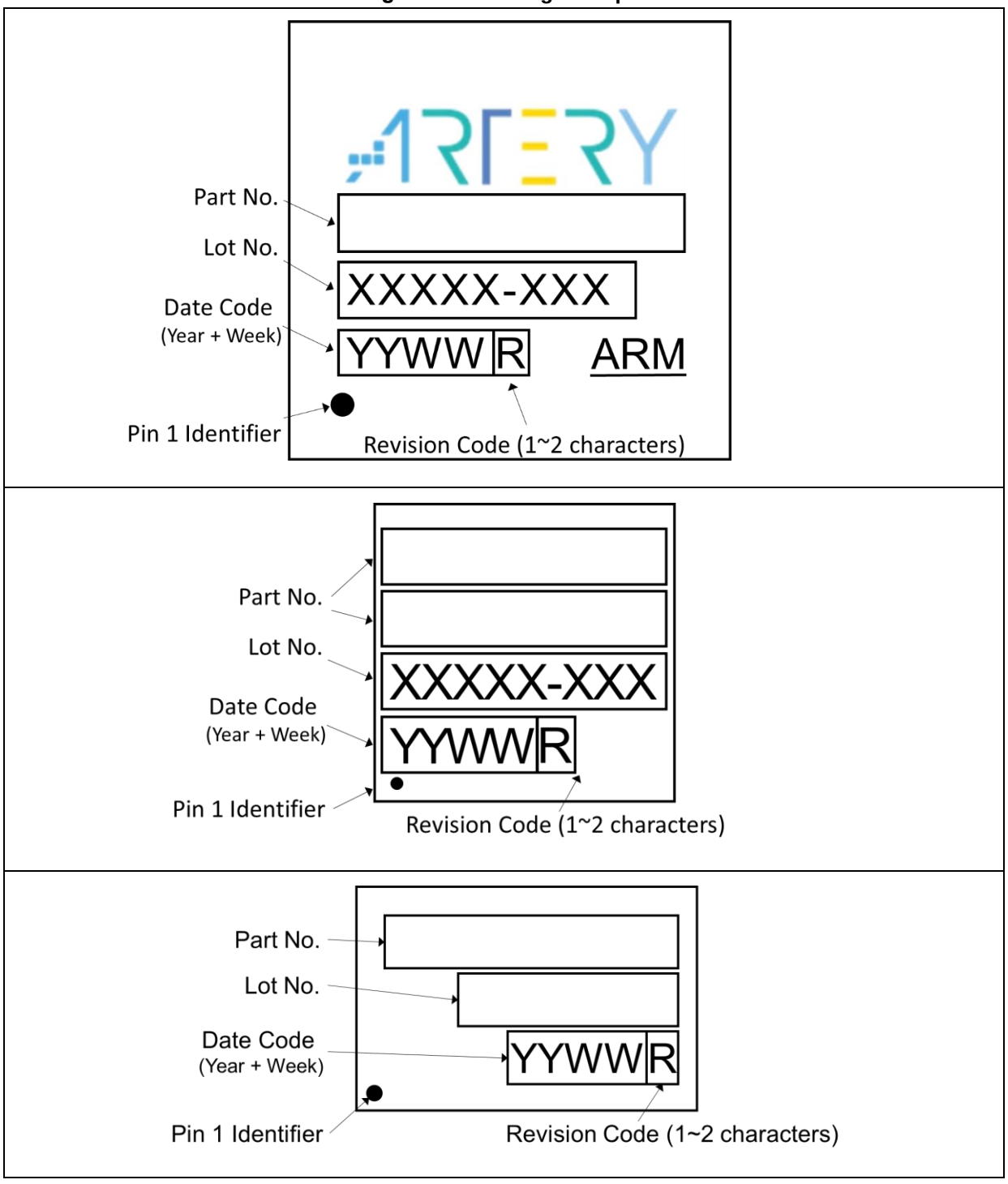
Table 53. TSSOP20 – 6.5 x 4.4 mm 20 pin thin shrink small package mechanical data

Symbol	Millimeters		
	Min	Typ	Min
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
C	0.09	-	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC.		
e	0.65 BSC.		
L1	1.00 REF.		
L	0.50	0.60	0.75
S	0.20	-	-
Θ	0°	-	8°

6.8 Device marking

Artery devices may have the following markings, depending on the types of packages.

Figure 35. Marking example



6.9 Thermal characteristics

The maximum chip junction temperature (T_j max) must never exceed the values given in *Table 8*. The maximum chip-junction temperature, T_j max, in degrees Celsius, may be calculated based on the following equation:

$$T_jmax = T_amax + (P_dmax \times \Theta_{JA})$$

Where:

- $T_a$max refers to the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_d$max is the sum of P_{INT}max and P_{GPIO}max ($P_d$max = P_{INT}max + P_{GPIO}max),
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{GPIO}max represents the maximum power dissipation on output pins where:

$$P_{GPIO}max = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the GPIOs at low and high level in the application.

Table 54. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 – 10 x 10 mm	82.5	°C/W
	Thermal resistance junction-ambient LQFP64 – 7 x 7 mm	85.1	
	Thermal resistance junction-ambient LQFP48 – 7 x 7 mm	85.1	
	Thermal resistance junction-ambient QFN48 – 6 x 6 mm	34.2	
	Thermal resistance junction-ambient LQFP32 – 7 x 7 mm	85.4	
	Thermal resistance junction-ambient QFN32 – 4 x 4 mm	54.0	
	Thermal resistance junction-ambient TSSOP20 – 6.5 x 4.4 mm	102.6	

7 Part numbering

Table 55. AT32F425 series part numbering

Examples: AT32 F 4 2 5 R 8 T 7 -7

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex™-M4

Product series

2 = Value line

Product application

5 = OTG series

Pin count

R = 64 pins

C = 48 pins

K = 32 pins

F = 20 pins

Internal Flash memory size

8 = 64 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package type

T = LQFP

U = QFN

P = TSSOP

Temperature range

7 = -40 °C to +105 °C

Package information

-7 = LQFP64 - 7 x 7 mm

-4 = QFN32 - 4 x 4 mm

None = other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

8 Document revision history

Table 56. Document revision history

Date	Version	Change
2021.12.10	2.00	Initial release

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