BL6552
Professional chip for three phase power monitoring and analysis
Data sheet

V1.1

table of Contents

1、 Product description

Bl6552 is a 7-channel three-phase power monitoring and analysis chip, which is suitable for three-phase intelligent circuit breaker, three-phase guide rail meter, electrical measuring instrument, power supply monitoring of high-power equipment and other applications, with high cost performance.

BL6552 integrates seven high-precision Sigma-Delta ADCs, reference voltage circuits, temperature sensors and other analog circuit modules, as well as digital signal processing circuits for processing electrical parameters such as power, effective value, energy, and temperature. It can be used to measure three-phase and The total (fundamental and harmonic) active power and energy, reactive power and energy, apparent power and energy of the combined phase; and fundamental active power and energy, reactive power and energy; and the effective value of current and voltage of each phase , Power factor and other parameters; with current loss monitoring, current and voltage peak detection, zero-crossing detection and other power quality management; it can give real-time waveforms.

bl6552 integrates spi and uart interfaces to facilitate the transfer of metering parameters and calibration parameters with external MCUs.

bl6552 internally uses data flow calculation methods to process various signals, and has good reliability in the case of external interference. The internal voltage monitoring circuit can ensure normal operation when power is turned on and off.

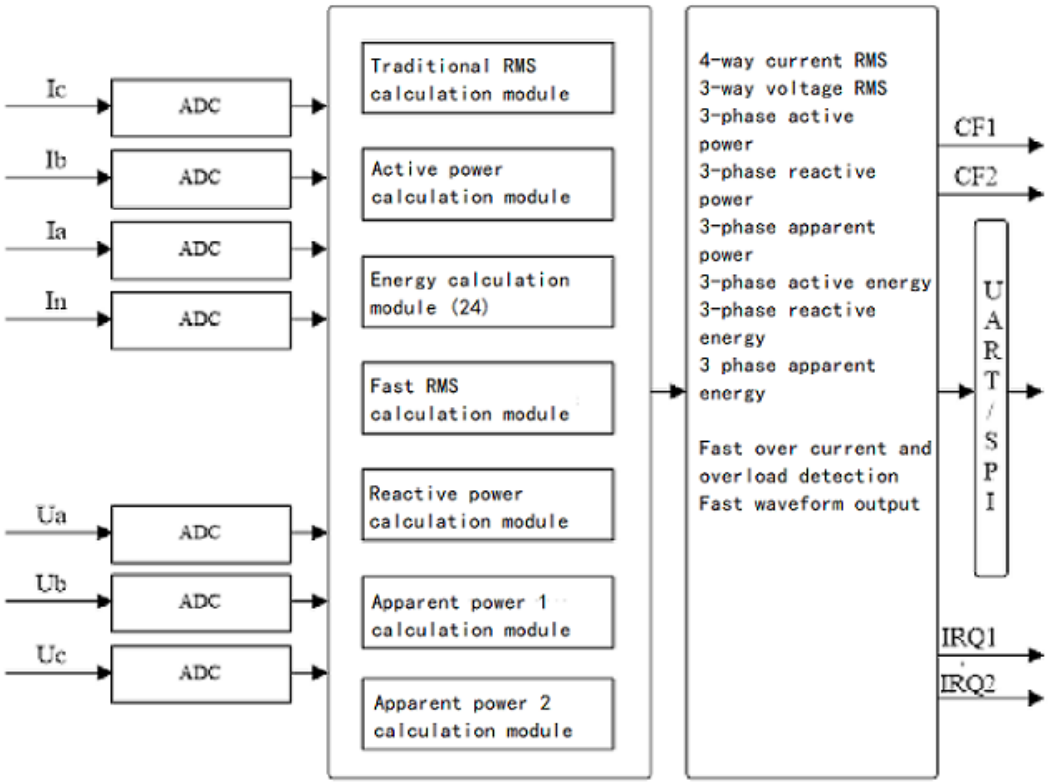
2、 Basic Features

2.1 main feature

- ✓ High precision, the non-linear error of active power within the input dynamic range of 8000:1 is less than 0.1%
- ✓ High stability, the output pulse signal bounces within the input dynamic range of 8000:1<0.02%@Ib
- ✓ Provide zero-line current input sampling
- ✓ Give each phase and total (fundamental and harmonic) active, reactive, and apparent power (24bit, support two calculation methods); and fundamental active and reactive power (24bit)
- ✓ Given the effective value of each phase voltage and current (24bit), the relative error within the detection range of 3000:1 is less than 0.1%
- ✓ Provide waveform sampling data of each phase voltage, current and neutral current (24bit)
- ✓ Give the total (fundamental and harmonic) active, reactive, and apparent energy (24bit)
- ✓ Give the total (fundamental and harmonic) active and reactive line period energy
- ✓ Give the total (fundamental and harmonic) positive and negative active energy
- ✓ Give the combined and four-quadrant reactive energy
- ✓ Gives 300 real-time waveforms per week
- ✓ Give power factor
- ✓ With fast effective value output
- ✓ Give voltage and current phase angle measurement
- ✓ Fast pulse output with active energy and reactive energy
- ✓ With voltage loss and phase failure detection function

- ✓ With current loss detection function
- ✓ With current and voltage peak detection and zero-crossing detection functions
- ✓ With frequency detection
- ✓ Programmable anti-creep threshold setting
- ✓ Programmable adjustment of pulse output frequency
- ✓ Programmable active power, reactive power, apparent power error and gain adjustment
- ✓ Programmable input active phase compensation
- ✓ The interrupt request signal can be given as needed to facilitate the control with the external MCU
- ✓ With uarttspi communication interface for easy data transmission
- ✓ Built-in 1.2v reference voltage source
- ✓ Single power supply 3.3v
- ✓ QFN36 PACKAGE

2.2 System Block Diagram



Three phase electric energy monitoring and analysis

It is mainly divided into analog signal processing and digital signal processing.The analog part mainly includes 7-channel high-precision Sigma-Delta ADC and related analog modules, and the digital part is a digital signal processor and related modules.

2.3 Pin arrangement

QFN36 PACKAGE

Serial number	name	input Output	description

1	INP	enter	Positive terminal input of neutral current channel
2	VREF	input Output	Reference voltage 1.2v
3	VAN	enter	A phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
4	VAP	enter	A phase voltage channel positive input
5	VBN	enter	B-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
6	VBP	enter	B-phase voltage channel positive terminal input
7	VCN	enter	C-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
8	VCP	enter	C-phase voltage channel positive terminal input
9	NRST	enter	Reset, active low
10	AGND	Power ground	Analog ground
11	DGND	Power ground	Digitally

12	_CS	enter	SPI CHIP SELECTION UART RATE SELECTION
13	SDO	Output	SPIIUART SEND TX
14	SDI	enter	SPIIUART RECEIVES RX
15	SCLK	enter	SPI CLOCK UART RATE SELECTION
16	_IRQ1	Output	Interrupt status logic output 1
17	_IRQ2	Output	Interrupt status logic output 2
18	CLKOUT	Output	Crystal pin
19	CLKIN	enter	Crystal oscillator pin, external crystal oscillator frequency 8MHz
20	VPP	power supply	Reserved, can be suspended
21	CF1	Output	Calibration pulse 1 (active power)
22	CF2	Output	Calibration pulse 2 (reactive power)
23	AT1	Output	Logic output pin, configurable output indication 1
24	AT2	Output	Logic output pin, configurable output indication 2

25	AT3	Output	Logic output pin, configurable output indication 3
26	DVDD18	Output	Digital module voltage 1.8V, external 0.1uF filter capacitor
27	SEL	enter	Default 0, select Uart; 1, select SPI
28	DVDD	power supply	Power 3.3v
29	AVDD	power supply	Power 3.3v
30	ICN	enter	C-phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
31	ICP	enter	C-phase current channel positive terminal input
32	IBN	enter	B-phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
33	IBP	enter	B-phase current channel positive terminal input
34	IAN	enter	A phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7v
35	IAP	enter	A phase current channel positive terminal input
36	INN	enter	The negative terminal input of the neutral current channel, the maximum differential voltage of each pair of pins is ±0.7v

2.4 Performance

2.4.1 Electrical parameter performance index

Parameter	Symbol	Test Condition	Measure Pin	Min	Typ	Max	Unit
Active power measurement error	$watt_{err}$	8000:1 input DR			0.1		%
Reactive power measurement error	var_{err}	8000:1 input DR			0.1		%
Phase angle between channels causes measurement errors (PF=0.8 CAPACITIVE) (PF=0.5 INDUCTIVE)	$pf08c_{err}$ $pf05l_{err}$	Phase lead 37° Phase lag 60°			0.1 0.1		% %
AC POWER SUPPLY SUPPRESSION (Change in output frequency range) DC POWER SUPPLY SUPPRESSION (Change in output frequency range)	ac_{psrr} dc_{psrr}	Current channel current input pin IP\IN@100mV, voltage channel input pin VP\VN=100mV,			0.01 0.1		% %
Voltage RMS measurement accuracy, relative error	$vrms_{err}$	3000:1 input DR			0.1		%
Current RMS measurement accuracy, relative error	$irms_{err}$	3000:1 input DR			0.1		%
Analog input Input level (peak) input resistance		Differential input		370	14	1000	mV kΩ kHz

Bandwidth (-3dB) Gain error Phase gain matching error		External 1.25 reference voltage External 1.25 reference voltage				4 3	% %
Internal voltage reference Baseline deviation Temperature Coefficient	Vref $Vref_{err}$ TempCoef				1.2 20		V mV ppm/℃
Logic input NRST, RXXSDI, SCLK,, CS Input high level Input low level		DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		 0.8	 V V
Logic output TXXSDO, CF1_WATT, CF2_VAR Output high level Output low level		DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		 1	 V V
power supply AVDD, DVDD DVDD18 AVDD DVDD	V_{avdd} V_{dvdd18} I_{avdd} I_{dvdd}	 DVDD18=1.8V AVDD=3.3 DVDD=3.3		3 1.6	3.3 1.8 6 6	3.6 2 9 9	V V mA mA

2.4.2 Limit range

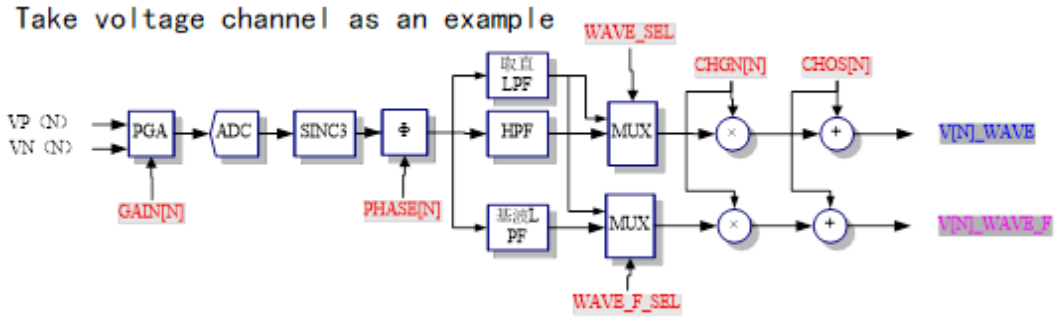
（T＝25 ℃）

project	symbol	extremum	unit
Power supply voltage vdd	AVDD, DVDD	-0.3 ~ +4	V
Power supply voltage dvdd18	DVDD18	-0.3 ~ +2.5	V
Programming voltage	VPP	-0.3 ~ +15	V
Analog input voltage (relative to gnd)	ICN, ICP, IBN, IBP, IAN, IAP, INN, INP, VCN, VCP, VBN, VBP, VAN, VAP	-1 ~ +AVDD	V
Analog output voltage (relative to gnd)	VREF	-0.3 ~ +AVDD	V

Digital input voltage (relative to gnd)	SEL, NRST, RXXSDI, SCLK,, CS, SEL	-0.3 ~ AVDD+0.3	V
Digital output voltage (relative to gnd)	CF_watt, CF_var, TXXSDO	-0.3 ~ AVDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstr	-55 ~ +150	℃
Power consumption (qfn36)	P	200	mW

3、 working principle

3.1 Principle of current and voltage waveform generation



A total of 7 high-precision ADCs, using double-ended differential signal input: channel N input signal VP[N] and VN[N]. 7 channels of waveform output, including 4 channels of current and 3 channels of voltage. In each channel (The current and voltage are the same), the input signal passes the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) to get 1bit PDM to the digital module, the digital module is phase-calibrated, down-sampling filter (SINC3), optional high-pass After the filter (HPF) or the fundamental low-pass filter, through the gain and offset correction modules, the required current waveform data and voltage waveform data (I(N)_WAVE, V(N)_WAVE) are obtained.

The 7-channel pga gain is adjustable (0000=1; 0001=2; 0010=8; 0011=16), see the gain register for adjustment.

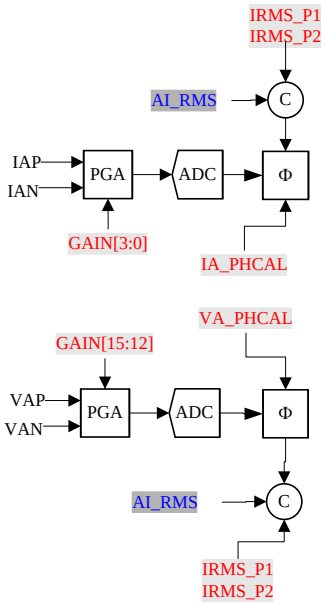
address	Name	Bit width	Defaults	description
60	GAIN1	24	0x000000	Channel pga gain adjustment register:

				[11:8]:C-PHASE CURRENT [15:12]:B PHASE CURRENT [19:16]:A PHASE CURRENT [23:20]:Neutral line current
61	GAIN2	20	0x00000	Channel pga gain adjustment register: [11:8]:A PHASE VOLTAGE [15:12]: PHASE B VOLTAGE [19:16]:C PHASE VOLTAGE

3.1.1 Active phase compensation

At the adc output position, a digital calibration method for small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Because this compensation must be timely, this This method is only suitable for small phase errors of <0.574 (range. Using time-shift technology to correct large phase errors will introduce significant phase errors in higher harmonics.

Since the transformer at the analog input terminal may have inconsistent angle differences when input signals of different amplitudes, increase the angle differential section compensation setting to allow three-section angle differential compensation.



Current channel angle differential segment definition register:

address	Name	Bit width	Defaults	description
62	IRMS_P1	24	0x010000	The angle difference segment point defines P1, which satisfies IRMSmin<P1<P2<IRMSmax
63	IRMS_P2	24	0x200000	The angle difference segment point defines P2, which satisfies IRMSmin<P1<P2<IRMSmax

The phase calibration register is a binary 24-bit register, and the data format of each register is as follows:

address	Name	Bit width	Defaults	description

64	IA_PHCAL	24	0x000000	A phase current channel angle difference correction register, when IRMSmin<effective value of input current<P1, [7:0] is the current channel phase used for correction, [7] is the enable bit, the minimum adjustment delay time is 250ns, corresponding to 0.0045 Degree 1LSB, the maximum adjustable is ±0.574 degrees). When P1<effective value of input current<P2, [15:8] is used to correct the current channel phase, [15] is the enable bit, and the adjustment accuracy is the same as above. When P2 <The effective value of input current<IRMSmax, [23:16] is the current channel phase used for correction, [23] is the enable bit, and the adjustment accuracy is the same as above.
65	IB_PHCAL	24	0x000000	B-phase current channel angle difference correction register (same as above)

66	IC_PHCAL	24	0x000000	C-phase current channel angle difference correction register (same as above)
67	VA_PHCAL	24	0x000000	Phase A voltage channel angle correction register, when IRMSmin<effective value of input current<P1, [7:0] is the voltage channel phase used for correction, [7] is the enable bit, the minimum adjustment delay time is 250ns, corresponding to 0.0045 Degree 1LSB, maximum adjustable ±0.574 degrees). When P1<effective value of input current<P2, [15:8] is used to correct the current channel phase, [15] is the enable bit, and the adjustment accuracy is the same as above. When P2 <The effective value of the input current<IRMSmax, [23:16] is used to correct the phase of the voltage channel, [23] is the enable bit, and the adjustment accuracy is the same as above.
68	VB_PHCAL	24	0x000000	B-phase voltage channel angle difference correction register (same as above)

69	VC_PHCAL	24	0x000000	C-phase voltage channel angle difference correction register (same as above)
90	IN_PHCAL	24	0x000000	IN phase current channel angle difference correction register, when IRMSmin<effective value of input current<P1, [7:0] is used to correct the current channel phase, [7] is the enable bit, the minimum adjustment delay time is 250ns, corresponding to 0.0045 Degree 1LSB, maximum adjustable ±0.574 degrees). When IRMSmin<effective value of input current<P1, [7:0] is used to correct the current channel phase, [7] is the enable bit, and the minimum adjustment delay time is 280ns , Corresponding to 0.005 degrees 1LSB, the maximum adjustable is ±0.625 degrees). When P1<effective value of input current<P2, [15:8] is used to correct the phase of the current channel, [15] is the enable bit, and the adjustment accuracy is the same as

				above .When P2<effective value of input current<IRMSmax, [23:16] is used to correct the current channel phase, [23] is the enable bit, and the adjustment accuracy is the same as above.

3.1.2 Channel offset correction

Contains 7 16-bit channel offset calibration registers CHOS[N], the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel. The deviation here may be caused by the input and the offset generated by the analog-to-digital conversion circuit itself. The deviation correction can be used in no load In this case, the waveform offset is 0.

address	Name	Bit width	Defaults	description
AC	IC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement

AE	IA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B2	VA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B3	VB_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B4	VC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement

These registers are used for channel deviation calibration

Correction formula:

$$WAVE[N] = WAVE0[N] + CHOS[N] * 2$$

Among them, wave0[n] is the measured value of the nth channel, chos[n] is the calibration value, and wave[n] is the output value after calibration.

3.1.3 Channel gain correction

Contains 7 16-bit channel gain calibration registers CHGN[N], the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use 2's complement data to adjust the gain error caused by the analog-to-digital conversion of the current channel and the voltage channel. The error here may be caused by the input and the analog-to-digital conversion circuit itself. The gain correction can be made in the range of ±50% Internal adjustment.

address	Name	Bit width	Defaults	description
A1	IC_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A2	IB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A3	IA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A7	VA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement

These registers are used for channel gain calibration.

Correction formula:

$$WAVE[N] = WAVE0[N] * (1 + \frac{CHGN[N]}{2^{16}})$$

Among them, wave0[n] is the measured value of the nth channel, chgn[n] is the gain calibration value, and wave[n] is the calibration output value.

3.1.4 Current and voltage waveform output

The current load current and voltage waveform data can be collected, the sampling current and voltage are updated at a rate of 15.6ksps, and 300 points can be sampled per cycle. Each sampled data is a 24bit signed number and stored in the waveform register (I(N)_WAVE) , V[N]_WAVE).The SPI rate is greater than 1.5Mbps, and the waveform values of multiple channels can be read continuously.

The channel can be selected through hpf and fundamental lpf, and finally a 7-channel waveform is obtained.

address	Name	Bit width	Defaults	description
2	IC_WAVE	24	0x000000	C-PHASE CURRENT WAVEFORM REGISTER
3	IB_WAVE	24	0x000000	Phase b current waveform register
4	IA_WAVE	24	0x000000	Phase a current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	Phase a voltage waveform register
9	VB_WAVE	24	0x000000	Phase b voltage waveform register

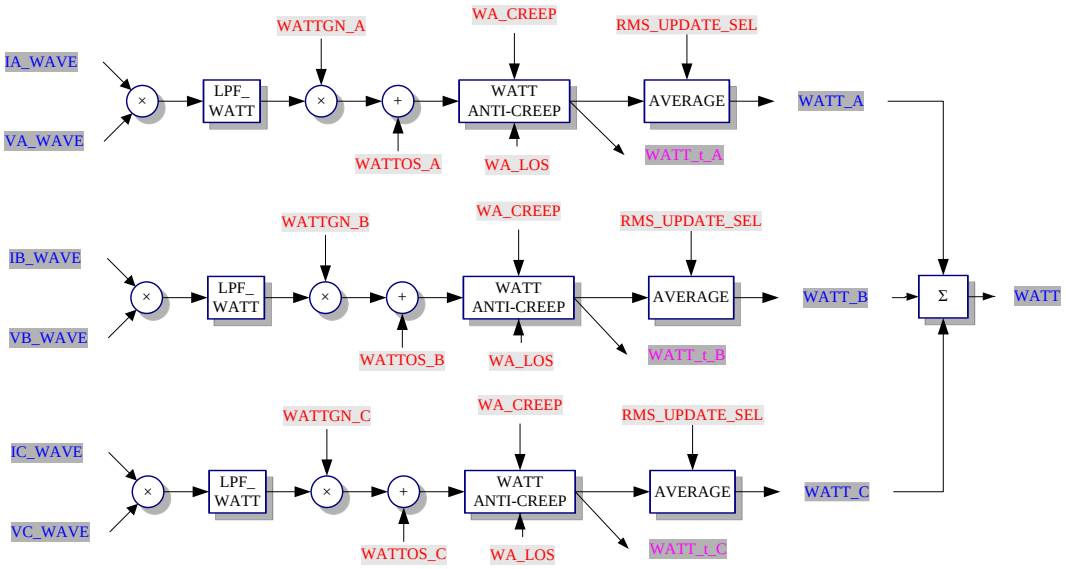
A	VC_WAVE	24	0x000000	C-phase voltage waveform register

The waveform is divided into full wave and fundamental wave. Through hpf, the AC measurement mode is used to output the full wave waveform. The fundamental wave lpf is the fundamental wave measurement mode and the fundamental wave waveform is output.

The waveform output selection is fixed, and it is set by the user mode register mode1[23].

0x96	MODE1	Working mode register	
No.	name	default value	description
[23]	WAVE_REG_SEL	1'b0	Current wave waveform register output selection, default 0 selects the waveform of the normal current channel, and 1 selects the waveform output of the leakage channel

3.2 Principle of active power calculation



The three-phase current and voltage waveforms are respectively subjected to digital multiplication, and then through low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order to obtain the split-phase power signal, which is added to obtain the total active power.

3.2.1 Active power output

The corresponding 3-phase current is multiplied by the 3-phase voltage to obtain the 3-phase power signal, which is added to obtain the total power.

address	Name	Bit width	Defaults	description
22	WATT_A	24	0x000000	A-phase active power register (full wave and fundamental wave optional)
23	WATT_B	24	0x000000	B-phase active power register (full wave and fundamental wave optional)

24	WATT_C	24	0x000000	C-phase active power register (full wave and fundamental wave optional)
25	WATT	24	0x000000	Combined active power register (full wave and fundamental wave optional)

Active power calculation formula: $\mathrm{WATT} = \frac{994*\mathrm{I_N(A)}*\mathrm{V(V)}}{\mathrm{Vref^2}} = \frac{994*\mathrm{P0}}{\mathrm{Vref^2}}$

among them,$\mathrm{I_N(A)}$, $\mathrm{V(V)}$Is the effective value input by the channel pin, P0 is the actual power of the applied load, vref is the built-in reference voltage, the typical value is 1.2V. The value 994 is the coefficient (determined by the actual test, the batch is consistent).

It can be set by the add_sel register, and the power sum is absolute value addition or algebraic sum addition.

0x98	MODE3	Working mode register	
No.	name	default value	description
[8]	add_sel	1'b0	watt and var conjoint sum addition method: 0-absolute value addition, |a|+|b|+|c|; 1-algebraic sum addition, a+b+c

3.2.2 Active power calibration

Contains three 16-bit active power offset correction registers WATTOS_AABBC and three 16-bit active power gain correction registers WATTGN_AABBC, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

Wattos is used to eliminate the DC deviation in the active power calculation, and wattgn is used to eliminate the gain deviation in the active power calculation. The deviation here may be caused by the crosstalk between the two channels generated on the PCB board and the integrated circuit itself in the power calculation. , It may also be the gain deviation of the adc channel itself.

Deviation correction can make the value in the active power register close to 0 under no load.

address	Name	Bit width	Defaults	description
B6	WATTGN_A	16	0x0000	Corresponding channel active power gain adjustment register, complement
B7	WATTGN_B	16	0x0000	Corresponding channel active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	Corresponding channel active power gain adjustment register, complement

C2	WATTOS_A	16	0x0000	Corresponding channel active power bias adjustment register, complement
C3	WATTOS_B	16	0x0000	Corresponding channel active power bias adjustment register, complement
C4	WATTOS_C	16	0x0000	Corresponding channel active power bias adjustment register, complement

Correction result of active power:

WATT=WATT0*(1+WATTGN/2^16) + WATTOS/2

Where watt is the active power after the nth phase is corrected, and watt0 is the active power before the nth phase is corrected.

3.2.3 Active power anti-creeping

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

The active anti-creep threshold register (WA_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, the output The active power is set to zero. This can make the value output to the active power register 0 under no-load conditions, even if there is a small noise signal.

address	Name	Bit width	Defaults	description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] is the reactive anti-creeping power threshold register [11:0] is the active anti-creeping power threshold register

$$Corresponding\ to\ CREEP\ value\ = \frac{Corresponding\ power\ register\ value}{2}$$

You can set wa_creep according to the watt value of the power register, and their corresponding relationship.The anti-submarine value generally takes 20 parts per million of the power full scale.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

The total active anti-creep threshold register (WA_CREEP2) is a 12bit unsigned number and the default is 00H. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, The output active power is set to zero. This is used to prevent creeping of the power sum.

address	Name	Bit width	Defaults	description
89	VAR_CREEP2/ WA_CREEP2	24	0x000000	[23:12] IS THE TOTAL REACTIVE ANTI-CREEPING POWER THRESHOLD REGISTER VAR_CREEP2; [11:0] THE TOTAL

				ACTIVE ANTI-CREEPING THRESHOLD REGISTER WA_CREEP 2

3.2.4 Active power small signal compensation

For the calculation of active power, in order to reduce the noise error in the small signal section, the small signal compensation register can be passed to the small signal compensation register to adjust the nonlinear error of the small signal section.

address	Name	Bit width	Defaults	description
82	WA_LOS_A	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.
83	WA_LOS_B	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.
84	WA_LOS_C	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.

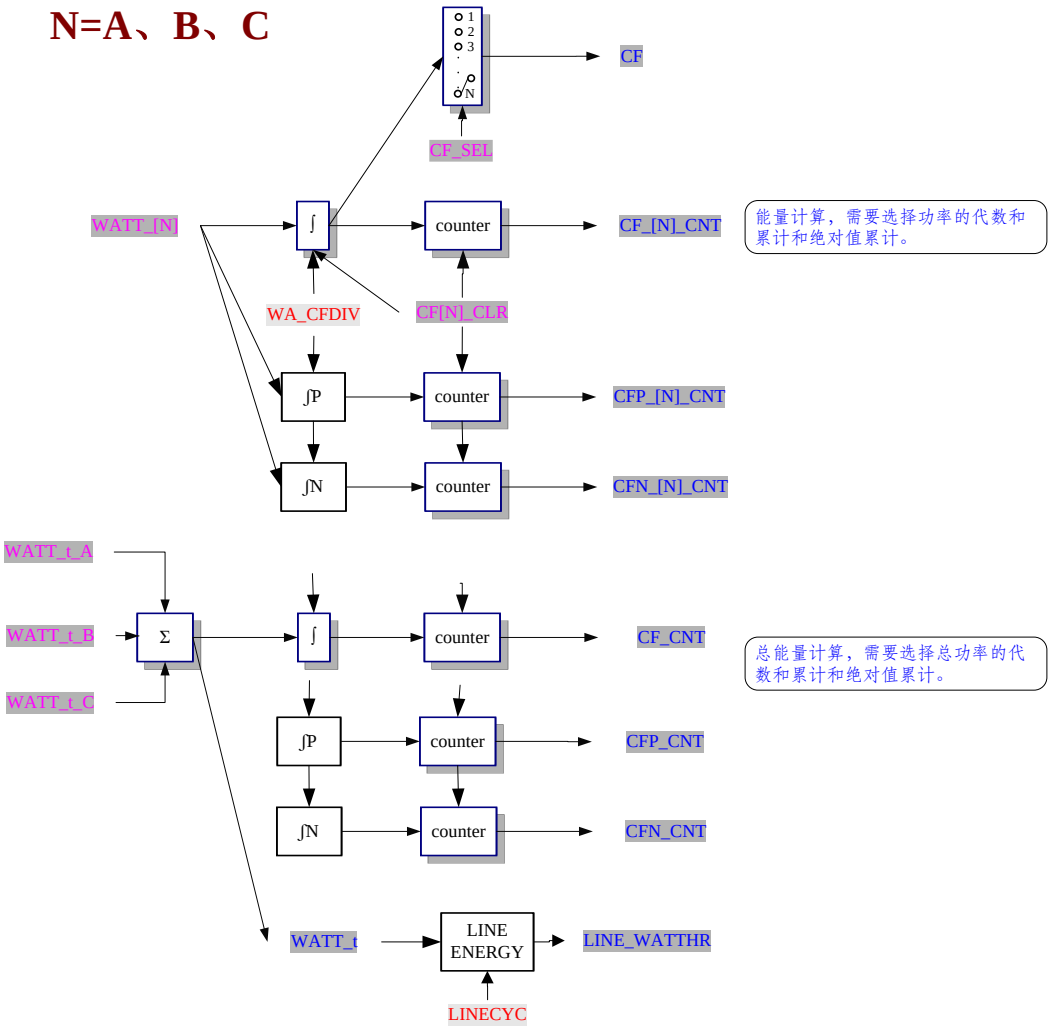
3.2.5 Active power selection

Active power calculation method, you can select fundamental active power or full-wave active power through watt_sel, the default is full-wave active power, you can select 7 channels separately:

0x98	MODE3	Working mode register	
No.	name	default value	description

[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave, 1-fundamental wave

3.3 Functional energy measurement principle



Provides three-phase energy pulse accumulation. The principle is that the active power of each phase is integrated for a period of time to obtain the functional energy during this period, and the energy is further converted into the corresponding frequency check pulse cf. The more electricity is used, the cf frequency is faster. The cf frequency is

slow when the power is low. The accumulation of functional quantities includes positive power accumulation, negative power accumulation, algebra and accumulation.

3.3.1 Functional output

Counting cf pulses can obtain energy (power consumption), which is stored in the nth phase energy accumulation register cf(n)_cnt and total energy register cf_cnt, as shown in the following figure.

address	Name	Bit width	Defaults	description
2F	CF_A_CNT	24	0x000000	Phase a active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B-phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C-PHASE ACTIVE PULSE COUNT, UNSIGNED
32	CF_CNT	24	0x000000	Conjunction active pulse count, no sign
33	CFP_A_CNT	24	0x000000	Phase a positive active pulse count, no sign
34	CFP_B_CNT	24	0x000000	B-phase positive active pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C-PHASE POSITIVE ACTIVE PULSE COUNT, UNSIGNED
36	CFP_CNT	24	0x000000	Conjunction positive active pulse count, no sign

37	CFN_A_CNT	24	0x000000	Phase a negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B-phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C-PHASE NEGATIVE ACTIVE PULSE COUNT, UNSIGNED
3A	CFN_CNT	24	0x000000	Conjunction negative active pulse count, unsigned

3.3.2 Function output selection

0x98	MODE3	Working mode register	
No.	name	default value	description
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable
[13:10]	CF_SEL	4'b0000	Channel cf_watt, cf_var output selection, The default is 0000, turn off cf_watt, cf_var; 0001, the power CF of watt_aavar_a; 0010, the power CF of watt_bbvar_b; 0011, power CF of watt_ccvar_c; 0100, power CF of watttvar; 0101, watt_p_aavar1 power CF; 0110, watt_p_bbvar2 power CF; 0111, power CF of watt_p_ccvar3; 1000, power CF of watt_ppvar4; 1001, watt_n_aava_a power CF; 1010, watt_n_va_b power CF; 1011,watt_n_ccva_c power CF; 1100,watt_nnva power CF 1101, (SAME AS 0100); 1110, APPARENT POWER CF; 1111, CLOSE CF;

[15]	cf_add_sel	1'b0	Watt and var energy addition methods: 0-absolute value addition; 1-algebraic sum addition (separation and combination)

First set mode3[9]=1 to select cf pin to output electric energy pulse, and then set cf_sel to choose how to output electric energy pulse.

CF_add_sel is used to set how the total energy is added, the algebraic sum or absolute value of each phase is added.

The counting results of CF pulses are stored in the CF*_*_CNT registers. The number of pulses can also be directly counted from the CF pin through the IIO interrupt. When the cycle of CF is less than 180ms, it is a pulse with a 50% duty cycle, which is greater than When equal to 180ms, the fixed pulse width is 90ms.

The power conversion formula corresponding to 1 cf:

Ecf= 58.6058574* $T_0 * Vref^2$(KWh)

Where T0 is the sampling interval, the typical value is 2 microseconds, VrefIs the reference voltage, the typical value is 1.2v.

3.3.3 Function output ratio

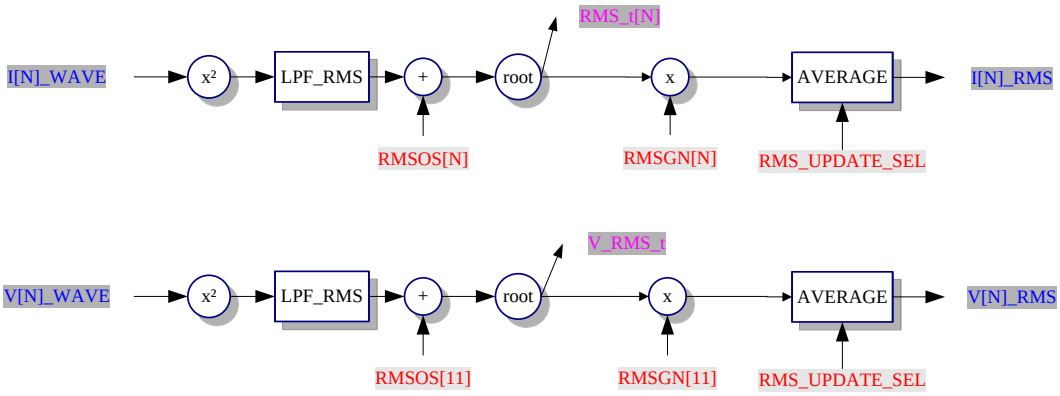
In the energy accumulation, the speed of energy accumulation can be set through the cf_div register, each file is 2 times the relationship, a total of 12 files.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

address	Name	Bit width	Defaults	description
CE	CFDIV	12	0x010	Active cf scaling register [11:0]

3.4 The calculation principle of the effective value of current and voltage

The calculation principle of the effective value of the channel, as shown below



The original waveform of each channel passes through the square circuit (X^2), the effective value low-pass filter (LPF_RMS), and the root circuit (ROOT) to obtain the instantaneous value RMS_t of the effective value, and then average the average value of each channel The values I[N]RMS and V_RMS.

3.4.1 Effective value output

The effective value calculation result is output and sum to 7 registers.

address	Name	Bit width	Defaults	description

D	IC_RMS	24	0x000000	C-phase current effective value register, unsigned
E	IB_RMS	24	0x000000	Phase b current RMS register, unsigned
F	IA_RMS	24	0x000000	Phase a current effective value register, unsigned
10	IN_RMS	24	0x000000	Zero wire current RMS register, unsigned
13	VA_RMS	24	0x000000	Phase a voltage effective value register, unsigned
14	VB_RMS	24	0x000000	Phase b voltage effective value register, unsigned
15	VC_RMS	24	0x000000	C-phase voltage effective value register, unsigned

When the channel is in the anti-submarine state, the effective value of the channel is not measured.

Current RMS conversion formula: $i\_rms = \frac{315021*I(A)}{Vref}$

Voltage RMS conversion formula: $v\_rms = \frac{20194*V(V)}{Vref}$

Vref is the reference voltage, and the typical value is 1.2V.

3.4.2 Setting of effective value input signal

Set MODE2[21:0].WAVE_RMS_SEL to select the effective value to calculate the input waveform. Each channel can be selected by two bits, 00-high pass, 01-select fundamental wave, 11-select sinc for direct output.

0x97	MODE2	Working mode register	
No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection, 00-high pass, 01-select fundamental wave, 11-select sinc output [3,2]: C PHASE CURRENT [5,4]: B-PHASE CURRENT [7,6]: Phase a current [9:8]: Neutral line current [15,14]: PHASE A VOLTAGE [17,16]: PHASE B VOLTAGE [19,18]:C-PHASE VOLTAGE

3.4.3 Valid value refresh rate setting

Set MODE2[22].RMS_UPDATE_SEL, you can choose the effective value average refresh time is 525ms or 1050ms, the default is 500ms.

0x97	MODE2	Working mode register

No.	name	default value	description
[22]	RMS_UPDATE_SEL	1'b0	Slow effective value register update speed selection, 1 is 1050ms, 0 is 525ms, and the default selection is 525ms;

3.4.4 Current and voltage RMS calibration

Contains 7 24-bit effective value offset correction registers RMSOS[N] and 7 16-bit effective value gain correction registers RMSGN[N], the default value is 0x0000.

They use the data in the form of 2's complement to calibrate the deviation in the effective value calculation. This deviation may come from input noise, because there is a step of square operation in the effective value calculation, which may introduce a DC offset caused by noise. Gain and offset correction can make the value in the effective value register close to 0 under no load.

address	Name	Bit width	Defaults	description
6D	IC_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
6E	IB_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
6F	IA_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register

70	IN_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
73	VA_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
74	VB_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
75	VC_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
78	IC_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
79	IB_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7A	IA_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7B	IN_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7E	VA_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7F	VB_RMSOS	24	0x000000	Corresponding channel effective value offset correction register

80	VC_RMSOS	24	0x000000	Corresponding channel effective value offset correction register

Calibration formula:

$$RMS[N] = \sqrt{RMS[N]_0^{\,2} + RMSOS[N] \times 256}$$

Here rms[n]0 is the effective value of the nth channel before correction, and rms[n] is the effective value of the nth channel after correction.

3.4.5 Effective value of anti-creeping

It has a patented effective value anti-submarine function to ensure that the effective value output is 0 when there is no current input.

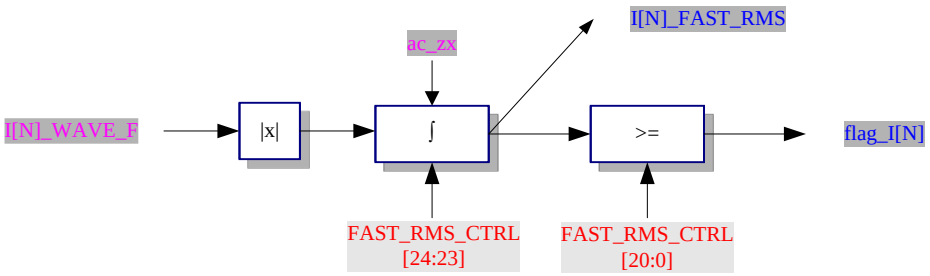
The effective value anti-creep threshold register (RMS_CREEP) is a 12bit unsigned number, and the default is 0x200. This value is internally expanded by 1 and compared with the absolute value of the input effective value signal. When the input effective value signal is less than this value, the output is valid The value is set to zero. This can make the value output to the effective value register 0 under no load, even if there is a small noise signal.

address	Name	Bit width	Defaults	description
8A	REVP_CREEP/ RMS_CREEP	24	0x04C200	[23:12] is the reverse indication threshold register REVP_CREEP (internal times 2^5, the value is equal to

				0.2% Ib, the maximum FFF is equal to 8% Ib); [11:0] is the effective value small signal threshold register RMS_CREEP, including zero Line (after internal times 2^2, the value is equal to 540, and the maximum FFF is equal to 16380);

3.5 Principle of overcurrent detection

The principle of fast effective value calculation is shown in the figure below.



7 channels have fast effective value registers, which can detect half cycle or cycle effective value. This function can be used for overcurrent detection.

The input waveform is obtained by taking the absolute value and then integrating within the specified time to obtain a fast effective value. This value can be compared with a preset threshold, and a flag can be given if it exceeds.

3.5.1 Fast effective value output

The 7-channel fast effective value output register is shown in the figure below

address	Name	Bit width	Defaults	description
18	IC_FAST_RMS	24	0x000000	C-phase current fast effective value register, unsigned
19	IB_FAST_RMS	24	0x000000	B-phase current fast effective value register, unsigned
1A	IA_FAST_RMS	24	0x000000	A phase current fast effective value register, unsigned
1B	IN_FAST_RMS	24	0x000000	Zero wire current fast effective value register, unsigned
1E	VA_FAST_RMS	24	0x000000	A phase voltage fast effective value register, unsigned
1F	VB_FAST_RMS	24	0x000000	B-phase voltage fast effective value register, unsigned
20	VC_FAST_RMS	24	0x000000	C-phase voltage fast effective value register, unsigned

3.5.2 Fast effective value input selection

See the channel waveform block diagram for the source of the waveform. You can choose to pass hpf and not pass hpf.

0x96	MODE1	Working mode register	
No.	name	default value	description

[22]	L_F_SEL	1'b0	Leakage selection through high pass, the default is 0 to select no high pass, and 1 to select high pass

3.5.3 Fast effective value accumulation time and threshold

To calculate the fast effective value, first take the absolute value, and then integrate according to the set cumulative time. Generally, it is an integer multiple of half cycle and cycle time.

address	Name	Bit width	Defaults	description
8B	FAST_RMS_CTRL	24	0x20FFFF	[23:21] Channel fast effective value register refresh time, half cycle and n cycle can be selected, the default is half cycle; [20:0] channel fast effective value threshold register

Choose the accumulated time by FAST_RMS_CTRL[23:21], which is divided into six types: 000-10ms, 001-20ms, 010-40ms, 011-80ms, 100-160ms, 101-320ms. The default selection of half-cycle cumulative response time is 20ms, cumulative The longer the time, the smaller the beating.

FAST_RMS_CTRL[20:0] is used to set the fast effective value exceeding threshold, once exceeded, the output flag flag[N] is 1.

$$FAST\_RMS\_CTRL[20:0] = \frac{I[N]\_FAST\_RMS}{8}$$

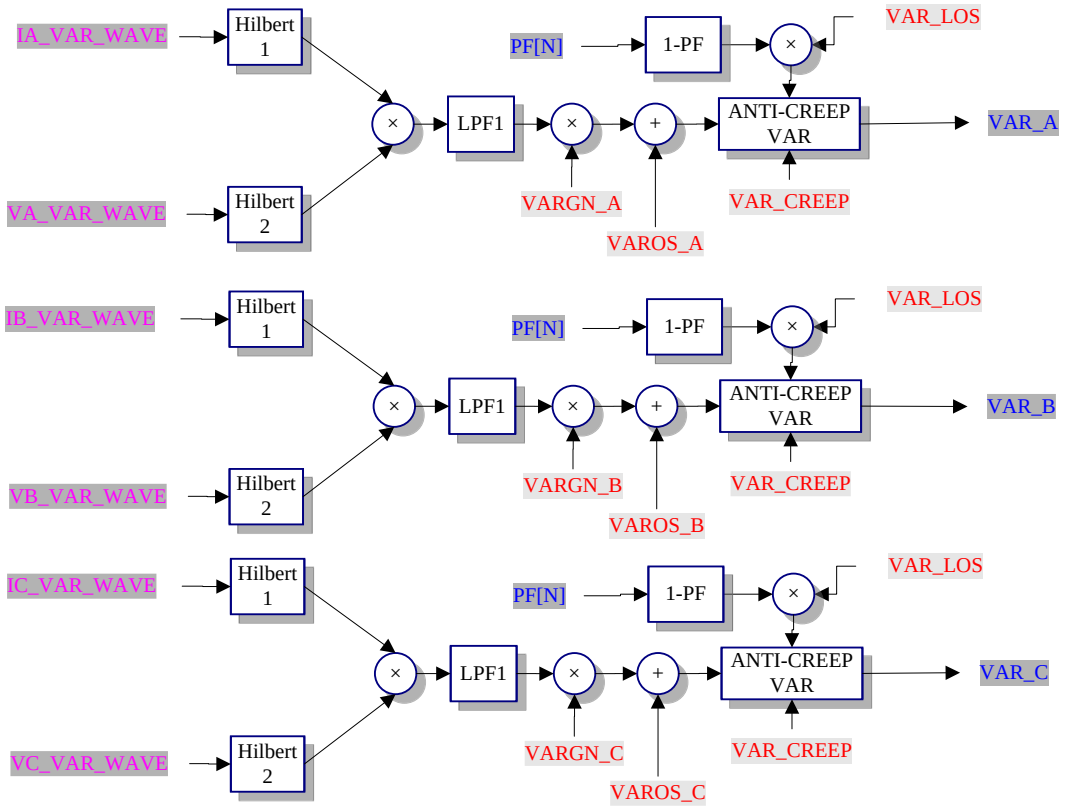
3.5.4 Grid frequency selection

In addition, it is necessary to distinguish between 50Hz and 60Hz half cycle time (AC_FREQ_SEL).

0x97	MODE2	Working mode register	
No.	name	default value	description
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1 is 60Hz, 0 is 50Hz, default selection is 50Hz

3.6 Reactive power calculation

The principle of reactive power calculation is shown in the figure below



After the current and voltage waveforms of each phase pass through the Hilbert filter, digital multiplication is performed, and then the reactive power signal can be obtained after the low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order. Obtained after integration Reactive energy pulse accumulation.

3.6.1 Reactive phase compensation

At the adc output position, a method for digital calibration of small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Since this compensation must be timely, this This method is only suitable for small phase errors of <0.6 (range. Using time-shift

technology to correct large phase errors will introduce significant phase errors in higher harmonics.

For the current and voltage signals of reactive power calculation, use a 4-bit register to adjust:

address	Name	Bit width	Defaults	description
6A	VAR_PHCAL_I	15	0x0000	Reactive phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase current channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase current channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the calculation of reactive power; [11], [7], [3] are the enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.01 degrees and 1LSB, and the maximum adjustable is ±0.08 degrees , The default is 0.04 degrees. Reactive power phase correction (coarse adjustment): [12] is the

				VAR_PHCAL2_IA register, when it is 1, the IA channel reactive power delay is 64us; [13] is the VAR_PHCAL2_IB register, when it is 1, the IB channel reactive power delay is 1. 64us; [14] is the VAR_PHCAL2_IC register, when it is 1, the IC channel reactive power delay is 64us;
6B	VAR_PHCAL_V	15	0x0000	Reactive power phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase voltage channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase voltage channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase voltage channel in the reactive power calculation; [11], [7], and [3] are the enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.01 degrees and 1LSB, and the maximum adjustable is ±0.08 degrees ,

				The default is 0.04 degrees. Reactive power phase correction (coarse adjustment): [12] is the VAR_PHCAL2_VA register, when it is 1, the VA channel reactive power delay is 64us; [13] is the VAR_PHCAL2_VB register, when it is 1, the VB channel reactive power delay is 1. 64us; [14] is the VAR_PHCAL2_VC register, when it is 1, the VC channel reactive power delay is 64us;

3.6.2 Reactive power output

Output 3 phase and combined phase reactive power, fundamental wave and full wave reactive power are given at the same time.

address	Name	Bit width	Defaults	description
5A	VAR_A	24	0x000000	Phase a (full wave) reactive power register
5B	VAR_B	24	0x000000	Phase b (full wave) reactive power register

5C	VAR_C	24	0x000000	C-phase (full wave) reactive power register
5D	VAR	24	0x000000	Combined phase (full wave) reactive power register
2A	FVAR_A	24	0x000000	Phase a (fundamental wave) reactive power register
2B	FVAR_B	24	0x000000	Phase b (fundamental wave) reactive power register
2C	FVAR_C	24	0x000000	C-phase (fundamental wave) reactive power register
2D	FVAR	24	0x000000	Combined phase (fundamental) reactive power register

3.6.3 Reactive power calibration

Contains three 16-bit reactive power offset correction registers VAROS and three 16-bit reactive gain correction registers VARGN, the default value is 0x0000.

Contains three 16-bit fundamental reactive power offset correction registers FVAROS and three 16-bit fundamental reactive gain correction registers FVARGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use data in the form of 2's complement to calibrate the deviation in the reactive power calculation. This deviation may come from input noise or phase difference, which may introduce DC offset and gain errors caused by noise. Gain and deviation correction can be Correct the reactive power measurement curve.

address	Name	Bit width	Defaults	description
B9	VARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BA	VARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BB	VARGN_C	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
C5	VAROS_A	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C6	VAROS_B	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C7	VAROS_C	16	0x0000	Corresponding channel reactive power bias adjustment register, complement

address	Name	Bit width	Defaults	description
BC	FVARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement

BD	FVARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
C8	FVAROS_A	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C9	FVAROS_B	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
CA	FVAROS_C	16	0x0000	Corresponding channel reactive power bias adjustment register, complement

Reactive power correction result:

VAR=VAR0*(1+VARGN/2^16) + VAROS*2

Where var is the active power after correction, and var0 is the reactive power before correction.

Correction result of fundamental reactive power:

FVAR=FVAR0*(1+FVARGN/2^16) + FVAROS*2

Where fvar is the active power after correction, and fvar0 is the reactive power before correction.

3.6.4 Anti-creeping of reactive power

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

The reactive power anti-creep threshold register (VAR_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input reactive power signal. When the absolute value of the input reactive power signal is less than this value The output reactive power is set to zero. This can make the value of the output to the reactive power register 0 in the case of reactive power measurement, even if there is a small noise signal.

address	Name	Bit width	Defaults	description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] IS THE REACTIVE ANTI-CREEPING POWER THRESHOLD REGISTER VAR_CREEP (INTERNAL TIMES 2^0); [11:0] IS THE ACTIVE ANTI-CREEPING POWER THRESHOLD REGISTER WA_CREEP (INTERNAL TIMES 2^0)

Var_creep can be set according to the var value of the power register, and their corresponding relationship.The anti-submarine value generally takes 20 parts per million to 200 parts per million of the full scale of reactive power.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

3.6.5 Reactive power small signal compensation

For the calculation of reactive power, in order to reduce the noise error in the small signal section, the small signal compensation register can be passed to the small signal compensation register to adjust the nonlinear error of the small signal section.

address	Name	Bit width	Defaults	description
82	VAR_LOS_A	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement.
83	VAR_LOS_B	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement.
84	VAR_LOS_C	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement.
85	FVAR_LOS_A	24	0x000	[11:0] Corresponding to reactive power (fundamental wave) small signal compensation register, complement.
86	FVAR_LOS_B	24	0x000	[11:0] Corresponding to reactive power (fundamental wave) small signal compensation register, complement.
87	FVAR_LOS_C	24	0x000	[11:0] Corresponding to reactive power (fundamental wave) small signal compensation register, complement.

3.6.6 Reactive energy output

Reactive energy can be obtained by counting reactive cf pulses, which is stored in the reactive energy accumulation register cfq_cnt, as shown in the figure below.

address	Name	Bit width	Defaults	description
3B	CFQ_A_CNT	24	0x000000	Phase a reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	Phase b reactive pulse count, unsigned

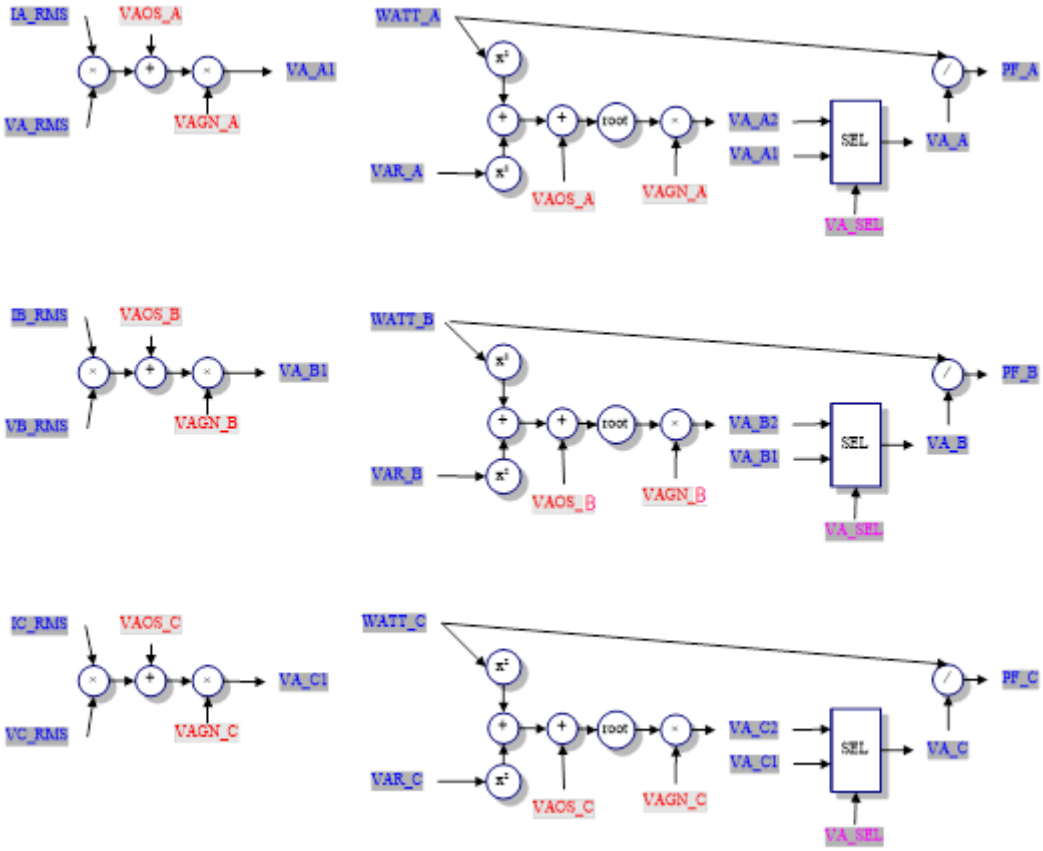
3D	CFQ_C_CNT	24	0x000000	C-PHASE REACTIVE PULSE COUNT, UNSIGNED
3E	CFQ_CNT	24	0x000000	Combination reactive pulse count, no sign
3F	CFQ1_CNT	24	0x000000	Reactive pulse count in the first quadrant, unsigned
40	CFQ2_CNT	24	0x000000	Second quadrant reactive pulse count, no sign
41	CFQ3_CNT	24	0x000000	Third quadrant reactive pulse count, no sign
42	CFQ4_CNT	24	0x000000	Fourth quadrant reactive pulse count, unsigned

Reactive energy calculation method, you can select fundamental reactive power or full-wave reactive power through var_sel, the default is fundamental reactive power:

0x98	MODE3	Working mode register	
No.	name	default value	description
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave

3.7 Apparent and power factor calculation

See the figure below for the apparent calculation principle



There are two ways of apparent calculation:

One is the digital multiplication of the effective values of current and voltage, and then gain and deviation calibration in order to obtain the reactive power signal. After integration, the reactive energy pulse accumulation is obtained. The active power is divided by the apparent power to obtain the power factor.

The second is obtained by adding the square of active power to the square of reactive power, and then opening the root sign.

The reactive power and power factor calculated in the second way have better accuracy when measuring small signals.

3.7.1 Apparent power and energy output

The output only has split-phase and combined-phase apparent power and energy.

address	Name	Bit width	Defaults	description
26	VA_A	24	0x000000	A PHASE APPARENT POWER REGISTER
27	VA_B	24	0x000000	B-PHASE APPARENT POWER REGISTER
28	VA_C	24	0x000000	C PHASE APPARENT POWER REGISTER
29	VA	24	0x000000	Conjunct apparent power register
43	CFS_A_CNT	24	0x000000	A PHASE APPARENT PULSE COUNT, UNSIGNED
44	CFS_B_CNT	24	0x000000	B-PHASE APPARENT PULSE COUNT, UNSIGNED
45	CFS_C_CNT	24	0x000000	C-PHASE APPARENT PULSE COUNT, UNSIGNED
46	CFS_CNT	24	0x000000	Conjunction apparent pulse count, no sign

3.7.2 Apparent power calibration

Contains three 16-bit apparent offset correction registers VAOS and three 16-bit apparent gain correction registers VAGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use 2's complement data to calibrate the deviation in the apparent calculation. This deviation may come from the previous stage, which may introduce offset and gain errors. Gain and deviation correction can correct the apparent measurement curve.

address	Name	Bit width	Defaults	description
BF	VAGN_A	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
C0	VAGN_B	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
C1	VAGN_C	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
CB	VAOS_A	16	0x0000	Corresponding channel apparent power bias adjustment register, complement
AND CC	VAOS_B	16	0x0000	Corresponding channel apparent power bias adjustment register, complement
CD	VAOS_C	16	0x0000	Corresponding channel apparent power bias adjustment register, complement

Correction result of apparent power:

VA=VA0*(1+VAGN/2^16) + VAOS*2

Where va is the apparent power after correction, and va0 is the apparent power before correction.

3.7.3 Power factor

Output split-phase and combined-phase power factor.

address	Name	Bit width	Defaults	description
47	PF_A	24	0x000000	Phase a power factor register
48	PF_B	24	0x000000	B-PHASE POWER FACTOR REGISTER
49	PF_C	24	0x000000	C-PHASE POWER FACTOR REGISTER
4A	PF	24	0x000000	Sum power factor register

24-bit signed number, complement. Bit[23] is the sign bit,

$$Power\ factor\ = \frac{PF}{2^{23}}$$

The calculation method of apparent power and power factor is selected by the va_sel register.

0x98	MODE3	Working mode register

No.	name	default value	description
[7]	va_sel	1'b0	va algorithm selection: 0-rmsi^2+rmsv^2; 1-(watt^2+var^2)^0.5

3.8 Calculation of three-phase current sum

3.8.1 The output of the current sum

The three-phase current sum can be selected from algebraic sum calculation, algebraic sum calculation, or fast effective value calculation, and output to:

address	Name	Bit width	Defaults	description
57	I_SUM	24	0x000000	Three-phase current instantaneous waveform and
58	I_SUM_RMS	24	0x000000	The effective value of the three-phase current instantaneous waveform sum, unsigned
59	I_SUM_FAST_RMS	24	0x000000	The fast effective value of the three-phase current instantaneous waveform sum, unsigned

3.8.2 Adjustment of current sum

Contains a 24-bit current and effective value offset correction register isum_rmsos and a 16-bit current and effective value gain correction register isum+rmsgn, the default value is 0000h.

address	Name	Bit width	Defaults	description
91	ISUM_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
92	ISUM_RMSOS	24	0x000000	Corresponding channel effective value offset correction register

3.8.3 Comparison of current sum

For the comparison of the neutral current, see the following registers:

0x98	MODE3	Working mode register	
No.	name	default value	description
[4]	isumlvl_sel	1'b0	When it is 0, compare the effective value of isumlvl and NI_RMS output neutral current; when it is 1, the effective value of the sum of instantaneous waveforms of isumlvl and the output three-phase current;

address	Name	Bit width	Defaults	description

8D	ISUMLVL	24	0xFFFFFF	Current comparison threshold register, select NI_RMS to compare with the ISUMLVL register, if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 0; if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 1. Note that IN_RMS can be selected as the effective value of the algebraic sum of three-phase transient currents Or the zero line actually measures the effective value. The function is the same as PKLVL. Mode3[4]

3.9 Small signal compensation

For the calculation of active power (fundamental wave and full wave), reactive power (fundamental wave and full wave), and apparent power, in order to reduce the noise error in the small signal section, you can pass to the small signal compensation register to adjust the small signal section Non-linear error.

address	Name	Bit width	Defaults	description

82	WA_LOS_A/ VAR_LOS_A	24	0x000000	[23:12] Corresponding to a phase active small signal compensation register, complement. [11:0] Corresponding to a phase reactive small signal compensation register, complement.
83	WA_LOS_B/ VAR_LOS_B	24	0x000000	[23:12] Corresponds to b-phase active small signal compensation register, complement. [11:0] Corresponds to b-phase reactive small signal compensation register, complement.
84	WA_LOS_C/ VAR_LOS_C	24	0x000000	[23:12] CORRESPONDS TO THE C-PHASE ACTIVE SMALL SIGNAL COMPENSATION REGISTER, COMPLEMENT. [11:0] CORRESPONDS TO THE C-PHASE REACTIVE SMALL SIGNAL COMPENSATION REGISTER, COMPLEMENT.
85	FWA_LOS_A /FVAR_LOS_A	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.

86	FWA_LOS_B/ FVAR_LOS_B	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
87	FWA_LOS_C/ FVAR_LOS_C	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.

3.10 Temperature measurement

Provide internal temperature measurement.

address	Name	Bit width	Defaults	description
5E	TPS1	10	0x0000	Internal temperature value register

3.11 Electrical parameter measurement

3.11.1 Line cycle measurement

With line cycle energy accumulation calculator, including active and reactive power.

address	Name	Bit width	Defaults	description
4B	LINE_ WATTHR	24	0x000000	Line cycle cumulative active energy register
4C	LINE_ VARHR	24	0x000000	Line cycle cumulative reactive energy register

The number of line cycles can be selected through the linecyc register:

address	Name	Bit width	Defaults	description
8F	SAGLVL/ LINECYC	24	0x100009	[23:12] The drop voltage threshold register SAGLVL, the voltage channel input is continuously lower than the value of this register for more than the time in SAGCYC, and the line voltage drop interrupt will be generated. The default is 100H, about 1116 full amplitude voltage input; [11: 0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles. Line cycle is related to external crystal oscillator, recommended crystal oscillator is 8MHz

3.11.2 Line frequency measurement

For the grid frequency test, develop a voltage channel test.

The count of the line period recorded in the PERIOD register, if the input signal deviates from 50Hzz60Hz, the corresponding count value will change.

address	Name	Bit width	Defaults	description

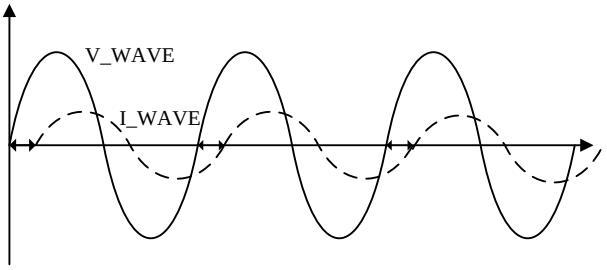
2E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)

Measure the frequency of the sine wave signal of the voltage channel.

$$Line\ voltage\ frequency\ = \frac{10000000}{PERIOD}\ \text{Hz}$$

3.11.3 Phase angle calculation

Phase angle measurement principle, see the figure below



The phase difference is obtained by calculating the time difference between the positive zero crossing of the current and the voltage, and the corresponding time value is updated to the register corner(n), and each register is a 16-bit unsigned number.

address	Name	Bit width	Defaults	description
4E	ANGLE_AB	16	0x0000	Is the phase-to-phase time register of voltage a phase and voltage b phase
4F	ANGLE_BC	16	0x0000	Is the phase-to-phase time register of voltage b-phase and voltage c-phase
50	ANGLE_AC	16	0x0000	Is the phase-to-phase time register of voltage a phase and voltage c phase

51	ANGLE_A	16	0x0000	Output a phase voltage and current time register
52	ANGLE_B	16	0x0000	Output B-phase voltage and current time register
53	ANGLE_C	16	0x0000	Output c-phase voltage and current time register

Phase angle conversion formula: 2*pi*ANGLE[N]*$\frac{f_c}{f_0}$The unit is radians

among them, f_cIs the measurement frequency of the AC signal source, the default is 50Hz, f_0Is the sampling frequency, the typical value is 1MHz.

3.11.4 Power sign bit

For power pulse cf output such as active and reactive power, there is a sign bit register indicating the direction of each cf. This direction indicates the direction of the corresponding accumulated energy (electricity or power supply) from the last cf to the current cf pulse.

address	Name	Bit width	Defaults	description
4D	SIGN	24	0x0000	CF SIGN BIT

SIGN[0]~ SIGN[23] CORRESPOND TO THE FOLLOWING CF

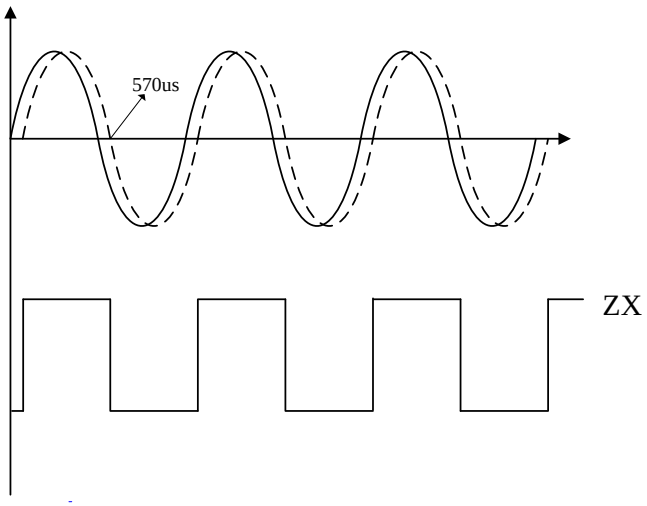
0	CF_A_CNT	8	CFN_A_CNT	16	CFQ1_CNT
1	CF_B_CNT	9	CFN_B_CNT	17	CFQ2_CNT
2	CF_C_CNT	10	CFN_C_CNT	18	CFQ3_CNT

3	CF_CNT	11	CFN_CNT	19	CFQ4_CNT
4	CFP_A_CNT	12	CFQ_A_CNT	20	CFS_A_CNT
5	CFP_B_CNT	13	CFQ_B_CNT	21	CFS_B_CNT
6	CFP_C_CNT	14	CFQ_C_CNT	22	CFS_C_CNT
7	CFP_CNT	15	CFQ_CNT	23	CFS_CNT

3.12 Fault detection

3.12.1 Zero crossing detection

Provides voltage zero-crossing detection. The zero-crossing signal is directly output from the pin ZS. ZS is zero to indicate the positive half cycle of the waveform, and zx is 1 to indicate the negative half cycle of the waveform. The delay from the actual input signal is about 570us.



3.12.2 Peak overrun

The threshold value of the effective value of current and voltage can be set by programming, which is set by the peak threshold register (i_pklvl, v_pklvl).

address	Name	Bit width	Defaults	description

8C	I_PKLVL/ V_PKLVL	24	0xFFFFFF	[23:12] Current peak value threshold register i_pklvl; [11:0] Voltage peak value threshold register v_pklvl

For example, when the fast effective value of the channel ia current is greater than the threshold set by the current peak threshold register (i_pklvl), the current overload indication pk_ia is given. If the corresponding pk_ia enable position in the interrupt mask register (mask1) is logic 1, then The irq logic output becomes active low.

Other current and voltage channels are similar, the output is placed in the status1 register

address	Name	Bit width	Defaults	description
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned

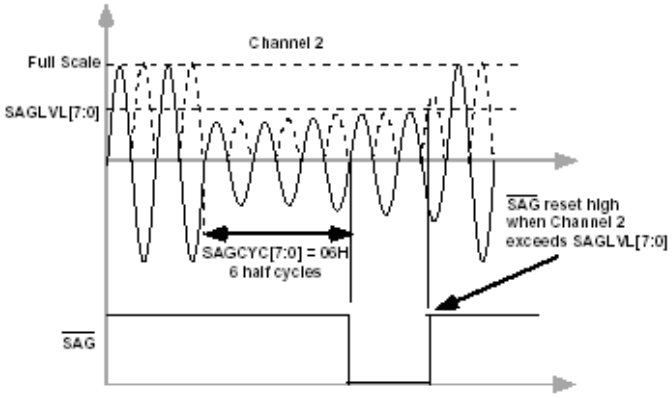
The corresponding positions are as follows:

position	Interrupt flag	Defaults	description
13	PK_VA	0	Indicates that the peak value of the effective value of the a-phase voltage channel exceeds pkvlvl interrupt, which is 1
14	PK_IA	0	Indicates that the peak value of the effective value of the phase a current channel exceeds the pkilvl interrupt, which is 1

15	PK_VB	0	Indicates that the peak value of the effective value of the phase b voltage channel exceeds the pkvlvl interrupt, which is 1
16	PK_IB	0	Indicates that the peak value of the effective value of the phase b current channel exceeds the pkilvl interrupt, which is 1
17	PK_VC	0	Indicates that the peak value of the effective value of the c-phase voltage channel exceeds pkvlvl interrupt, which is 1
18	PK_IC	0	Indicates that the peak value of the effective value of the c-phase current channel exceeds the pkilvl interrupt, which is 1
19	PK_NI	0	Indicates that the peak value of the effective value of the n-phase current channel exceeds the pkilvl interrupt, which is 1

3.12.3 Line voltage drop

It can be indicated by programming. When the effective value of the line voltage is lower than a certain peak value for more than a certain number of half cycles, an indication of the line voltage drop is given.



As shown in the figure above, when the effective value of the voltage is less than the threshold set in the drop voltage threshold register (saglvl) and the drop time exceeds the set time in the drop line cycle register (sagcyc) (the figure shows after the sixth half cycle, sagcyc[11:0]=06h), the line voltage drop event is recorded by setting the sag flag bit in the interrupt status status1 register.

position	Interrupt flag	Defaults	description
0	SAG_A	0	Indicates that a phase line voltage drop interrupt is generated, and the drop is 1
1	SAG_B	0	Indicates that the voltage drop of phase b is interrupted, and the drop is 1
2	SAG_C	0	Indicates that the voltage drop interruption of phase c is generated, and the drop is 1

If the corresponding sag enable position in the interrupt mask register (mask1) is logic 1, the irq logic output becomes active low.

address	Name	Bit width	Defaults	description

8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] Fall line period register sagcyc, default 04h. [15:0] Zero-crossing timeout register zxtout, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated, default ffffh.
8F	SAGLVL/ LINECYC	24	0x100009	[23:12] The drop voltage threshold register SAGLVL, the voltage channel input is continuously lower than the value of this register for more than the time in SAGCYC, and the line voltage drop interrupt will be generated. The default is 100H, about 1116 full amplitude voltage input; [11: 0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles. Line cycle is related to external crystal oscillator, recommended crystal oscillator is 8MHz

The drop voltage threshold register (SAGLVL) can be written or read by the user, and the initial value is FFFH. The drop line period register (SAGCYC) can also be

written or read by the user, and the initial value is FFH. The resolution of this register is 10mss LSB, the maximum delay time of such an interrupt is limited to 2.55s.

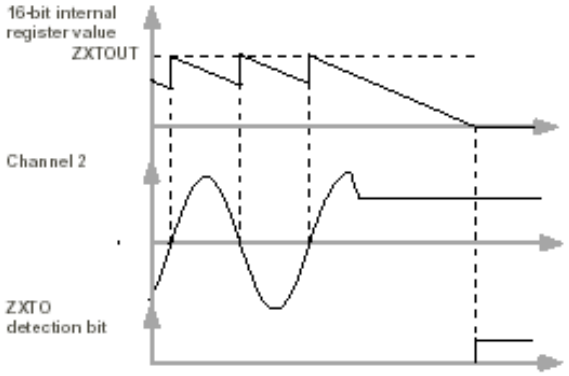
3.12.4 Zero crossing timeout

The zero-crossing detection circuit is also connected to a register zxtout that detects the zero-crossing signal timeout. Whenever the detection voltage channel has a zero-crossing signal, zxtout is set to the initial value. If there is no zero-crossing signal, it will decrement. When the zero signal is output, the value in this register will become 0. At this time, the corresponding bit zxto in the interrupt status register is set to 1. If the corresponding enable bit zxto in the interrupt mask register is also 1, the zero crossing signal Timeout events are also reflected on the interrupt pin irq. Regardless of whether the corresponding enable bit in the interrupt register is set or not, the zxto flag bit in the interrupt status register (mask) is always set to be valid when the zxtout register is reduced to 0 1.

address	Name	Bit width	Defaults	description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] Fall line period register sagcyc, default 04h. [15:0] Zero-crossing timeout register zxtout, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated, default ffffh.

The zero-crossing timeout register ZXTOUT can be written or read by the user, the initial value is FFFFH. The resolution of this register is 70.5uss LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



The comparison result is placed in the status1 register, corresponding to the location:

position	Interrupt flag	Defaults	description
3	ZXTO_A	0	Indicate the generation of a phase zero crossing timeout interrupt, the timeout is 1
4	ZXTO_B	0	Indicates that the phase b zero-crossing timeout interrupt is generated, and the timeout is 1
5	ZXTO_C	0	Indicate the generation of phase c zero-crossing timeout interrupt, the timeout is 1

3.12.5 Zero crossing indicator

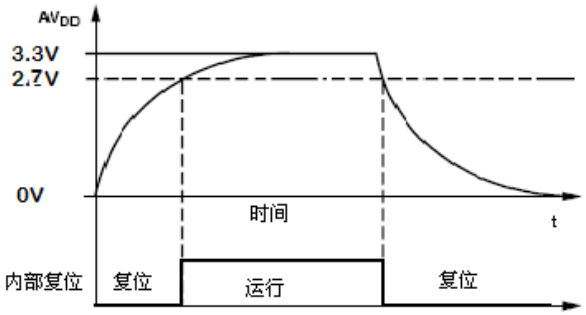
The result is placed in the status1 register, corresponding to the location:

position	Interrupt flag	Defaults	description
6	ZX_VA	0	Indicate the sign bit of a phase voltage waveform
7	ZX_IA	0	Indicate the sign bit of phase a current waveform
8	ZX_VB	0	Indicate the sign bit of the b-phase voltage waveform
9	ZX_IB	0	Indicate the sign bit of phase b current waveform
10	ZX_VC	0	Indicate the sign bit of the c-phase voltage waveform
11	ZX_IC	0	Indicate the sign bit of the c-phase current waveform
12	ZX_IN	0	Indicates the sign bit of the n-phase current waveform

3.12.6 Power supply indication

Contains an on-chip power monitoring circuit that can continuously detect analog power (avdd). If the power supply voltage is less than 2.7v ± 5%, the entire circuit is not

activated (not working), that is to say, when the power supply voltage is less than 2.7v, it is not performed Energy accumulation. This approach can ensure that the device maintains correct operation when the power is powered on. This power monitoring circuit has a hysteresis and filtering mechanism, which can eliminate false triggers caused by noise to a large extent. Generally, the power supply The decoupling part of the power supply should ensure that the ripple on the avdd does not exceed 3.3v (5%.



片内电源供电监视

4、 Internal register

4.1 Electrical parameter register (external read)

address	Name	Bit width	Defaults	description
2	IC_WAVE	24	0x000000	C-PHASE CURRENT WAVEFORM REGISTER
3	IB_WAVE	24	0x000000	Phase b current waveform register
4	IA_WAVE	24	0x000000	Phase a current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	Phase a voltage waveform register
9	VB_WAVE	24	0x000000	Phase b voltage waveform register
A	VC_WAVE	24	0x000000	C-phase voltage waveform register
D	IC_RMS	24	0x000000	C-phase current effective value register, unsigned
E	IB_RMS	24	0x000000	Phase b current RMS register, unsigned
F	IA_RMS	24	0x000000	Phase a current effective value register, unsigned
10	IN_RMS	24	0x000000	Zero wire current RMS register, unsigned
13	VA_RMS	24	0x000000	Phase a voltage effective value register, unsigned

14	VB_RMS	24	0x000000	Phase b voltage effective value register, unsigned
15	VC_RMS	24	0x000000	C-phase voltage effective value register, unsigned
18	IC_FAST_RMS	24	0x000000	C-phase current fast effective value register, unsigned
19	IB_FAST_RMS	24	0x000000	B-phase current fast effective value register, unsigned
1A	IA_FAST_RMS	24	0x000000	A phase current fast effective value register, unsigned
1B	IN_FAST_RMS	24	0x000000	Zero wire current fast effective value register, unsigned
1E	VA_FAST_RMS	24	0x000000	A phase voltage fast effective value register, unsigned
1F	VB_FAST_RMS	24	0x000000	B-phase voltage fast effective value register, unsigned
20	VC_FAST_RMS	24	0x000000	C-phase voltage fast effective value register, unsigned
22	WATT_A	24	0x000000	A-phase active power register (full wave and fundamental wave optional)

23	WATT_B	24	0x000000	B-phase active power register (full wave and fundamental wave optional)
24	WATT_C	24	0x000000	C-phase active power register (full wave and fundamental wave optional)
25	WATT	24	0x000000	Combined active power register (full wave and fundamental wave optional)
26	VA_A	24	0x000000	A PHASE APPARENT POWER REGISTER
27	VA_B	24	0x000000	B-PHASE APPARENT POWER REGISTER
28	VA_C	24	0x000000	C PHASE APPARENT POWER REGISTER
29	VA	24	0x000000	Conjunct apparent power register
2A	FVAR_A	24	0x000000	Phase a (fundamental wave) reactive power register
2B	FVAR_B	24	0x000000	Phase b (fundamental wave) reactive power register
2C	FVAR_C	24	0x000000	C-phase (fundamental wave) reactive power register
2D	FVAR	24	0x000000	Combined phase (fundamental) reactive power register

2E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)
2F	CF_A_CNT	24	0x000000	Phase a active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B-phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C-PHASE ACTIVE PULSE COUNT, UNSIGNED
32	CF_CNT	24	0x000000	Conjunction active pulse count, no sign
33	CFP_A_CNT	24	0x000000	Phase a positive active pulse count, no sign
34	CFP_B_CNT	24	0x000000	B-phase positive active pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C-PHASE POSITIVE ACTIVE PULSE COUNT, UNSIGNED
36	CFP_CNT	24	0x000000	Conjunction positive active pulse count, no sign
37	CFN_A_CNT	24	0x000000	Phase a negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B-phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C-PHASE NEGATIVE ACTIVE PULSE COUNT, UNSIGNED

3A	CFN_CNT	24	0x000000	Conjunction negative active pulse count, unsigned
3B	CFQ_A_CNT	24	0x000000	Phase a reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	Phase b reactive pulse count, unsigned
3D	CFQ_C_CNT	24	0x000000	C-PHASE REACTIVE PULSE COUNT, UNSIGNED
3E	CFQ_CNT	24	0x000000	Combination reactive pulse count, no sign
3F	CFQ1_CNT	24	0x000000	Reactive pulse count in the first quadrant, unsigned
40	CFQ2_CNT	24	0x000000	Second quadrant reactive pulse count, no sign
41	CFQ3_CNT	24	0x000000	Third quadrant reactive pulse count, no sign
42	CFQ4_CNT	24	0x000000	Fourth quadrant reactive pulse count, unsigned
43	CFS_A_CNT	24	0x000000	A PHASE APPARENT PULSE COUNT, UNSIGNED
44	CFS_B_CNT	24	0x000000	B-PHASE APPARENT PULSE COUNT, UNSIGNED

45	CFS_C_CNT	24	0x000000	C-PHASE APPARENT PULSE COUNT, UNSIGNED
46	CFS_CNT	24	0x000000	Conjunction apparent pulse count, no sign
47	PF_A	24	0x000000	Phase a power factor register
48	PF_B	24	0x000000	B-PHASE POWER FACTOR REGISTER
49	PF_C	24	0x000000	C-PHASE POWER FACTOR REGISTER
4A	PF	24	0x000000	Sum power factor register
4B	LINE_ WATTHR	24	0x000000	Line cycle cumulative active energy register
4C	LINE_ VARHR	24	0x000000	Line cycle cumulative reactive energy register
4D	SIGN	24	0x0000	CF SIGN BIT
4E	ANGLE_AB	16	0x0000	Is the phase-to-phase time register of voltage a phase and voltage b phase
4F	ANGLE_BC	16	0x0000	Is the phase-to-phase time register of voltage b-phase and voltage c-phase
50	ANGLE_AC	16	0x0000	Is the phase-to-phase time register of voltage a phase and voltage c phase

51	ANGLE_A	16	0x0000	Output a phase voltage and current time register
52	ANGLE_B	16	0x0000	Output B-phase voltage and current time register
53	ANGLE_C	16	0x0000	Output c-phase voltage and current time register
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned
55	STATUS2	24	0x000000	Interrupt status register 2, unsigned
56	STATUS3	24	0x000000	Interrupt status register 3, unsigned
57	I_SUM	24	0x000000	Three-phase current instantaneous waveform and
58	I_SUM_RMS	24	0x000000	The effective value of the three-phase current instantaneous waveform sum, unsigned
59	I_SUM_FAST_RMS	24	0x000000	The fast effective value of the three-phase current instantaneous waveform sum, unsigned
5A	VAR_A	24	0x000000	Phase a (full wave) reactive power register
5B	VAR_B	24	0x000000	Phase b (full wave) reactive power register

5C	VAR_C	24	0x000000	C-phase (full wave) reactive power register
5D	VAR	24	0x000000	Combined phase (full wave) reactive power register
5E	TPS1	10	0x0000	Internal temperature value register

4.2 Calibration register (external write)

address	Name	Bit width	Defaults	description
60	GAIN1	24	0x000000	Channel pga gain adjustment register, see "Front-end gain adjustment" description for details. [11:8]:C-PHASE CURRENT [15:12]:B PHASE CURRENT [19:16]:A PHASE CURRENT [23:20]:Neutral line current
61	GAIN2	20	0x00000	Channel pga gain adjustment register, see "Front-end gain adjustment" description for details. [11:8]:A PHASE VOLTAGE [15:12]: PHASE B VOLTAGE [19:16]:C PHASE VOLTAGE

62	IRMS_P1	24	0x010000	The angle difference segment point defines P1, which satisfies IRMSmin<P1<P2<IRMSmax
63	IRMS_P2	24	0x200000	The angle difference segment point defines P2, which satisfies IRMSmin<P1<P2<IRMSmax
64	IA_PHCAL	24	0x000000	A phase current channel angle difference correction register, when IRMSmin<effective value of input current<P1, [7:0] is the current channel phase used for correction, [7] is the enable bit, the minimum adjustment delay time is 250ns, corresponding to 0.0045 Degree 1LSB, the maximum adjustable is ±0.574 degrees). When P1<effective value of input current<P2, [15:8] is used to correct the current channel phase, [15] is the enable bit, and the adjustment accuracy is the same as above. When P2 <The effective value of input

				current<IRMSmax, [23:16] is the current channel phase used for correction, [23] is the enable bit, and the adjustment accuracy is the same as above.
65	IB_PHCAL	24	0x000000	B-phase current channel angle difference correction register (same as above)
66	IC_PHCAL	24	0x000000	C-phase current channel angle difference correction register (same as above)
67	VA_PHCAL	24	0x000000	Phase A voltage channel angle correction register, when IRMSmin<effective value of input current<P1, [7:0] is the voltage channel phase used for correction, [7] is the enable bit, the minimum adjustment delay time is 250ns, corresponding to 0.0045 Degree 1LSB, maximum adjustable ±0.574 degrees). When P1<effective value of input

				current<P2, [15:8] is used to correct the current channel phase, [15] is the enable bit, and the adjustment accuracy is the same as above. When P2 <The effective value of the input current<IRMSmax, [23:16] is used to correct the phase of the voltage channel, [23] is the enable bit, and the adjustment accuracy is the same as above.
68	VB_PHCAL	24	0x000000	B-phase voltage channel angle difference correction register (same as above)
69	VC_PHCAL	24	0x000000	C-phase voltage channel angle difference correction register (same as above)
6A	VAR_PHCAL_I	15	0x0000	Reactive phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase current channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase current

				channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the calculation of reactive power; [11], [7], [3] are the enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.01 degrees and 1LSB, and the maximum adjustable is ±0.08 degrees , The default is 0.04 degrees. Reactive power phase correction (coarse adjustment): [12] is the VAR_PHCAL2_IA register, when it is 1, the IA channel reactive power delay is 64us; [13] is the VAR_PHCAL2_IB register, when it is 1, the IB channel reactive power delay is 1. 64us; [14] is the VAR_PHCAL2_IC register, when it is 1, the IC channel reactive power delay is 64us;

6B	VAR_PHCAL_V	15	0x0000	Reactive power phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase voltage channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase voltage channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase voltage channel in the reactive power calculation; [11], [7], and [3] are the enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.01 degrees and 1LSB, and the maximum adjustable is ±0.08 degrees , The default is 0.04 degrees. Reactive power phase correction (coarse adjustment): [12] is the VAR_PHCAL2_VA register, when it is 1, the VA channel reactive power delay is 64us; [13] is the VAR_PHCAL2_VB register, when it is 1, the VB channel reactive power delay

				is 1. 64us; [14] is the VAR_PHCAL2_VC register, when it is 1, the VC channel reactive power delay is 64us;
6D	IC_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
6E	IB_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
6F	IA_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
70	IN_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
73	VA_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
74	VB_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
75	VC_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
78	IC_RMSOS	24	0x000000	Corresponding channel effective value offset correction register

79	IB_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7A	IA_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7B	IN_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7E	VA_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
7F	VB_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
80	VC_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
82	WA_LOS_A/ VAR_LOS_A	24	0x000000	[23:12] Corresponding to a phase active small signal compensation register, complement. [11:0] Corresponding to a phase reactive small signal compensation register, complement.
83	WA_LOS_B/ VAR_LOS_B	24	0x000000	[23:12] Corresponds to b-phase active small signal compensation register, complement. [11:0] Corresponds to b-

				phase reactive small signal compensation register, complement.
84	WA_LOS_C/ VAR_LOS_C	24	0x000000	[23:12] CORRESPONDS TO THE C-PHASE ACTIVE SMALL SIGNAL COMPENSATION REGISTER, COMPLEMENT. [11:0] CORRESPONDS TO THE C-PHASE REACTIVE SMALL SIGNAL COMPENSATION REGISTER, COMPLEMENT.
85	FWA_LOS_A /FVAR_LOS_A	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
86	FWA_LOS_B/ FVAR_LOS_B	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
87	FWA_LOS_C/ FVAR_LOS_C	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] Reactive anti-creeping power threshold register

				[11:0] is the active anti-creeping power threshold register
89	VAR_CREEP2/ WA_CREEP2	24	0x000000	[23:12] is the total reactive power anti-creeping power threshold register [11:0] total active anti-creeping power threshold register;
8A	REVP_CREEP/ RMS_CREEP	24	0x04C200	[23:12] IS THE REVERSE INDICATION THRESHOLD REGISTER REVP_CREEP; [11:0] IS THE EFFECTIVE VALUE SMALL SIGNAL THRESHOLD REGISTER RMS_CREEP
8B	FAST_RMS_CTRL	24	0x20FFFF	[23:21] Channel fast effective value register refresh time, half cycle and n cycle can be selected, the default is half cycle; [20:0] channel fast effective value threshold register
8C	I_PKLVL/ V_PKLVL	24	0xFFFFFF	[23:12] Current peak value threshold register i_pklvl; [11:0] Voltage peak value threshold register v_pklvl

8D	ISUMLVL	24	0xFFFFFF	Current comparison threshold register, select NI_RMS to compare with the ISUMLVL register, if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 0; if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 1. Note that IN_RMS can be selected as the effective value of the algebraic sum of three-phase transient currents Or the zero line actually measures the effective value. The function is the same as PKLVL. Mode3[4]
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] Fall line period register sagcyc, default 04h. [15:0] Zero-crossing timeout register zxtout, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated, default ffffh.

8F	SAGLVL/ LINECYC	24	0x100009	[23:12] The drop voltage threshold register SAGLVL, the voltage channel input is continuously lower than the value of this register for more than the time in SAGCYC, and the line voltage drop interrupt will be generated. The default is 100H, about 1116 full amplitude voltage input; [11: 0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles. Line cycle is related to external crystal oscillator, recommended crystal oscillator is 8MHz
90	IN_PHCAL	24	0x000000	IN phase current channel angle difference correction register, when IRMSmin<effective value of input current<P1, [7:0] is used to correct the current channel phase, [7] is the enable bit, the minimum adjustment delay time is 280ns, corresponding to 0.005

				Degree 1LSB, maximum adjustable ±0.625 degrees). When IRMSmin<effective value of input current<P1, [7:0] is used to correct the current channel phase, [7] is the enable bit, and the minimum adjustment delay time is 280ns , Corresponding to 0.005 degrees 1LSB, the maximum adjustable is ±0.625 degrees). When P1<effective value of input current<P2, [15:8] is used to correct the phase of the current channel, [15] is the enable bit, and the adjustment accuracy is the same as above .When P2<effective value of input current<IRMSmax, [23:16] is used to correct the current channel phase, [23] is the enable bit, and the adjustment accuracy is the same as above.
91	ISUM_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register

92	ISUM_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
93	ADC_PD	11	0x000	Enable control of 7 channels adc [2]: C PHASE CURRENT [3]: B-PHASE CURRENT [4]: Phase a current [5]: Neutral line current [8]: Phase a voltage [9]: B-PHASE VOLTAGE [10]:C-PHASE VOLTAGE
94	TPS_CTRL	16	0x07FF	[15] Temperature measurement switch, 0xb1 temperature measurement is off, 0xb0 is turned on, default 0xb0, temperature measurement is turned on
96	MODE1	24	0x000000	User mode selection register 1
97	MODE2	24	0x000000	User mode selection register 2
98	MODE3	24	0x000000	User mode selection register 3
9A	MASK1	24	0x000000	Interrupt mask register, which controls whether an interrupt generates a valid irq1 output, see "Interrupt Mask Register" description for details

9B	MASK2	24	0x000000	Interrupt mask register, which controls whether an interrupt generates a valid irq2 output, see "Interrupt Mask Register" description for details
9D	RST_ENG	24	0x000000	Energy clearing setting register, see "Energy clearing setting register" description for details
9E	USR_WRPROT	16	0x0000	User write protection setting register
9F	SOFT_RESET	24	0x000000	When the input is 5a5a5a, the system is reset-only the state machine and registers of the digital part are reset! When the input is 55AA55, the user read and write registers are reset-Reset: reg60 to reg9f, rega0 to regd0

4.3 Calibration p register

Calibration register

address	Name	Bit width	Defaults	description
A1	IC_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement

A2	IB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A3	IA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A7	VA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
AC	IC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AE	IA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement

B2	VA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B3	VB_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B4	VC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B6	WATTGN_A	16	0x0000	Corresponding channel active power gain adjustment register, complement
B7	WATTGN_B	16	0x0000	Corresponding channel active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	Corresponding channel active power gain adjustment register, complement
B9	VARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BA	VARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BB	VARGN_C	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BC	FVARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement

BD	FVARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BF	VAGN_A	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
C0	VAGN_B	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
C1	VAGN_C	16	0x0000	Corresponding channel apparent power gain adjustment register, complement
C2	WATTOS_A	16	0x0000	Corresponding channel active power bias adjustment register, complement
C3	WATTOS_B	16	0x0000	Corresponding channel active power bias adjustment register, complement
C4	WATTOS_C	16	0x0000	Corresponding channel active power bias adjustment register, complement
C5	VAROS_A	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C6	VAROS_B	16	0x0000	Corresponding channel reactive power bias adjustment register, complement

C7	VAROS_C	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C8	FVAROS_A	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C9	FVAROS_B	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
CA	FVAROS_C	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
CB	VAOS_A	16	0x0000	Corresponding channel apparent power bias adjustment register, complement
AND CC	VAOS_B	16	0x0000	Corresponding channel apparent power bias adjustment register, complement
CD	VAOS_C	16	0x0000	Corresponding channel apparent power bias adjustment register, complement
CE	CFDIV	12	0x010	Active cf scaling register [11:0]
D0	checksum	16	0x0010	Calibration register checksum, checksum has problems and restores to the default value

4.4 Mode register

4.4.1 Mode register 1

0x96	MODE1	Working mode register	
No.	name	default value	description
[10:0]		00	Keep
[21:11]		00	Keep
[22]	L_F_SEL	1'b0	Leakage selection through high pass, the default is 0 to select no high pass, and 1 to select high pass
[23]	WAVE_REG_SEL	1'b0	Current wave waveform register output selection, default 0 selects the waveform of the normal current channel, and 1 selects the waveform output of the leakage channel

4.4.2 Mode register 2

0x97	MODE2	Working mode register	
No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection, 00-high pass, 01-select fundamental wave, 11-select sinc output [3,2]: C PHASE CURRENT

			[5,4]: B-PHASE CURRENT [7,6]: Phase a current [8,9]: Neutral line current [15,14]: PHASE A VOLTAGE [17,16]: PHASE B VOLTAGE [19,18]:C-PHASE VOLTAGE
[22]	RMS_UPDATE_SEL	1'b0	Slow effective value register update speed selection, 1 is 1000ms, 0 is 500ms, 500ms is selected by default;
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1 is 60Hz, 0 is 50Hz, default selection is 50Hz

4.4.3 Mode register 3

0x98	MODE3	Working mode register	
No.	name	default value	description
[4]	isumlvl_sel	1'b0	When it is 0, compare the effective value of isumlvl and NI_RMS output neutral current; when it is 1, the effective value of the sum of instantaneous waveforms of isumlvl and the output three-phase current;
[6:5]	period_sel	2'00	Line voltage frequency cycle channel selection 2'b00-A; 2'b01-B; 2'b10-C; 2'b11-A

[7]	va_sel	1'b0	va algorithm selection: 0-rmsi^2+rmsv^2; 1-(watt^2+var^2)^0.5
[8]	add_sel	1'b0	watt and var conjoint sum addition method: 0-absolute value addition, |a|+|b|+|c|; 1-algebraic sum addition, a+b+c
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable
[13:10]	CF_SEL	4'b0000	Channel cf_watt, cf_var output selection, The default is 0000, turn off cf_watt, cf_var; 0001, the power CF of watt_aavar_a; 0010, the power CF of watt_bbvar_b; 0011, power CF of watt_ccvar_c; 0100, power CF of watttvar; 0101, watt_p_aavar1 power CF; 0110, watt_p_bbvar2 power CF; 0111, power CF of watt_p_ccvar3; 1000, power CF of watt_ppvar4; 1001, watt_n_aava_a power CF; 1010, watt_n_va_b power CF; 1011,watt_n_ccva_c power CF; 1100,watt_nnva power CF 1101, (SAME AS 0100); 1110, APPARENT POWER CF; 1111, CLOSE CF;
[14]			Keep
[15]	cf_add_sel	1'b0	Watt and var energy addition methods: 0-absolute value addition; 1-algebraic sum addition (separation and combination)
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave
[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave, determined by mode1[10:0]; 1-fundamental wave, determined by mode1[21:11]
[18]	IRQ_SEL	1'b0	0-OUTPUT IRQ112, DEFAULT;

4.5 Interrupt status register

4.5.1 STATUS1 REGISTER

Interrupt register 1 0x54

Bit	Interrupt flag	Defaults	description
0	SAG_A	0	Indicates that a phase line voltage drop interrupt is generated, and the drop is 1
1	SAG_B	0	Indicates that the voltage drop of phase b is interrupted, and the drop is 1
2	SAG_C	0	Indicates that the voltage drop interruption of phase c is generated, and the drop is 1
3	ZXTO_A	0	Indicate the generation of a phase zero crossing timeout interrupt, the timeout is 1
4	ZXTO_B	0	Indicates that the phase b zero-crossing timeout interrupt is generated, and the timeout is 1
5	ZXTO_C	0	Indicate the generation of phase c zero-crossing timeout interrupt, the timeout is 1
6	ZX_VA	0	Indicate the sign bit of a phase voltage waveform
7	ZX_IA		Indicate the sign bit of phase a current waveform
8	ZX_VB		Indicate the sign bit of the b-phase voltage waveform
9	ZX_IB		Indicate the sign bit of phase b current waveform
10	ZX_VC		Indicate the sign bit of the c-phase voltage waveform

11	ZX_IC		Indicate the sign bit of the c-phase current waveform
12	ZX_IN		Indicates the sign bit of the n-phase current waveform
13	PK_VA	0	Indicates that the peak value of the effective value of the a-phase voltage channel exceeds pkvlvl interrupt, which is 1
14	PK_IA	0	Indicates that the peak value of the effective value of the phase a current channel exceeds the pkilvl interrupt, which is 1
15	PK_VB	0	Indicates that the peak value of the effective value of the phase b voltage channel exceeds the pkvlvl interrupt, which is 1
16	PK_IB	0	Indicates that the peak value of the effective value of the phase b current channel exceeds the pkilvl interrupt, which is 1
17	PK_VC	0	Indicates that the peak value of the effective value of the c-phase voltage channel exceeds pkvlvl interrupt, which is 1
18	PK_IC	0	Indicates that the peak value of the effective value of the c-phase current channel exceeds the pkilvl interrupt, which is 1
19	PK_NI	0	Indicates that the peak value of the effective value of the n-phase current channel exceeds the pkilvl interrupt, which is 1
20	pk_isum	0	Indicate three-phase current and exceed threshold

21	PS_V	0	Voltage phase sequence, 0 is normal, 1 is reverse phase sequence, suitable for three-phase four-wire. When there is a phase failure, the output is 0;
22	PS_I	0	Indicate the current phase sequence, 0 is normal, 1 is the reverse phase sequence, the current phase sequence detection is only accurate when the current value is greater than 5%Ib; when there is a phase failure, the output is 0; suitable for three-phase four-wire;

4.5.2 STATUS2 REGISTER

Interrupt register 2 0x55

Bit	Interrupt flag	Defaults	description
0	REVP_WATT_A	0	Indicates that the sign of phase a active power calculation has changed
1	REVP_WATT_B	0	Indicates that the sign of phase b active power calculation has changed
2	REVP_WATT_C	0	Indicates that the sign of the c-phase active power calculation has changed
3	REVP_VAR	0	Indicates that the sign of a phase reactive power calculation has changed

4	REVP_VAR	0	Indicates that the sign of phase b reactive power calculation has changed
5	REVP_VAR	0	Indicates the sign change of c-phase reactive power calculation
6	REVP_FVAR	0	Indicates that the sign of the phase a fundamental reactive power calculation has changed
7	REVP_FVAR	0	Indicates that the sign of the phase b fundamental reactive power calculation has changed
8	REVP_FVAR	0	Indicate the sign change of c-phase fundamental reactive power calculation
9	REVP_FWATT_A	0	Indicate the sign change of the fundamental active power calculation of phase a
10	REVP_	0	Indicates that the sign of the fundamental active power calculation of phase b has changed
11	REVP_FWATT_C	0	Indicates that the sign of the c-phase fundamental active power calculation has changed
12	REVP_VA_A	0	Indicates a sign change in the apparent power calculation of phase a
13	REVP_VA_B	0	Indicates that the apparent power calculation of phase b has a sign change
14	REVP_VA_C	0	Indicates that the apparent power calculation of phase c has a sign change

15	REVP_WATT	0	Indicates the sign change of the total active power calculation of the combined phase
16	REVP_FWATT	0	Indicates the sign change of the total fundamental active power calculation of the combined phase
17	REVP_WATT_OR/ REVP_FWATT_OR	0	Indicates the sign change of the fundamental active power calculation of any one phase of the three-phase active power rate
18	REVP_VAR_OR	0	Indicate the sign change of any phase reactive power calculation in the three phases
19	REVP_FAVR_OR	0	Indicates that the fundamental reactive power calculation of any one of the three phases has a sign change
20	REVP_VA_OR	0	Indicates that the apparent power calculation of any one of the three phases has a sign change
21	VREF_LOW	0	Indicates that the reference voltage value is low, when it is 1, vref<1v; when it is 0, it is normal
22	SPI_INPUT_ERR	0	SPI INPUT CHECK, WHEN IT IS 1, THE CHECKSUM IS WRONG; WHEN IT IS 0, IT IS NORMAL
23	UART_INPUT_ERR	0	UART INPUT CHECK, WHEN IT IS 1, THE CHECKSUM IS WRONG; WHEN IT IS 0, IT IS NORMAL

5、 Communication Interface

Register data are all sent in 3 bytes (24bit), register data less than 3 bytes, unused bits are filled with 0, and 3 bytes are sent together.

Select by pin sel, when sel=1, it is spi, when sel=0, it is uart

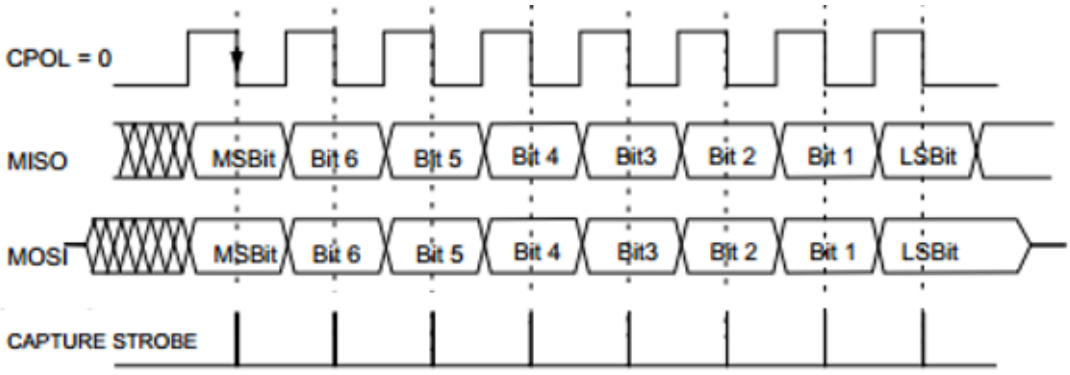
5.1 SPI

5.1.1 Overview

- ✓ Slave mode, half-duplex communication, maximum communication speed 1.5m
- ✓ 8-bit data transmission, MSB first, LSB behind
- ✓ Fix a clock polarity phase (cpol=0, cpha=1)

5.1.2 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state, SCLK is at low level, and the data transmission is on the first edge, that is, the transition of SCLK from low to high, so Data sampling is on the falling edge, and data transmission is on the rising edge.



5.1.3 Frame structure

In the communication mode, first send the 8bit identification byte (0x81) or (0x82), (0x82) is the read identification byte, (0x81) is the write identification byte, and then the register address byte is sent to determine the address of the access register (Please refer to the BL6552 register list). The following figure shows the data transfer sequence of read and write operations respectively. After one frame of data transfer is completed, BL6552 re-enters the communication mode. The number of SCLK pulses required for each read and write operation Both are 48 bits.

There are two types of frame structures, which are explained as follows:

1) Write register

Cmd: {0x81}+ Addr+Data_H+Data_M+Data_L+SUM

{0x81} is the frame identification byte of the write operation;

Addr is the internal register address of BL6552 corresponding to the write operation;

The checksum byte CHECKSUM is (((0x81)+ADDR+DATA_H+DATA_M+DATA_L)& 0xFF) and then inverted by bit.

写操作帧	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

2) Read register

Cmd:{0x82}+Addr

Returns: Data_H+Data_M+Data_L+SUM

{0x82} is the frame identification byte of the read operation;

Addr is the internal register address of BL6552 corresponding to the read operation (0x00-0xff);

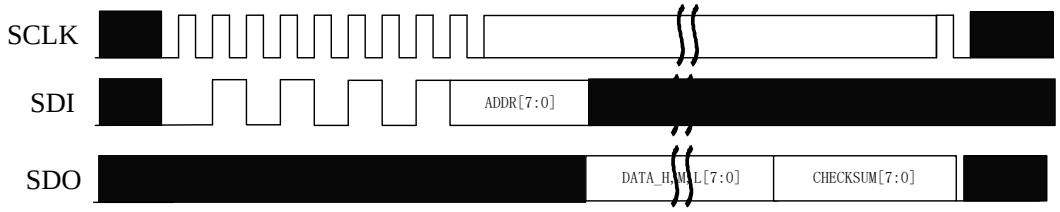
Among them, the checksum byte CHECKSUM is (((0x82)+ADDR+DATA_H+DATA_M+DATA_L)& 0xFF) and then inverted by bit.

读命令帧	0x82	ADDR[7:0]

读数据帧	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

5.1.4 Read operation timing

During the data read operation of bl6552, at the rising edge of sclk, bl6552 shifts the corresponding data out to the dout logic output pin. During the next time when the sclk is 1, the dout value remains unchanged, that is, at the next At the falling edge, the external device can sample the dout value. Like the data write operation, the MCU must first send the identification byte and address byte before the data read operation.

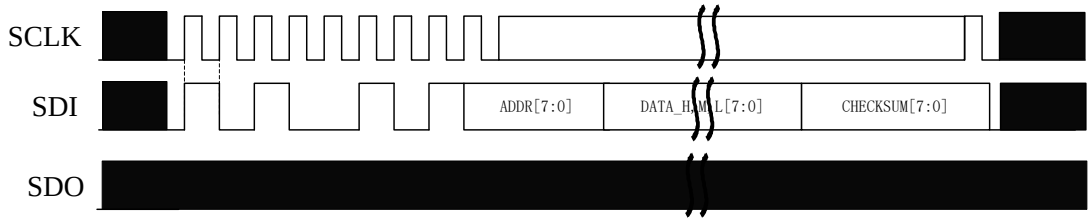


When BL6552 is in communication mode, the frame identification byte {0x82} indicates that the next data transfer operation is read. Then the byte immediately following is the address of the target register to be read. BL6552 starts to move out of the register on the rising edge of SCLK All the remaining bits of the register data are shifted out on the subsequent rising edge of SCLK. Therefore, on the falling edge, the

external device can sample the output data of the SPI. Once the read operation is over, the serial interface will re-enter the communication mode At this time, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK signal.

5.1.5 Write operation timing

The serial writing sequence is carried out in the following manner. The frame identification byte {0x81} indicates that it is written during data transfer operations. The MCU will prepare the data bits that need to be written to BL6552 before the lower edge of SCLK, and at this clock of SCLK The lower edge of the SCLK starts to shift in the register data. All the remaining bits of the register data are also shifted to the left on the lower edge of the SCLK.



5.1.6 Fault tolerance mechanism of spi interface

1) If the frame recognition byte is wrong or the sum byte is wrong, the frame data is abandoned.

2) SPI module reset: send 6 bytes of 0xFF through the SPI interface, and the SPI interface can be reset separately;

3) _CS IS PULLED HIGH TO RESET.

5.2 UART

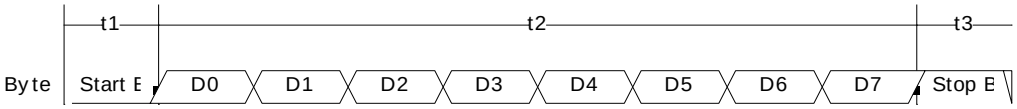
5.2.1 Overview

- ✓ Select by pin uart_sel, when sel=1, it is spi, when sel=0, it is uart
- ✓ The communication baud rate is 4800bpss9600bpss19200bpss38400bpss, no parity, stop bit 1;

Baud rate setting	4800	9600	19200	38400
CS PIN	0	0	1	1
SCLK PIN	0	1	0	1

In uart mode, cs and sclk pins are used as baud rate setting pins.

5.2.2 Format per byte

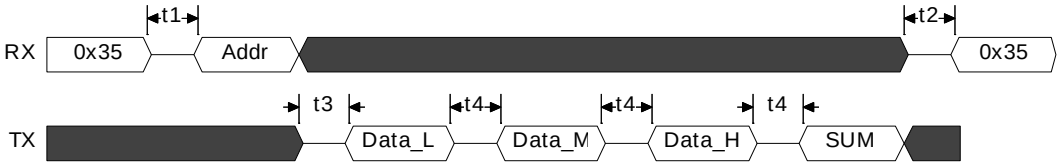


Start bit low level duration t1=208us (4800bps);

The valid data bit time lasts t2=208*8=1664us(4800bps);

Stop bit high level duration t3=2*208u(4800bps)s;

5.2.3 Read timing



The host UART read data sequence is shown in the figure below.The host first sends the command byte (0x35), then the address byte (ADDR) that needs to be read, and then BL6552 sends the data byte in turn, and finally the checksum byte.

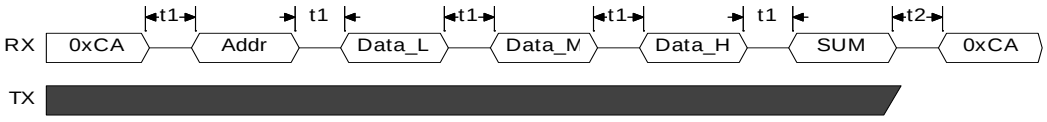
{0x35} is the frame identification byte of the read operation;

Addr is the internal register address of BL6552 corresponding to the read operation (0x00-0xff);

The SUM byte is (Addr+Data_L+Data_M+Data_H)&0xFF reverse;

	Description	Min	Type	Max	Unit
t1	The interval between mcu sending bytes	0		20	mS
t2	Frame interval	0.5			uS
t3	The interval time from the end of MCU sending register address to bl050 sending byte during read operation		110		uS
t4	BL6552 INTERVAL TIME BETWEEN SENDING BYTES		1		Bit

5.2.4 Write timing



The host UART write data sequence is shown in the figure below.The host first sends the command byte (0xCA), then the write address byte (ADDR), then sends the data byte in turn, and finally the checksum byte.

{0xCA} is the frame identification byte of the write operation;

Addr is the internal register address of BL6552 corresponding to the write operation;

The CHECKSUM byte is ((ADDR+Data_L+Data_M+Data_H)& 0xFF) and then inverted by bit.

5.2.5 Protection mechanism of uart interface

1) The UART communication of BL6552 provides a time-out protection mechanism.If the interval between bytes exceeds 18.5mS, the UART interface will automatically reset.
2) If the frame recognition byte is wrong or the checksum byte is wrong, the frame data is abandoned.
3) UART module reset: The RX pin is pulled high after the low level exceeds 32 bps (6.67ms at 4800 bps), and the UART module is reset.

6、 Package information

6.1 order information

BL6552 QFN36 PACKAGE

6.2 Package

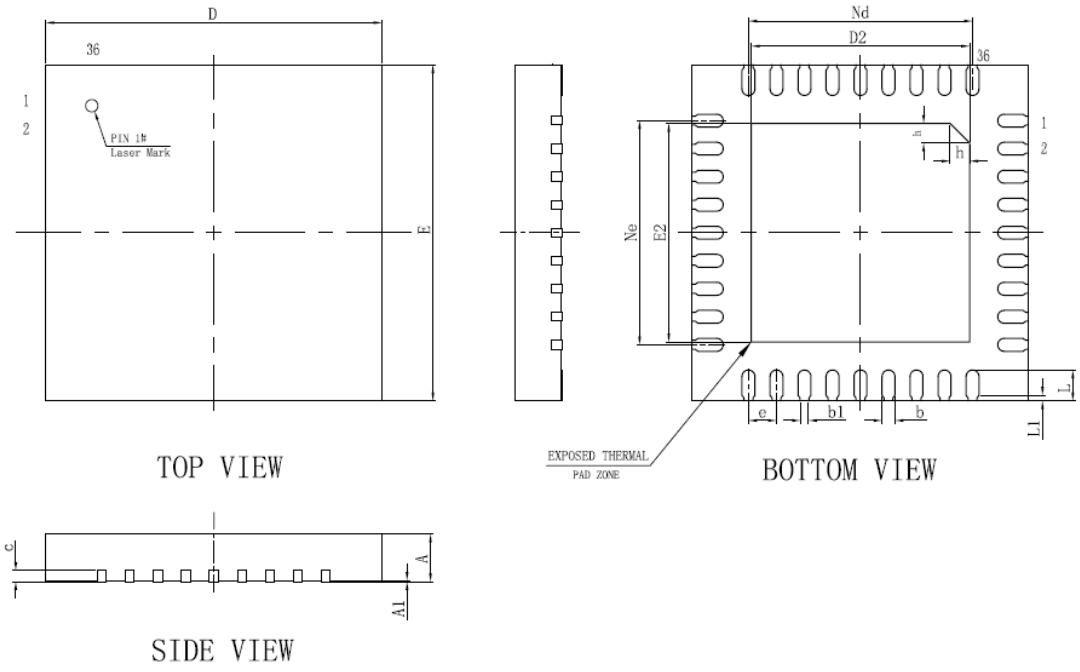
Moisture sensitivity level MSL 3

Warranty Two years

Packing Taping

smallest packaging 4000/reel

Package appearance



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
b1	0.16REF		
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
Nd	3.95	4.00	4.05
e	0.50BSC		
E	5.90	6.00	6.10
E2	3.80	3.90	4.00
Ne	3.95	4.00	4.05
L	0.50	0.55	0.60
L1	0.10REF		
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	181X181		