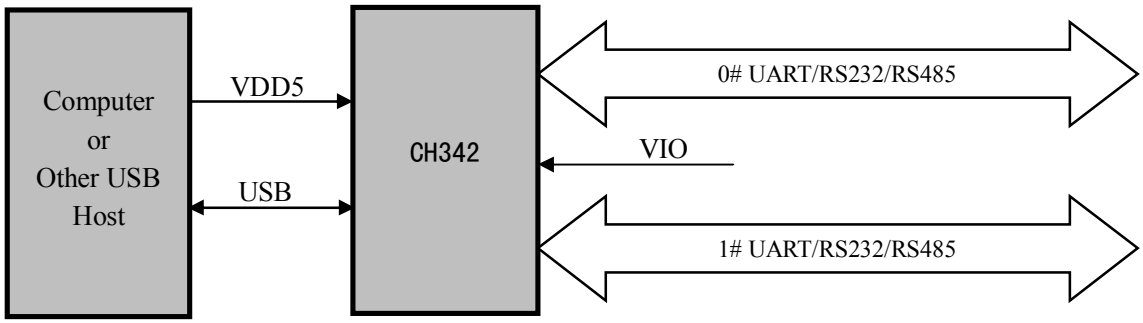
USB to Dual Serial Ports Chip CH342

Datasheet
Version: 1E
http://wch.cn

1. Introduction

CH342 is a USB bus converter chip, which converts USB to dual UART.

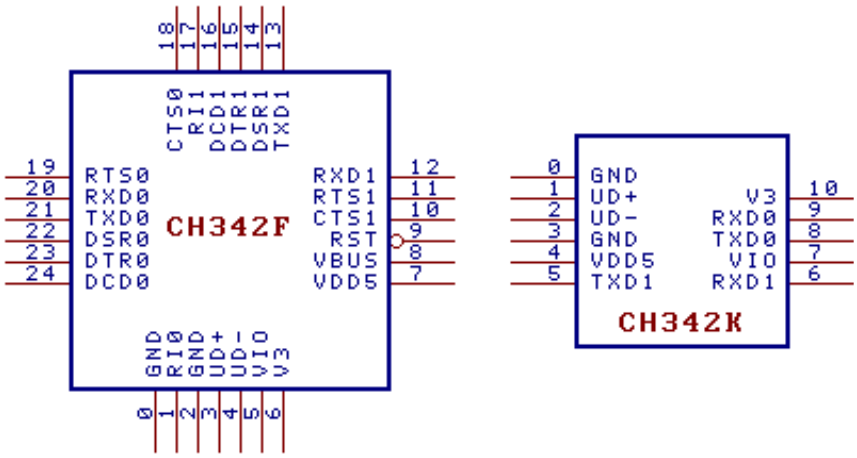
Each UART supports high-speed full-duplex and odd/even parity, provides standard MODEM signals, used to expand serial ports for computer or upgrade directly from normal serial device or MCU to USB bus.



2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating systems.
- Supports free installation OS which built-in CDC driver or multi-functional high-speed VCP vendor driver.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 50bps to 3Mbps.
- UART supports 5, 6, 7 or 8 data bits, supports odd, even, space, mark and none parity.
- Supports common MODEM interface signals RTS, DTR, DCD, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW, used for controlling RS485 to transmit-receive switch.
- Supports RS232 interface, through external voltage conversion chip.
- Supports 5V and 3.3V power supply voltages.
- UART interface I/O powered independently, supports 5V, 3.3V, 2.5V, 1.8V power supply voltages.
- Integrated power-on reset, integrated clock, no external crystal required.
- Built-in EEPROM used to configure the chip of VID, PID, maximum current value, vendor and product information string, etc.
- Integrated Unique ID (USB Serial Number).
- RoHS compliant QFN24, ESSOP10 lead-free package.

3. Packages



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
QFN24_4X4	4*4mm		0.5mm	19.7mil	Square leadless 24-pin patch	CH342F
ESSOP-10	3.9mm	150mil	1.00mm	39mil	Narrow pitch 10-pin patch with bottom plate	CH342K

Note: The backplane of CH342F/CH342K is 0# pin GND, which is an optional but recommended connection; other GND are necessary connections.

The USB transceiver of CH342 is designed according to the built-in design of USB2.0, and it is recommended that no external resistor is in series with UD+ and UD- pins.

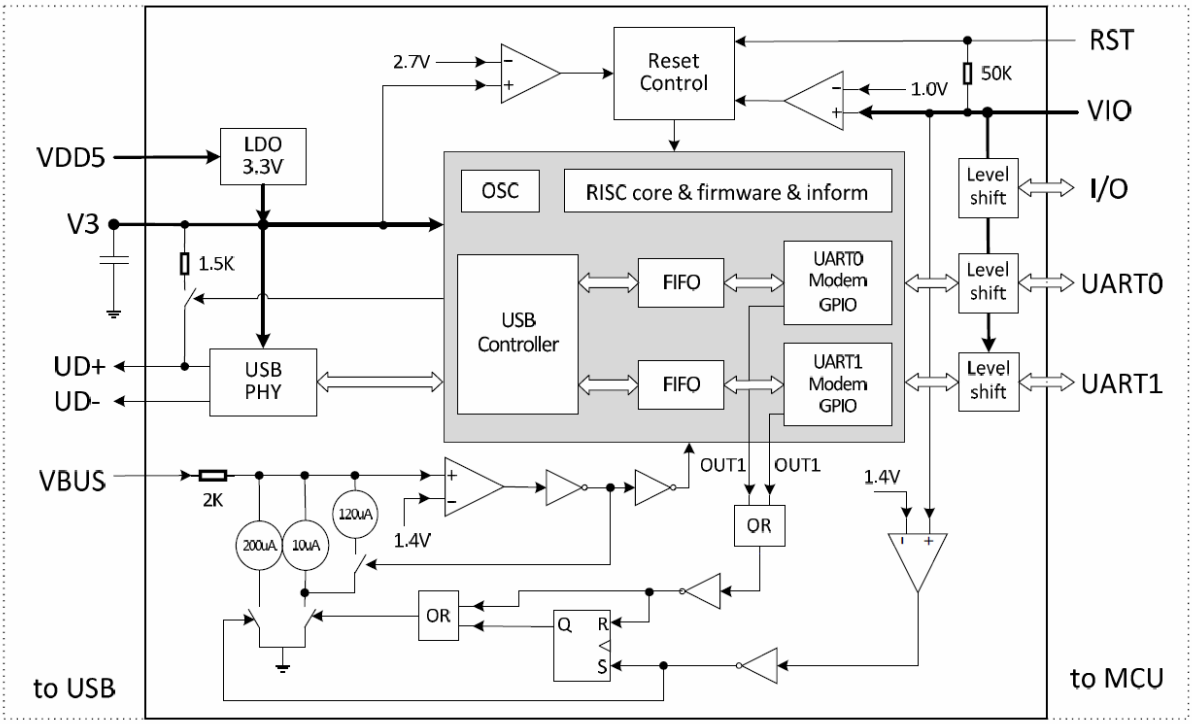
4. Pin definitions

QFN24 Pin No.	ESSOP10 Pin No.	Pin Name	Pin Type	Pin Description
7	4	VDD5	POWER	Power supply voltage input, requires an external decoupling capacitor
5	7	VIO	POWER	I/O Power supply voltage input, requires an external decoupling capacitor
2,0	3,0	GND	POWER	Ground, connected to ground of USB bus directly
6	10	V3	POWER	Internal power regulator output and core and USB power input, When VDD5 voltage is less than 3.6V, connect VDD5 to input the external power supply, an external power decoupling capacitor is required to be connected when the VDD5 voltage is greater than 3.6V
9	NONE	RST	IN	Input of external reset, active low, built-in pull-up resistor
3	1	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistors
4	2	UD-	USB signal	Connect to USB D- Signal directly, do not series resistors
8	NONE	VBUS	IN	VBUS status detection input of USB bus, intergrated

				pull-down resistor
21	8	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
20	9	RXD0	IN	Receive asynchronous data input of UART0, built-in pull-up resistor
18	NONE	CTS0	IN	UART0 MODEM input signal, clear to send, active low
22	NONE	DSR0	IN	UART0 MODEM input signal, data set ready, active low
1	NONE	RI0	IN	UART0 MODEM input signal, ring indicator, active low
24	NONE	DCD0	IN	UART0 MODEM input signal, data carrier detect, active low
23	NONE	DTR0 TNOW0	OUT	UART0 MODEM input signal, data terminal ready, active low If an external pull-down resistor is detected during power-on, it will switch to UART0 sends ongoing status indication, active at high level
19	NONE	RTS0	OUT	UART0 MODEM input signal, request to send, active low
13	5	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
12	6	RXD1	IN	Receive asynchronous data input of UART1, built-in pull-up resistor
10	NONE	CTS1	IN	UART1 MODEM input signal, clear to send, active low
14	NONE	DSR1 TNOW1	IN	UART1 MODEM input signal, data set ready, active low If DTR1 detects an external pull-down resistor during power-on, and DSR1 detects a low level (external pull-down), DSR1 will switch to the ongoing status indication sent by the UART1, active at high level
17	NONE	RI1	IN	UART1 MODEM input signal, ring indicator, active low
16	NONE	DCD1	IN	UART0 MODEM input signal, data carrier detect, active low
15	NONE	DTR1 TNOW1	OUT	UART1 MODEM input signal, data terminal ready, active low If DTR1 detects an external pull-down resistor during power-on, and DSR1 detects a high level (internal pull-up), DTR1 will switch to the ongoing status indication sent by the UART1, active at high level
11	NONE	RTS1	OUT	UART1 MODEM input signal, request to send, active low
NONE	NONE	ACT#	OUT	USB configuration completed state output, active low, invalid when suspended

5. Function descriptions

5.1. Internal structure



5.2. Power and power consumption

CH342 has 3 power supplies and an intergrated voltage regulator which generates 3.3V.VDD5 is the input power regulator .V3 is the output of the voltage regulator and USB transceiver and core power supply input, and VIO is the I/O pin power supply.

CH342 supports 5V or 3.3V supply voltage, and the V3 pin should be externally connect to a power decoupling capacitor with a capacity of about 0.1uf. When using 5V power supply (greater than 3.8V), VDD5 inputs external 5V power supply (for example, the USB bus power supply), the internal voltage regulator generates 3.3V on V3 which used by USB transceivers. When using 5V power supply (greater than 3.8V), VDD5 inputs external 5V power supply (for example, the USB bus power supply), the internal voltage regulator generate 3.3V on V3 which used by USB transceivers. When using 3.3V power supply. V3 still requires an external decoupling capacitor.

VIO pin of CH342 provides I/O power for dual serial port I/O and RST pin. It support 1.8V~5V power supply voltage. VIO should use the same power supply as MCU and other peripherals. UD+, UD- and VBUS pins use V3 power supply, not VIO power supply.

CH342 automatically supports USB device suspension to save power consumption. In the USB suspend state, if the I/O output pin has no external load and the I/O input pin is float (internally pulled up) or in a high level state, the VIO power supply will not consume current. In addition, when V3 and VDD5 lose power and are at a voltage of 0V, the current consumption of VIO is the same as above, and VIO will not flow current backwards to VDD5 or V3.

VBUS should be connected to USB power supply, and when the loss of USB power is detected, CH342 will turn off the USB and sleep (suspend). The CH342K/J chip has no VBUS pin, so it is assumed that there is always a USB power supply.The intergrated pull-down resistor of the VBUS pin can be controlled by the computer software by setting the OUT1 signal in the serial port MCR register (SERIAL_IOC_MCR_OUT1). When OUT1 is invalid, the pull-down resistor will be turned on (default status). When OUT1 is valid, the pull-down resistor will be turned off.

When the VBUS pin is connected with a resistor in series and then used to control the VIO power supply through PMOS, CH342 will provide a VIO low voltage protection mechanism. During the period when the

VBUS pull-down resistor is turned off, if the VIO voltage is detected to be lower than about 1.4V, the CH342 will automatically absorb about 300uA discharge current at the VBUS pin until the VIO voltage rises to end the discharge current and automatically turn on the pull-down resistor.

The following are several power connection schemes for reference.

<table>
<tr><td rowspan="2">Power supply scheme</td><td>UART signals voltage</td><td>VDD5 pin</td><td>V3 pin</td><td>VIO pin</td><td>MCU or peripheral power supply</td></tr>
<tr><td>MCU operating voltage</td><td>No lower than V3pin's voltage</td><td>Rated voltage: about 3.3 V</td><td colspan="2">Both use the same power supply 1.8V~5V</td></tr>
<tr><td rowspan="4">All USB Power Supply</td><td>5V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">USB power supply 5V</td></tr>
<tr><td>3.3V</td><td>USB power supply 5V</td><td>External capacitor</td><td colspan="2">Powered by V3 for 3.3V, up to 10 mA</td></tr>
<tr><td>3.3V</td><td colspan="4">USB 5V power stepped down to 3.3V via external LDO power regulator, V3 connects to external capacitor.</td></tr>
<tr><td>1.8V～4V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">The USB power supply is reduced in voltage through an external LDO regulator</td></tr>
<tr><td>USB+ self-supply dual power supplies</td><td>1.8V～5V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">Self-powered 1.8V～5V (1.8V,2.5V,3.3V,5V)</td></tr>
<tr><td rowspan="2">All Self-powered</td><td>4V～5V</td><td>Self-powered 4V- 5V</td><td>Only connected to the capacitor</td><td colspan="2">Self-powered 4V- 5V</td></tr>
<tr><td>1.8V～5V</td><td colspan="2">Self-powered, rated voltage 3.3V, external capacitor</td><td colspan="2">Self-powered 1.8V～5V</td></tr>
</table>

5.3. UART

The pins of CH342 in asynchronous serial port mode include: data transmission pins, MODEM control signal pins and auxiliary pins.

Data transmission pins include: TXD pin and RXD pin. When the serial port input is idle, RXD will be at high level. When the serial port output is idle, TXD will be at high level.

The MODEM contact signal pins include: CTS pin, DSR pin, RI pin, DCD pin, DTR pin and RTS pin. All these MODEM control signals are controlled by the computer application program and their purposes can be defined.

The DTR0 pin of the CH342 is used as a configuration input pin during power-on or reset. It can be connected to a 4.7KΩ (3～8KΩ) pull-down resistor to generate a default low level to make the serial port enter half-duplex mode and switch the original DTR0 pin to TNOW0 output pin, for indicating that the UART0 is sending data. In half-duplex mode, TNOW0 can be used to directly control the receiving and transmitting switch of RS485 transceiver.

The DTR1 pin of CH342 is used as a configuration input pin during power-on or reset. It can be connected to a 4.7KΩ (3～8KΩ) pull-down resistor to generate a default low level, so that the UART1 will enter the half-duplex mode. If DSR1 detects a high level (the default pull-up resistor is provided internally), DTR1 will be switched to the TNOW1 output pin; if DSR1 detects a low level (a 4.7KΩ pull-down resistor is connected externally), and DSR1 will be switched to the TNOW1 output pin. TNOW1 is used for indicating that the UART1 is sending data. Refer to TNOW0 for the functions of TNOW1.

Auxiliary pins include: ACT# pins. The ACT# pin is the status output of the USB device configuration completion, which can be used to notify the MCU or drive the LED connected to the VIO after the current limiting resistor is connected in series.

The asynchronous serial port of CH342 supports CTS and RTS hardware automatic flow control, which can be enabled by software. If enabled, the serial port will continuously send the next data only when it detects that the CTS pin input is valid (active at low level). Otherwise, the serial port transmission will be suspended; when the receiving buffer area is null, the serial port will automatically validate RTS pin (active at low level), and the serial port will automatically invalidate the RTS pin until the data in the receiving buffer area is full, and the RTS pin will be validated again when the buffer area is null. Using hardware automatic rate control, you can connect your own CTS pin to the other party's RTS pin and can connect your own RTS pin to the other party's CTS pin.

CH342 has intergrated separate transmit-receive buffer and supports simplex, half-duplex or full duplex asynchronous serial communication. Serial data includes 1 low-level start bit, 5, 6, 7 or 8 data bits, 1 or 2 high-level stop bits, and supports odd/even/mark/blank checking. CH342 supports common communication baud rates: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M and 3M, etc.

In applications with high communication baud rate, it is recommended to enable hardware automatic flow control. The full-speed USB is only 12Mbps. Considering the factors such as protocol overhead, two serial ports should not be simultaneously in a continuous or full-duplex high-speed communication status of 1Mbps and above in the practical applications.

The allowable baud rate error of the CH342 serial port receiving signal should not be more than 2%, and the baud rate error of the serial port transmitting signal should be less than 1.5%.

In the Windows operating system of the computer, CH342 supports the CDC drive program that comes with the system. The high-speed VCP vendor drive program can be also installed to simulate the standard serial ports, so most of serial port applications are fully compatible and usually no any modification is required.

CH342 can be used to upgrade the original serial peripheral device, or to add additional serial ports to the computer through the USB bus. RS232, RS485, RS422 and other interfaces can be further provided through the external level conversion device.

5.4. Clock, reset and others

CH342 has the intergrated USB pull-up resistors, and the UD+ and UD- pins should be directly connected to the USB bus.

CH342 has the intergrated power-on reset circuit. CH342F chip also provides an external reset input pin active at low level. When the RST pin is at low level, the CH342 chip will be reset; when the RST pin returns to a high level, the internal reset delay of CH342 will last for about 15mS. Then, enter the normal operating status.

CH342 has an intergrated low-voltage reset circuit. It monitors the voltages of the V3 pin and the VIO pin at the same time. When the V3 voltage is lower than VRV3 or the VIO voltage is lower than VRVIO, the chip will be automatically reset by hardware.

CH342 has an intergrated clock generator, without external crystal and oscillation capacitor.

In large batch applications, the manufacturer identification code VID and product identification code PID of CH342 and product information can be customized.

5.5. Parameter configuration

In larger batch applications, the vendor VID and product identification PID of CH342 and product information can be customized.

In less batch applications, it can use CH342F that built-in EEPROM (The last 4th digit of the batch number is a letter, then the built-in EEPROM). After user installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, it can be flexibly configured the vendor VID, product identification PID, maximum current, BCD version number, vendor information and product information string descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

(Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage temperature	-55	105	℃
VDD5	USB supply voltage (VDD5 pin power supply, GND pin grounded)	-0.5	6.0	V
VIO	Serial port I/O supply voltage (VIO pin power supply, GND pin grounded)	-0.5	6.0	V
VVBUS	Voltage on the VBUS pin	-0.5	6.5	V
VUSB	Voltage on the USB signals pin	-0.5	V3+0.5	V
VUART	Voltage on the serial port and other pins	-0.5	VIO+0.5	V

6.2. Electrical characteristics

(Test conditions: TA=25℃, VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V, excluding USB pins)

Name	Parameter description			Min	Typ	Max	Unit
VDD5	USB Power supply voltage	V3 pin is not connected to VDD5 and V3 is connected to the capacitor		4.0	5	5.5	V
		V3 pin is connected to VDD5, VDD5=V3		3.0	3.3	3.6	
VIO	VIO supply voltage on the serial port and other I/O			1.7	5	5.5	V
IVDD	VDD5 or V3 supply current during operation				3	15	mA
IVIO	VIO supply current during operation				0	10	mA
ISLP	Operating Supply Current(USB Suspend)	VDD5 power supply =5V			0.09	0.16	mA
		VDD5=V3 power supply=3.3V			0.005	0.015	mA
		VIO power supply, no I/O load/ pull-up			0.002	0.05	mA
ILDO	External load capacity of internal power regulator					10	mA
VIL	Low level input voltage		VIO=5V	0		1.5	V
			VIO=3.3V	0		0.9	V
			VIO=1.8V	0		0.5	V
VIH	High level input voltage		VIO=5V	2.5		VIO	V
			VIO=3.3V	1.9		VIO	V

		VIO=1.8V	1.3		VIO	V
VIHVBS	High level voltage of VBUS pin	VIO=1.8V～5V	1.7		5.8	V
VOL	Low level Output voltage	VIO=5V, drawing 15mA current		0.4	0.5	V
		VIO=3.3V, drawing 8mA current		0.3	0.4	V
		VIO=1.8V, drawing 3mA current		0.3	0.4	V
VOH	High level Output voltage Non-reset status	VIO=5V, output 10mA current	VIO-0.5	VIO-0.4		V
		VIO=3.3V, output 5mA current	VIO-0.4	VIO-0.3		V
		VIO=1.8V, output 2mA current	VIO-0.4	VIO-0.3		V
IPUP	Serial port and RST pin pull-up current (Pulled up to VIO voltage)	VIO=5V	35	150	220	uA
		VIO=3.3V	15	60	90	uA
		VIO=1.8V	3	14	21	uA
IPDN	Pull-down current of VBUS pin	VBUS>1.6V	6	10	16	uA
		VBUS<1.3V	50	140	200	uA
VRV3	Power-on reset / low-voltage reset voltage threshold of V3 power		2.5	2.7	2.9	V
VRVIO	Low-voltage reset voltage threshold of VIO power		0.8	1.0	1.15	V
VESD	HBM ESD withstand voltage on USB or I/O pin		5	6		KV

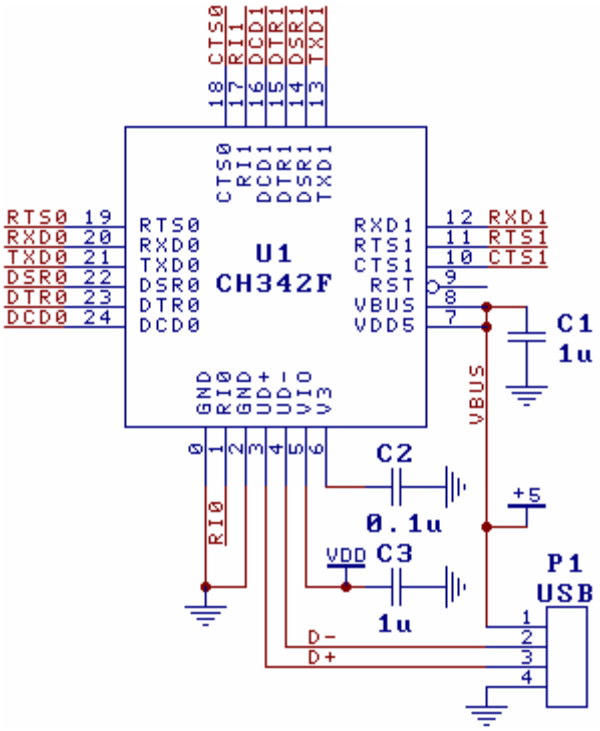
6.3. Timing parameters

(Test Conditions: TA=25℃, VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V)

Name	Parameter description		Min	Typ	Max	Unit
FD	Error of internal clock (Comparative influenced baud rate)	TA=-15℃～60℃	-1.0	±0.5	+1.0	%
		TA=-40℃～85℃	-1.5	±0.8	+1.5	%
TRSTD	Reset delay after power-on or external reset input		9	15	25	mS
TRI	Effective signal width of RST external reset input		100			nS
TSUSP	USB automatic suspend time		3	5	9	mS
TWAKE	Wake-up completion time after chip sleep		1.2	1.5	5	uS

7. Applications

7.1. USB to dual 9-Line TTL UART (Figure below)



The figure above shows the USB to dual TTL serial ports realized by CH342F. The signal wires in the figure can only be connected to RXD, TXD and the common ground wire. Other signal lines can be selected as needed, and can be suspended when not needed.

P1 is a USB port. The USB bus includes a pair of 5V power lines and a pair of data signal lines. Generally, the +5V power line is red, the ground line is black, the D+ signal line is green, and the D- signal line is white. The supply current provided by the USB bus can reach 500mA, and the VBUS pin detects the USB power supply status here.

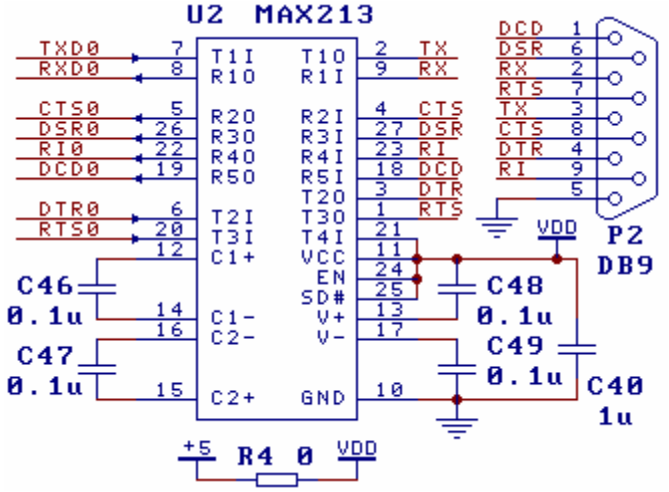
Three power supply schemes: Firstly, all USB power supplies; USB bus is directly used to provide 5V power supply for CH342 chip and USB products, i.e., 5V power for VDD5=VBUS=USB, 5V for VIO=VMCU=USB or 1.8V～4V after voltage reduction; secondly, separate and independent power supply; the self-supplied standing power VDD is used for VIO of CH342 and the MCU of the product together, and the USB power is used for CH342. VDD5 is connected to the USB power VBUS, i.e., 5V power of VDD5=VBUS=USB, and the power of VIO=VMCU=VDD=self-supplied 1.8V-5V; thirdly, all self-supplied powers; the USB power is only detected but not used. USB product provides standing power VDD through selfsupply; mainly two types: VDD5=VIO=VMCU=VDD=self-supply 5V orVDD5=V3=VIO=VMCU=VDD= self-supply 3.3V.

Capacitor C2 of V3 pin is 0.1uF, and is used for the decoupling of the internal 3.3V power supply node decoupling of CH342, and C1 and C3 are used for the decoupling of the external power supply.

For CH342F, if VIO has been short-circuited with V3 in the application, then capacitor C3 can be omitted.

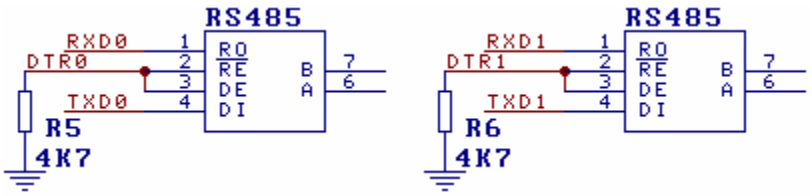
It should be noticed that the decoupling capacitors C1, C2 and C3 should be as close as possible to the connected pins of CH342 when the printed circuit board PCB is designed; the D+ and D- signal lines should be close to parallel wiring, and ground wire or covered copper should be provided on both sides to reduce the external signal interference;

7.2. USB to dual 9-Lines RS232 UART (Figure below)



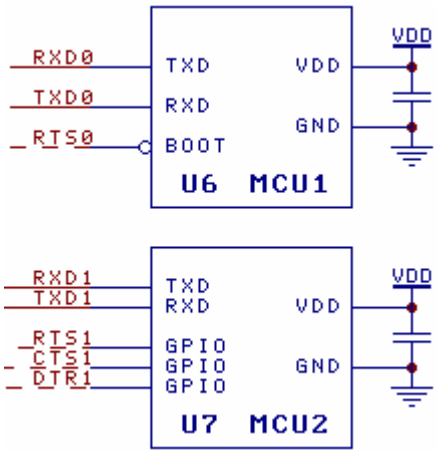
CH342F provides common UART signals and MODEM signals. In the figure, one path of TTL serial port is converted to RS232 serial port through the external level conversion circuit U2. The other path is similar. Port P2 is a DB9 pin, and its pins and functions are the same as those of the ordinary 9-pin serial port of the computer. The similar models of U2 include MAX213/ADM213/SP213/MAX211. USB bus uniformly supplies power to U2 in the figure through R4.

7.3. USB to dual RS485 UART (Figure below)



In the figure, the DTR pin is externally connected to the pull-down resistor, so as to switch to the TNOW pin, which is used to control the DE (high active transmission enabling) and RE# (low active transmission enabling) pins of the RS485 transceiver. The RS485 transceiver and VIO should share the same power.

7.4. Connection to dual MCU UART to supply power respectively (Figure below)



The figure above shows the reference circuit of MCU connected to CH342 chip through two TTL serial ports to realize USB communication under dual power supply mode. CH342 is powered by USB bus. Another self-supplied power VDD is used for VBUS, MCU1, MCU2 and VIO. VDD supports 5V, 3.3V, 2.5V and 1.8V.

If UART speed is high, then MCU2 can realize hardware automatic flow control through CTS1 and RTS1 with reference to the figure above.

If necessary, VBUS (OUT1) can also be used to control PMOS power switch for supplying power to MCU from the USB power, as shown in the following figure: +5 is USB power supply, VDD is VIO power supply and MCU power supply of CH342. By default, the pull-down resistor of VBUS is turned on to generate a pull-down current, so that the PMOS grid electrode has enough voltage for switching on, and VBUS supplies power to VIO. After RTS and DTR are set in the computer software, it is valid when OUT1 is set. Then, the pull-down resistor of VBUS will be turned off, so that the grid electrode of PMOS will lose voltage and be turned off. Eventually, VIO voltage drop leads to the MCU low voltage reset. When VIO voltage drops to about 1.4V, VIO low-voltage protection mechanism will be triggered, VBUS will automatically sink the pull-down current and recover the pull-down resistor, so that the PMOS will be turned on again and VIO will be restored to supply power. VIO voltage drop and MCU reset are realized in the whole process. LED D1 is used to prevent VBUS voltage from being too low. In addition, connecting a diode in series between Q1 and VDD can prevent VDD from flowing back to +5.