PRELIMINARY DATASHEET

CGY2131UH

500mW 39-44 GHz Power Amplifier

DESCRIPTION

The CGY2131UH is a PHEMT GaAs Power Amplifier with output power of 27dBm (500mW) and more than 22dB of gain over the frequency range 39 to 44 GHz.

The 1dB compression point is 26 dBm with excellent linearity delivering an OIP3 of 34.5 dBm. DC power supply is typically 4.5V and PAE is above 15%

The CGY2131UH is manufactured using the D01PH GaAs PHEMT power process from OMMIC. This process has a 130nm gate length with a Ft of 110Ghz and a Fmax of 180GHz.

The D01PH process used to manufacture the MMIC have been evaluated by ESA and is in the EPPL (European Preferred Part List). This very reliable process is suitable to manufacture power amplifiers dedicated to flight models in aerospace applications as well as high perfromance power amplifiers for terrestrial applications.

APPLICATIONS

- High performance GaAs Power Amplifier
- Earth-to-space or point-to-point radiolinks
- Backhaul networks
- Telecommunications
- RF Driver for High Power Amplifiers

FEATURES

- Usable frequency range from 39 to 44 GHz
- Psat > 500mW (27dBm)
- P1dB ~ + 26dBm
- Gain ~ + 22dB
- 50 Ohms input and output matched
- Delivered as 100 % on-wafer RF tested dies
- Samples and evaluation Boards Available
- Die size is 3.07 x 1.86 mm

The MMIC is available in the die form, OMMIC can deliver packaged version of the component.

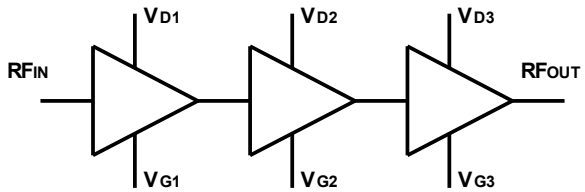

Figure 1: CGY2131 Power Amplifier block diagram

RoHS Compliant

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MAXIMUM VALUES

T_{amb} = + 25 °C, at Die backside; backside grouded, unless otherwise specified.

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{G1}, V_{G2}, V_{G3}	Gate voltage	V_{D1}, V_{D2}, V_{D3} left open	- 2.5	0	V
V_{D1}, V_{D2}, V_{D3}	Drain voltage	V_{G1}, V_{G2}, V_{G3} left open	0	+ 6	V
I_{D1}	Drain current	$V_{D1,2,3}$ = 4.5V and $V_{G1,2,3}$ = -0,3V		200	mA
I_{D2}				350	
I_{D3}				500	
P_{IN}	Input power			+ 10	dBm
T_{amb}	Ambient temperature		- 40	+ 85	° C
T_j	Junction temperature			+ 175	° C
T_{stg}	Storage temperature		- 55	+ 85	° C

Operation of this device outside the parameter ranges may cause permanent damage

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	UNIT
$R_{th\ (j-a)}$	Thermal resistance from junction to ambient (DC at T_{amb} max)	TBD	° C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
RF_{in}	Input frequency		39		44	GHz
Performances on Reference Board at f_i = 42 GHz						
$V_{D1,2,3}$	Supply voltage			4,5		V
I_{DD}	Total Supply current @Psat	$V_{G1,2,3}$ = - 0,3V		800		mA
G	Gain	$V_{G1,2,3}$ = - 0,3V		+ 20		dB
NF	Noise Figure			TBD		dB
P1dB	1dB compression point	$V_{G1,2,3}$ = - 0,3V		+ 26		dBm
Psat	Saturated power	$V_{G1,2,3}$ = - 0,3V		+ 27,5		dBm
PAE	Power Added Efficiency	$V_{G1,2,3}$ = - 0,3V RF_{IN} = + 10 dBm		16		%
OIP3	Output third order intercept point	I_{D3} = 350 mA		+ 34,5		dBm
IMD3	2 Carriers 14 dB below P1dB			- 44		dBc
ISO_{rev}	Reverse Isolation	RF_{OUT} / RF_{IN}		- 43		dB
S_{11}	Input reflection coefficient	50 Ohms		- 6		dB
S_{22}	Output reflection coefficient	50 Ohms		- 9		dB
P_{OFF}	Leakage when HPA off	RF_{IN} = + 10 dBm $V_{G1,2,3}$ = - 2.5V		- 30		dBm

(*) Measurement reference planes are the INPUT and OUTPUT coaxial connectors.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

On-Wafer measurements is the standard way of performing device testing but have inherently poor thermal conditions. Tests are performed under full biasing conditions and CW operation which combined with poor thermal conditions give a lower gain and P1dB compared to the MMIC's real performances with a good thermal heatsink..

S-PARAMETERS (SMITH CHARTS)

Conditions : V_{D1} = V_{D2} = V_{D3} = 4.5V, V_{G1} = V_{G2} = V_{G3} = -0.3V, (I_{DQ1} = 100mA, I_{DQ2} = 190mA, I_{DQ3} = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)

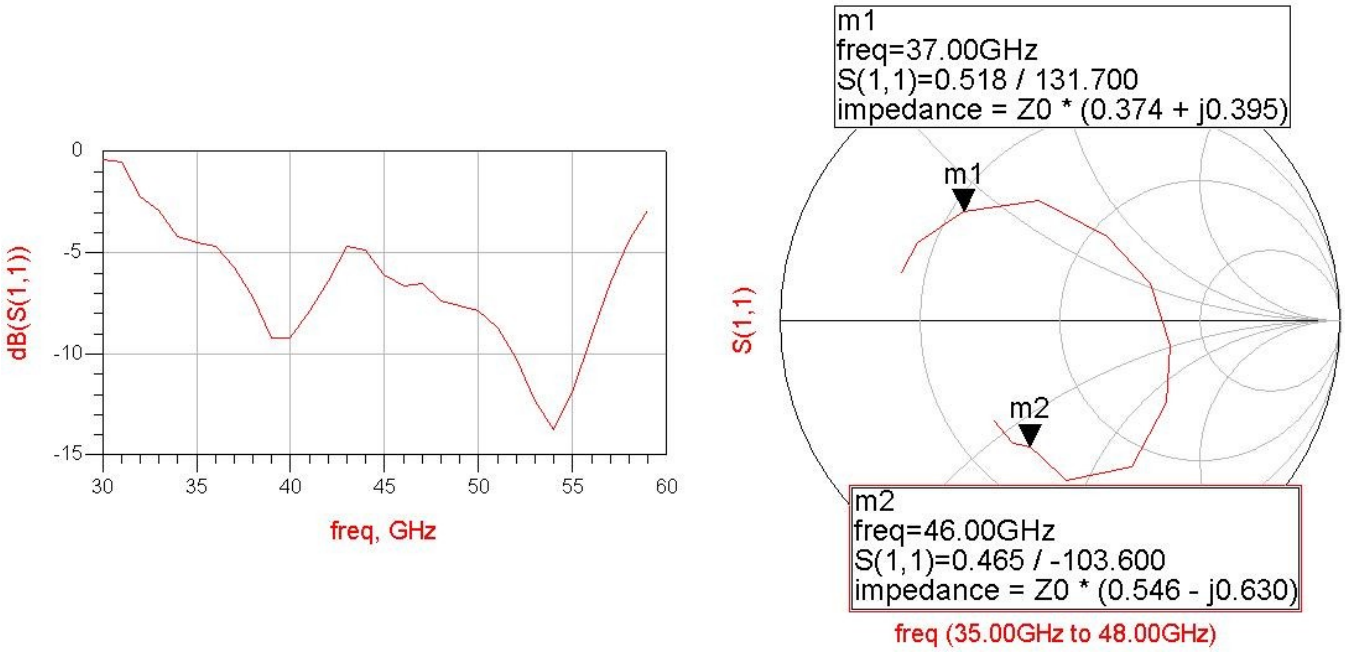

Figure 2: S11 parameter On Wafer measurements

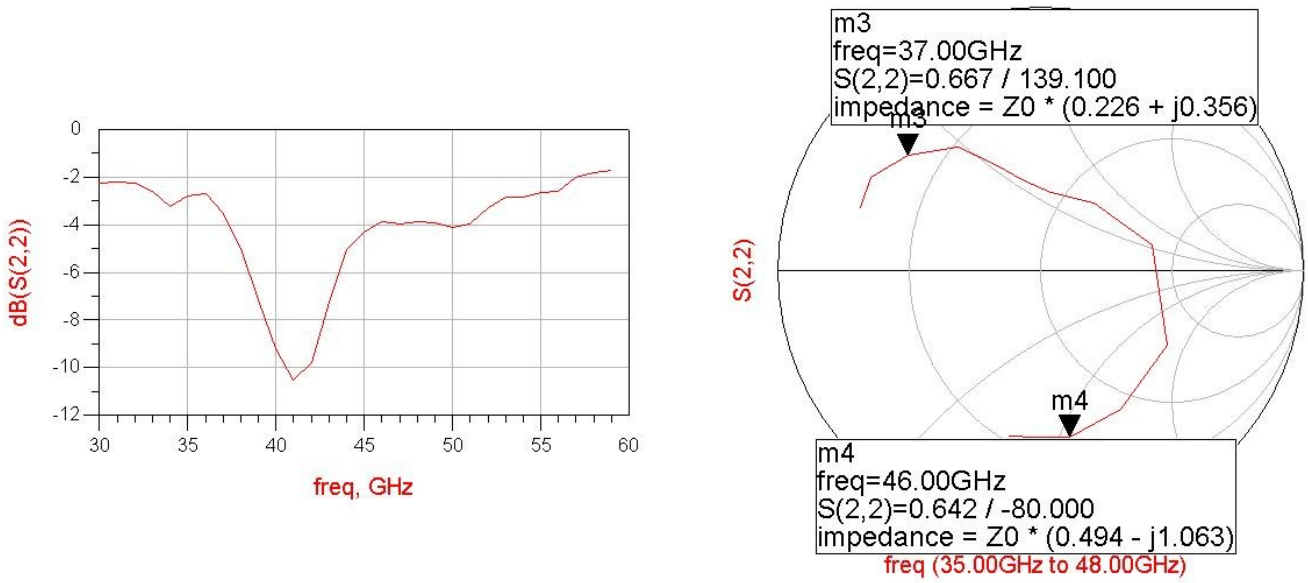

Figure 3: S22 parameter On Wafer measurements

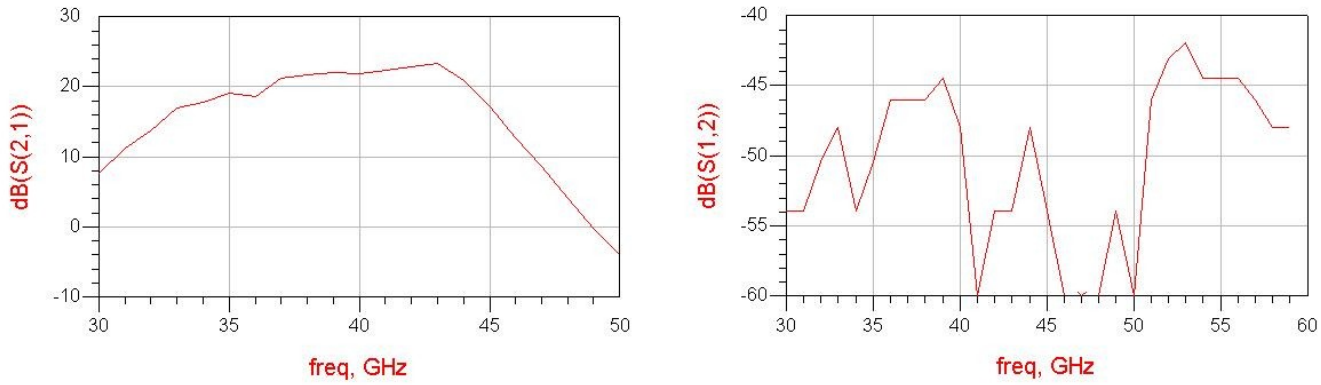

Figure 4: S21 and S12 parameter On Wafer measurements

S-PARAMETERS (TABLE)

Conditions : V_{D1} = V_{D2} = V_{D3} = 4.5V, V_{G1} = V_{G2} = V_{G3} = -0.3V, (I_{DQ1} = 100mA, I_{DQ2} = 190mA, I_{DQ3} = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)

GHz	|S11|	S11 Phase	|S21|	S21 Phase	|S12|	S12 Phase	|S22|	S22 Phase
30.0	0.954	-161.7	2.385	54.9	0.0020	131.5	0.772	-179.9
31.0	0.941	-171.5	3.610	25.2	0.0022	99.8	0.777	176.9
32.0	0.772	179.0	4.814	-10.4	0.0029	104.4	0.770	171.7
33.0	0.713	173.2	6.982	-53.9	0.0043	104.1	0.740	162.5
34.0	0.618	166.4	7.745	-90.2	0.0025	67.1	0.690	167.6
35.0	0.594	163.0	8.954	-137.0	0.0031	49.9	0.724	161.0
36.0	0.581	151.6	8.541	-175.7	0.0046	47.7	0.735	151.3
37.0	0.518	131.7	11.495	148.1	0.0054	62.3	0.667	139.1
38.0	0.436	100.4	12.162	99.6	0.0055	19.3	0.562	123.8
39.0	0.345	61.1	12.546	58.2	0.0065	-9.9	0.439	113.3
40.0	0.346	22.1	12.431	15.4	0.0045	-45.5	0.347	100.6
41.0	0.403	-12.8	13.122	-28.1	0.0011	-26.3	0.298	82.4
42.0	0.479	-37.8	13.756	-74.9	0.0021	34.6	0.324	51.4
43.0	0.582	-63.7	14.504	-132.9	0.0025	-10.4	0.434	12.6
44.0	0.572	-88.1	10.977	166.5	0.0037	-27.5	0.561	-30.6
45.0	0.494	-97.9	7.137	110.1	0.0024	-37.6	0.610	-60.2
46.0	0.465	-103.6	4.305	68.7	0.0015	-97.9	0.642	-80.0
47.0	0.470	-111.1	2.698	26.7	0.0005	-116.0	0.632	-91.7
48.0	0.427	-124.2	1.594	-2.2	0.0010	106.5	0.642	-101.2
49.0	0.415	-126.0	0.956	-33.2	0.0018	42.2	0.637	-106.1
50.0	0.403	-135.9	0.632	-57.8	0.0007	-28.5	0.622	-116.5
51.0	0.366	-148.5	0.449	-84.1	0.0052	82.2	0.632	-105.4
52.0	0.307	-166.9	0.235	-109.4	0.0066	34.6	0.686	-111.2
53.0	0.242	165.6	0.269	-139.2	0.0082	5.6	0.723	-115.8
54.0	0.205	127.8	0.148	-158.0	0.0055	-2.2	0.720	-118.8
55.0	0.254	75.7	0.144	162.7	0.0059	-36.1	0.737	-121.5
56.0	0.354	40.3	0.094	142.8	0.0055	-23.9	0.743	-123.5
57.0	0.474	16.0	0.024	113.2	0.0052	-55.4	0.792	-127.2
58.0	0.602	-3.5	0.031	34.9	0.0037	-45.4	0.810	-129.6
59.0	0.713	-16.3	0.022	167.3	0.0039	-43.4	0.823	-134.9

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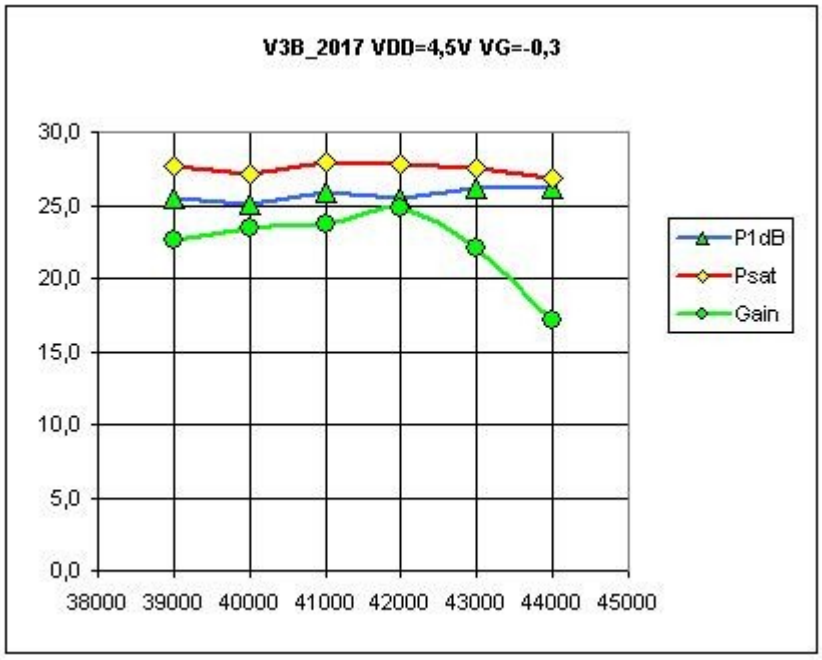
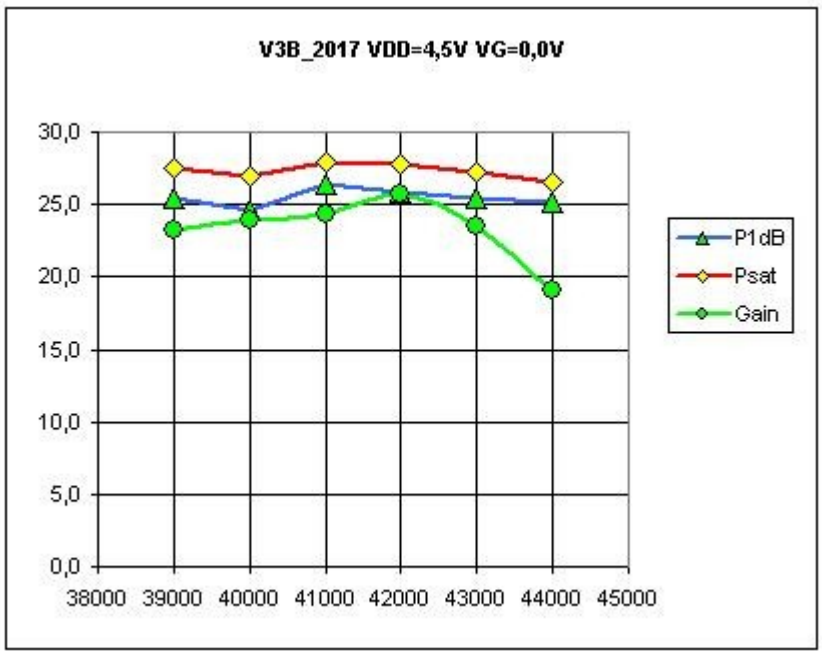
1DB COMPRESSION POINT, SATURATED POWER AND GAIN

Conditions : $V_{D1} = V_{D2} = V_{D3} = 4.5V$, $V_{G1} = V_{G2} = V_{G3} = -0.3V$, ($I_{DQ1}$ = 100mA, I_{DQ2} = 190mA, I_{DQ3} = 280 mA), T_{amb} = + 25°C (On-Wafer measurements)



Conditions : $V_{D1} = V_{D2} = V_{D3} = 4.5V$, $V_{G1} = V_{G2} = V_{G3} = 0.0V$, ($I_{D1}$ = 170mA, I_{D2} = 310mA, I_{D3} = 430 mA), T_{amb} = + 25°C (On-Wafer measurements)



APPLICATION SCHEMATICS

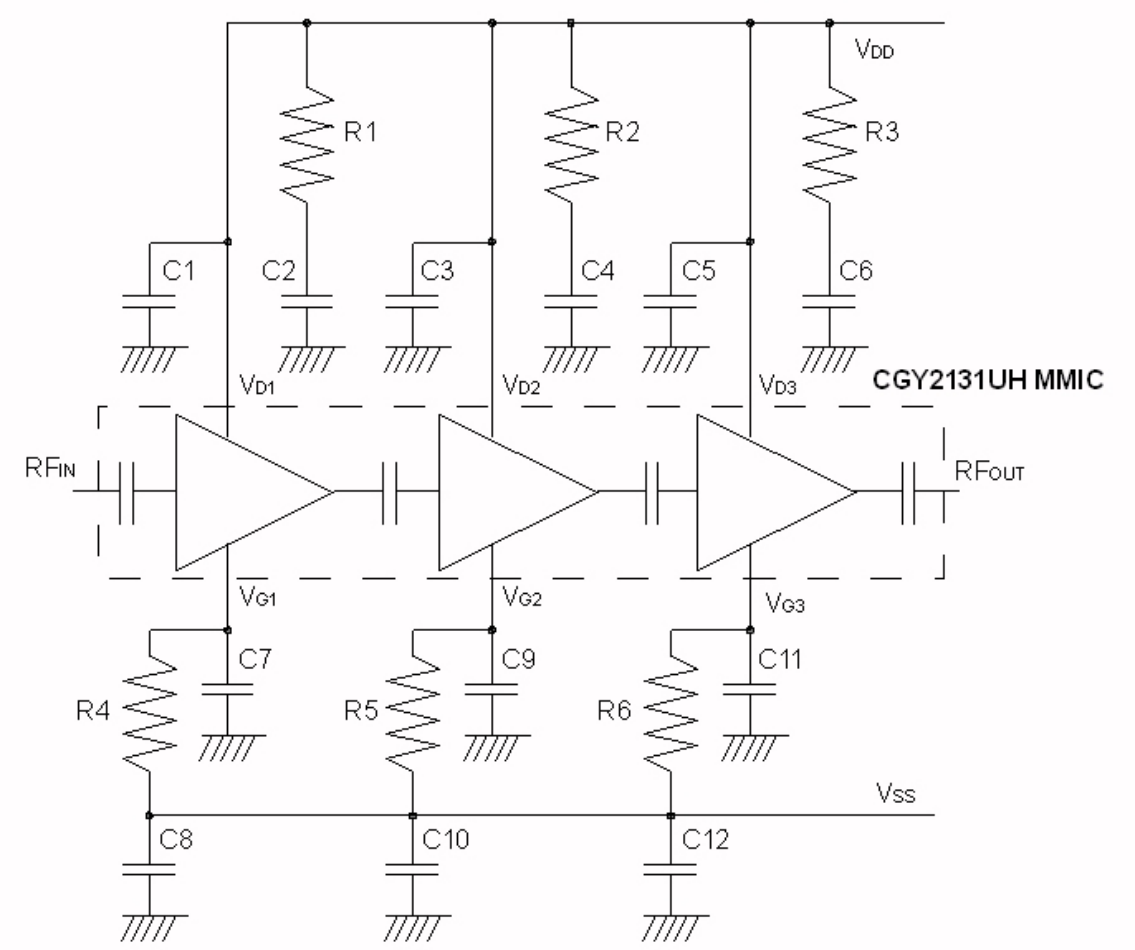


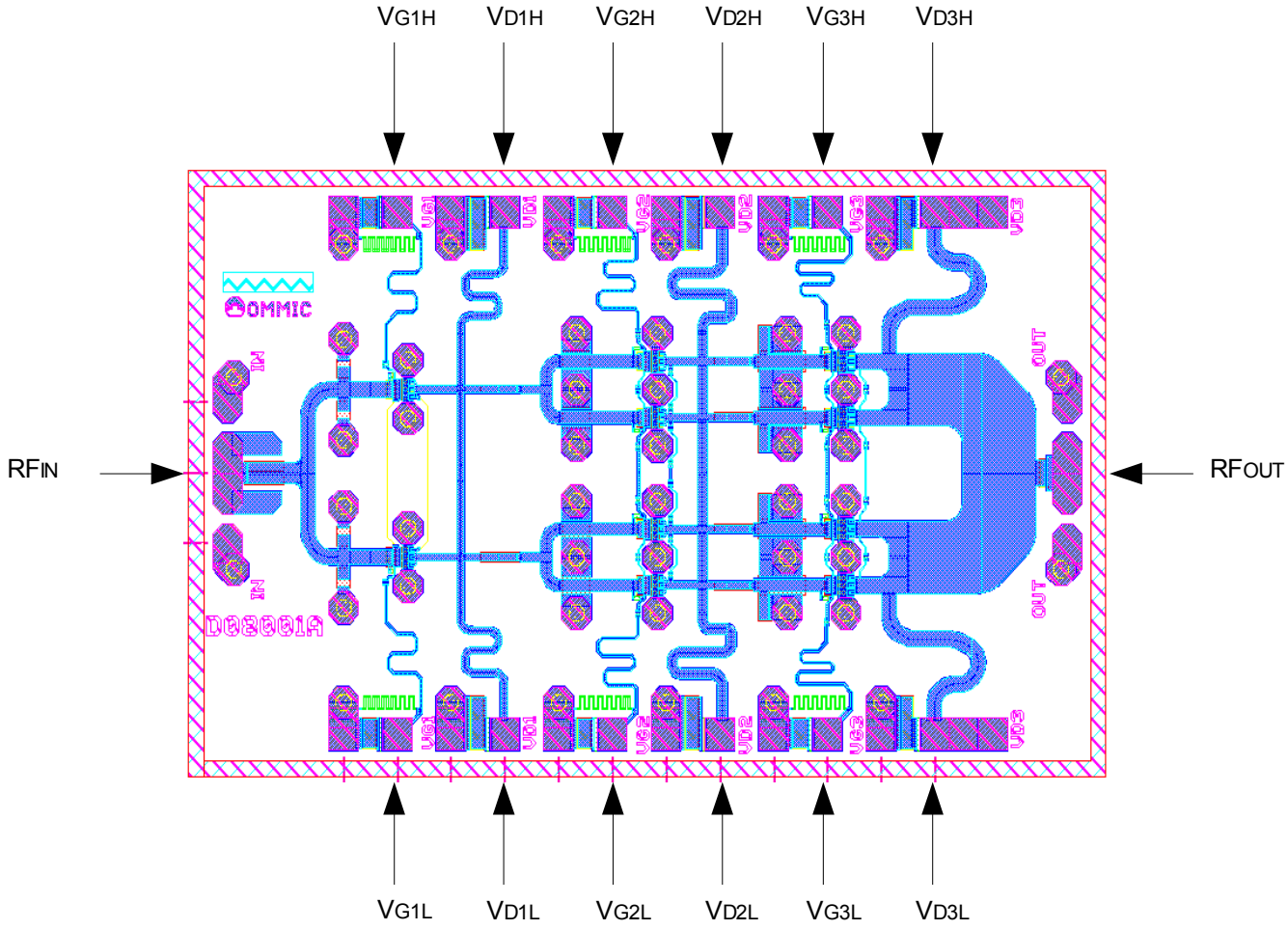
Figure 6 : APPLICATION SCHEMATICS

Component NAME	Value	Type	Comment
C1, C3, C5 C7, C9, C11	47p	Chip Capacitor	Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5#013B soldered close to the die, bonding as short as possible
R1, R2, R3	39	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-0739RL
R4, R5, R6	100	SMD 0603 Resistor	YAGEO (PHYCOMP) RC0603FR-07100RL
C2, C4, C6 C8, C10, C12	100n	SMD 0603 Capacitor	MURATA GRM188R71H104KA93D

In order to save DC power consumption and improve PAE each gate can be individually driven at a different bias voltage. In this case, when using the targeted RF signal (modulated carrier), the distortion is monitored while adjusting V_{G1}, V_{G2} and V_{G3}. The global strategy is to introduce all the distortion allowed by the targeted standard in the last stage of the amplifier by adjusting V_{G3} while V_{G2} and V_{G1} are positioned in such a way that the I_{D2}, I_{D1} are kept at the minimum value corresponding to a neglectable contribution to the global distortion.

In order to validate each stage of the amplifier, with respect to the DC, it is recommended to set V_{GN} to -1.5V, then to set V_{DN} to +1V checking that the current is not too high, after that, V_{DN} can be set to +4.5V. When V_{GN} is changed from -1.5 to -0.3V, the drain current I_{DN} increases slowly in a controlled manner to reach the typical targeted value.

DIE LAYOUT AND PIN CONFIGURATION



It is hightly recommended to place 47pF RF decoupling chip capacitors C1, C3, C5, C7 , C9, C11 at each DC terminal with as short as possible bonding wires. Additionnaly for power up, prior to apply drain voltage, gates voltages should be set to VG = -1,5 volt. On shut down, reverse order operation should be performed.

The gate voltage of each stage, starting from the output stage should be adjusted to obtain the desired quiescent drain current.

PINOUT

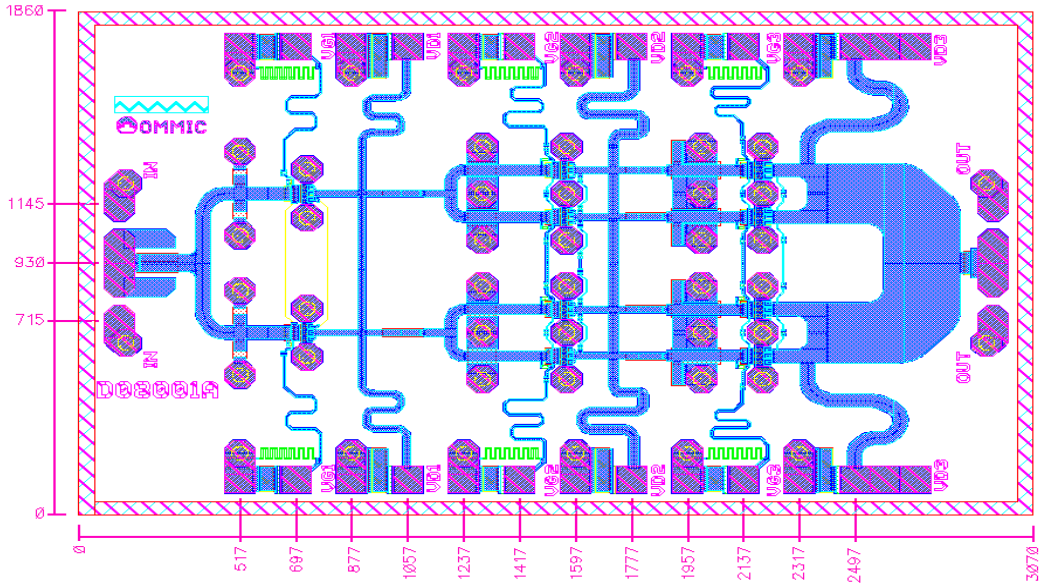
Symbol	Pad	Description
RF_{OUT}	OUT	RF output
RF_{IN}	PIN	RF input
V_{D1H}	VD1	First stage Drain (Higher Line-up)
V_{D2H}	VD2	Second stage Drain (Higher Line-up)
V_{D3H}	VD3	Third stage Drain (Higher Line-up)
V_{G1H}	VG1	First stage Gate (Higher Line-up)
V_{G2H}	VG2	Second stage Gate (Higher Line-up)
V_{G3H}	VG3	Third stage Gate (Higher Line-up)
V_{D1L}	VD1 (internally connected to V_{D1H})	First stage Drain (Lower Line-up)
V_{D2L}	VD2 (internally connected to V_{D2H})	Second stage Drain (Lower Line-up)
V_{D3L}	VD3 (internally connected to V_{D3H})	Third stage Drain (Lower Line-up)
V_{G1L}	VG1 (internally connected to V_{G1H})	First stage Gate (Lower Line-up)
V_{G2L}	VG2 (internally connected to V_{G2H})	Second stage Gate (Lower Line-up)
V_{G3L}	VG3 (internally connected to V_{G3H})	Third stage Gate (Lower Line-up)
GND	BACKSIDE	Ground

Note :
It is key in order to ensure good performance and stability that the ground pad present on the backside of the die is suitably connected to the ground.

PACKAGE

Type	Description	Terminals	Pitch (mm)	Die size (mm)
DIE	100% RF and DC on wafer tested	14	-	3.07 x 1.86 x 0.1

BONDING PAD COORDINATES



SOLDERING

During soldering process, to avoid permanent damages or impact on reliability, die temperature should never exceed 330°C.

Temperature in excess of 300°C should not be applied to the die longer than 1mn

Toxic fumes will be generated at temperatures higher than 400°C

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
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ORDERING INFORMATION

Generic type	Package type	Version	Sort Type	Description
CGY2131	UH	C1		On-Wafer measured Die

RoHS Compliant

Document History :
Version 1.0, Last Update 26/07/2010
Version 1.0, Demo board Update 14/09/2011

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