PRODUCT DATASHEET

CGY2112UH/C1

10.7Gb/s Linear TransImpedance Amplifier

DESCRIPTION

The CGY2112UH is a 10.7 Gb/s TransImpedance Amplifier (TIA), designed for use in optical reception systems.
The device is intended to be used with a PIN or APD photodetector. There is a built in AGC function which limits the peak-to-peak output voltage and protects the device from optical input overload.
The die is manufactured using OMMIC's 0.18 µm gate length PHEMT Technology. The MMIC uses gold bonding pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

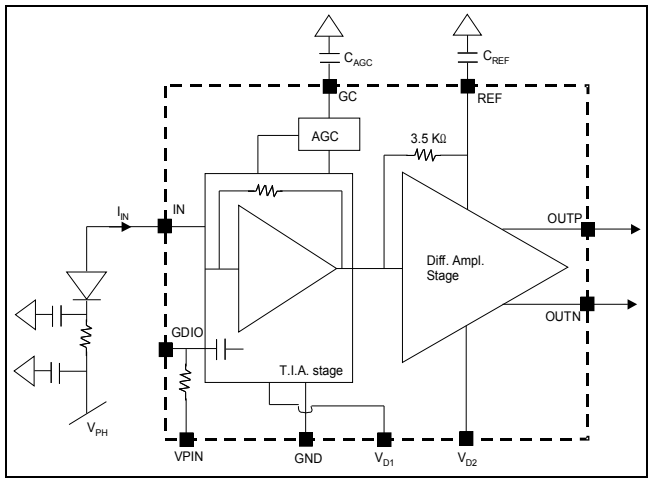
FEATURES

- Suitable for 10.7 Gb/s optical fiber links
- Single +5 V supply voltage
- 2 KΩ (66 dBΩ) single-ended transimpedance
- Sensitivity : -21 dBm
- Built in AGC function
- 85 mA consumption current at +5 V
- 425 mW Power consumption at +5 V
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD Available

APPLICATIONS

- 10 Gbps optical receivers
- DWDM SONET/SDH
- Transponders modules : MSA300, XENPAK, XPAK, X2
- Transceivers modules : XFP

RoHS Compliant



Block Diagram of the CGY2112UH/C1

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LIMITING VALUES

T_{amb} = 25 °C unless otherwise noted

Symbol	Parameter	Conditions	MIN.	MAX.	UNIT
V_{DD}	Supply voltage		- 0.5	+ 8	V
V_{PH}	Photodiode biasing voltage	Photodiode cathode connected to a supply voltage via GDIO and VPIN pads	- 15	+ 15	V
I_{IN}	Input photo-current	Average at V_{DD} = 5.0 V	-1	4	mA
T_j	Junction temperature			+ 150	° C
T_{stg}	Storage temperature		- 55	+ 150	° C

OPERATING CONDITIONS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
V_{DD}	Positive Supply voltage		4.75	5.0	5.25	V
T_{op}	Operating ambient temperature		-10		+85	°C
Input interface	DC coupled					
Output interface	AC coupled					

DC CHARACTERISTICS

Typical data are defined at T_{amb} = 25 °C, V_{DD} = 5 V ; unless otherwise noted.

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
I_{DD}	Supply current			85	110	mA
V_{INDC}	DC input voltage (see note 1)			1.2		V
I_{IN_LIM}	Input average current for AGC activation (see note 2)			100		uA
$\lvert dV_{OUT} \rvert$	Voltage offset between the two outputs in absolute value	At 8 µA DC input current			+0.5	V
V_{OUTDC}	DC voltage available at OUTP and OUTN pads			3.6	4	V

NOTE

1. V_{INDC} : DC voltage available at the RF input pad of the TIA.
2. For an input average current less than I_{IN_LIM}, the output voltage is proportional to the input current. Whereas for an input average current higher than I_{IN_LIM}, the AGC function is activated, leading to a linear decrease of the gain.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document “OM-CI-MV/ 001/ PG” contains more information on the precautions to take.

AC CHARACTERISTICS

All measured data are at V_{DD} = 5V; T_{amb} = 25 °C; R_L = 50 Ω. The TIA is measured on-wafer using RF probes without any light beam on the top of the IC (see note 1). Unless otherwise stated.

Photodiode elements and parasitics :

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
C_{PH}	Photodiode capacitance	Suggested value		0.2		pF
L_{PH}	Photodiode bonding inductance	Suggested value		1.0		nH
R_{PH}	Photodiode series resistance	Suggested value		8.0		Ω
$L_{BOND,OTHER}$	Inductance on each of all other bond pads on the TIA (excluding the RF input inductance)	Suggested value		0.5		nH

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
	Data rate		10.7			Gb/s
$\|ZT\|_{LF}$	Low-Frequency Transimpedance gain	F=0.2GHz, single-ended (note 2)	65	66	69	dBΩ
$\Delta\|ZT\|$	Transimpedance ripple (=$\|ZT\|$ - $\|ZT\|_{LF}$)	F = 0.2 MHz to 1 GHz	-1		+1	dB
		F = 1 GHz to 2.5 GHz	-1		+2	dB
		F = 2.5 GHz to 4 GHz	-1		+3	dB
		F = 4 GHz to 6.5 GHz	-1		+4	dB
		F = 6.5 GHz to 8 GHz	-2		+4	dB
		F = 8 GHz to F_c			+4	dB
F_c	Transimpedance cut-off frequency	$\|ZT\|$ = $\|ZT\|_{LF}$ – 3 dB	9.1	9.5		GHz
$F_{c,Low}$	Low Frequency cut-off (note 3)	AC coupled at the outputs (via 100 nF capacitor)			25	KHz
I_{PKMAX}	Maximum peak input current before input overload (note 4)		2.5			mApp
T_G	Group delay	F = 0.2 MHz to Fc		±25	±30	ps
V_{OUT}	Output swing, single-ended			600		mVpp
S_{22}	Output reflection coefficient (note 5). Input loading conditions : C_{PH} = 0.2 pF; L_{PH} = 1.0 nH; R_{PH} = 8 Ω	F = 0.2GHz to 5.5GHz			-10	dB
		F = 5.5 GHz to 10GHz			-8	dB
I_{NOISE}	Total integrated input RMS noise	F = 0.1 GHz to F_c		960		nA
S	Optical input sensitivity (note 6)	ρ = 0.95 A/W, r_e = 12 dB, BER = 10^{-12}		-21		dBm
K	Microwave Stability Factor	All passive source and load impedances	1.1			
R_L	Output load termination (OUTP, OUTPN)			50		Ω

NOTE

1) With a light beam on the top of the IC, RF performances might be slightly different.

2) The gain specification is guaranteed down to the lower cut-off frequency. 0.2 GHz is specified as a reference for convenience of measurement.

3) The CGY2112UH is AC coupled at its outputs via an external capacitor, C. So the low frequency cut-off is determined by the time constant RC, where R is the total output resistance (on-chip output series 50 Ohms impedance of the TIA circuit plus the external 50 Ohms load) equivalent to 100 Ohms. Assuming that C is 100 nF, the low frequency cut-off is given by : F_{c_low} = 1/(2*pi*R*C) = 16 KHz.

4) This characteristics is guaranteed by design and by measurement (verified using evaluation boards with 2^{31} – 1 PRBS, BER of 10^{-12}).

5) With typical output bond wire inductances L_{OUTP}, L_{OUTN} = 0.5 nH, the Output reflection coefficient is improved.

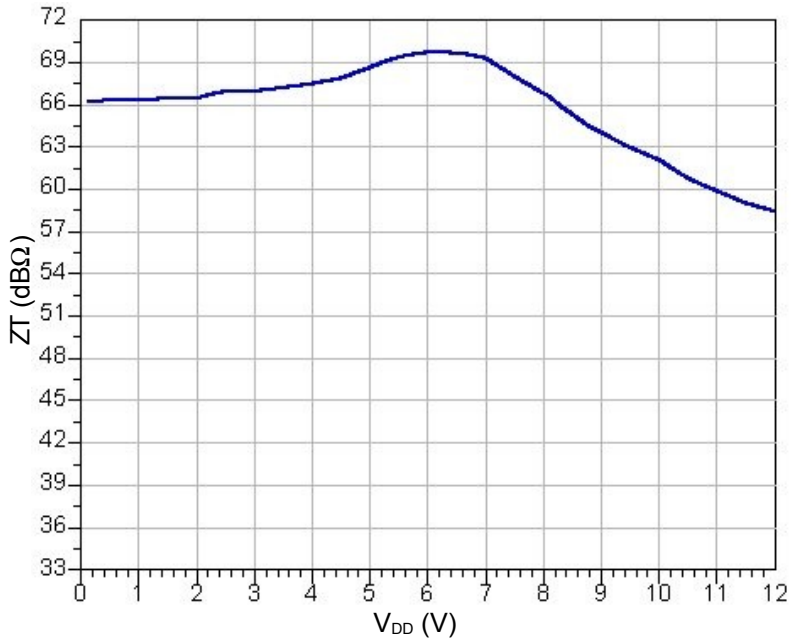
6) The sensitivity is computed from the total integrated input RMS noise. To obtain a system bit-error rate of 10^{-12}, the signal-to-noise ratio must be 14.1 or better. The input sensitivity, expressed in average power, is calculated as :

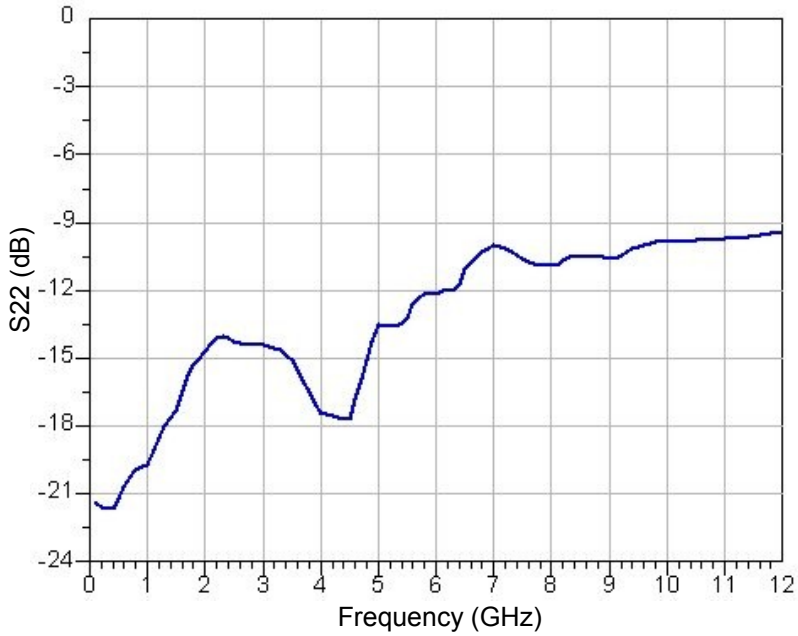
$$Sensitivity = 10\log\left(\frac{14.1\times I_{NOISE}\times(r_e+1)}{2\times\rho\times(r_e-1)}\times 1000\right) \text{ dBm}$$

where ρ and r_e are respectively, the photodiode responsivity in A/W and the extinction ratio. I_{NOISE} is measured in amperes.

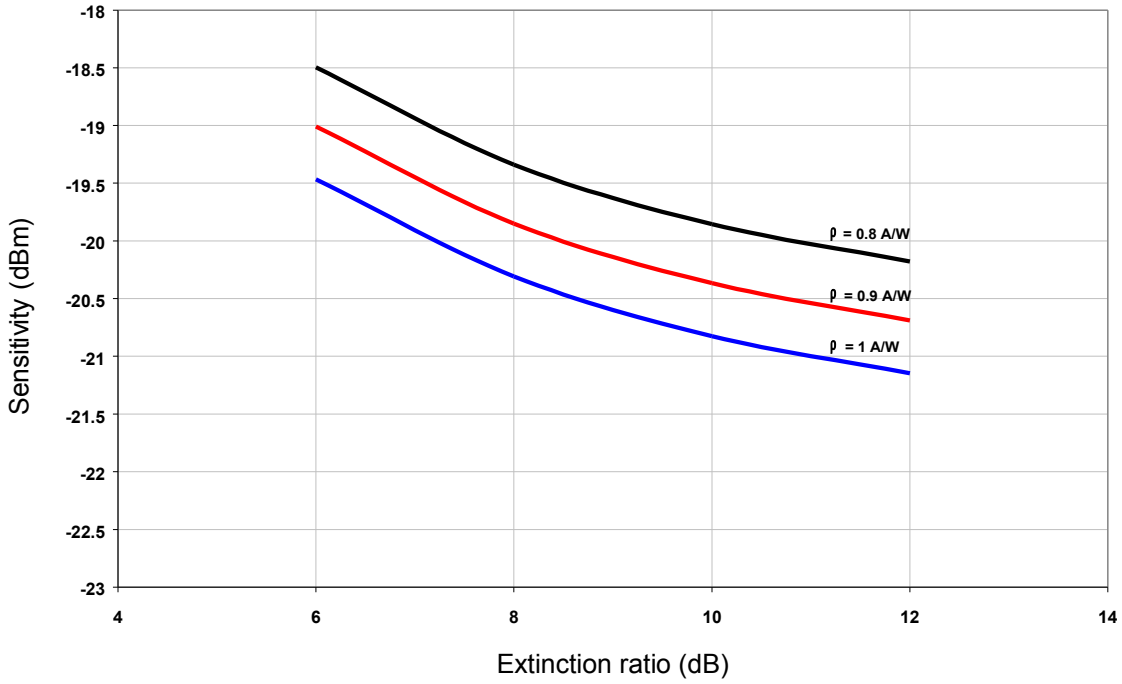
MEASURED PERFORMANCE CHARACTERISTICS

Operating Temperature of 25°C. V_{DD} = +5 V. Results are from on-wafer measurements.





Transimpedance gain vs. V_{DD} and Output Return Loss vs. Frequency
Input Loading Conditions : C_{PH} = 0.1 pF, L_{PH} = 1 nH, R_{PH} = 8 Ω.

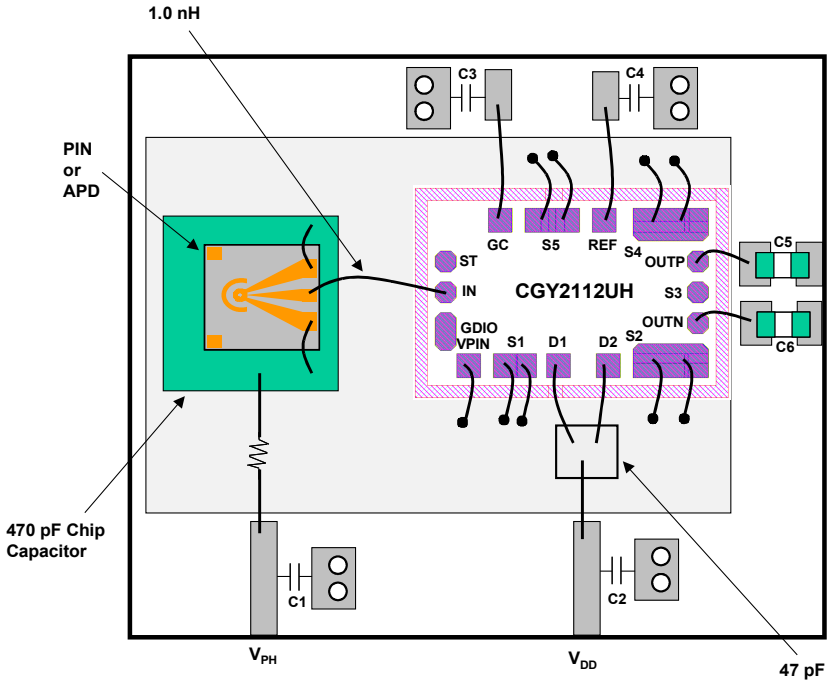


Sensitivity vs. Extinction ratio at various photodiode sensitivity, ρ.

APPLICATION INFORMATION

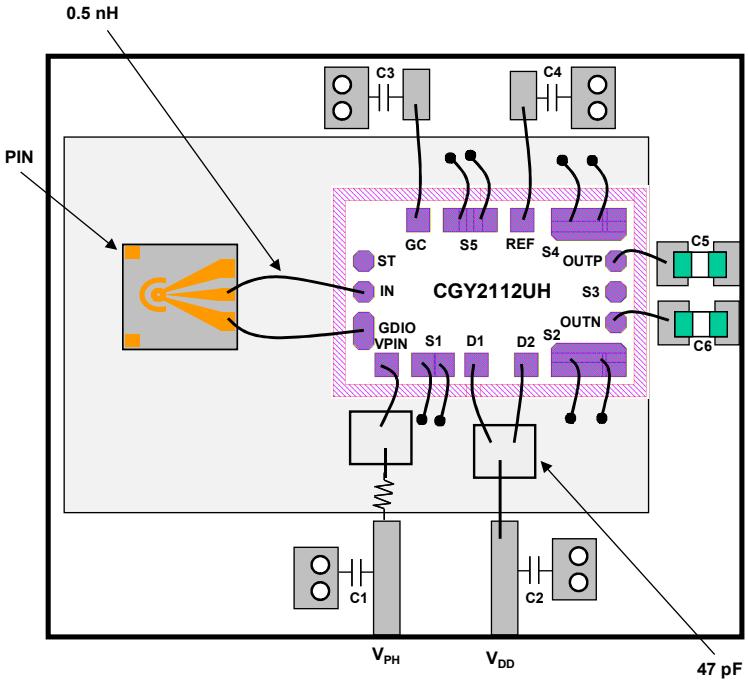
The performance of the photo-receiver module is dependent both on the photodiode capacitance and on the interconnection inductance between the photodiode and the CGY2112UH/C1. The circuit was optimized for a photodiode capacitance C_{PH} lower than 0.2 pF with a low photodiode series resistance (R_{PH}) to give the best noise performance from the receiver module.

In this application note, two modules layout are proposed, the difference occurs only at the receiver input :



The figure above shows a configuration which is suitable for both PIN and APD photodiodes.

The figure below shows a second configuration that is suitable for photodiodes only :



The CGY2112UH/C1 also offers an option to bias the photodiode through the VPIN pad. It is important to note that APD photodiode cannot be mounted with this configuration (more than 15 V, DC supply voltage (required for APD) cannot be applied on this pad due to potential problems via the substrate).

It is recommended to use a total input equivalent bonding inductance value of typical 1.0 nH, while 1.3 nH should be considered as a maximum value. The length of the output bonding wire should be minimized.

To improve power supply rejection throughout the frequency band, 47 pF and 100 nF capacitors are required. The 47 pF capacitor provides a decoupling at frequencies above 1 GHz and should be positioned close to the chip. The 100 nF capacitor is for decoupling at lower frequencies and can be positioned further away from the chip.

A good RF grounding connection should be maintained between the ground pads of the chip and the ground of the system. The grounding of high gain amplifiers is critical for achieving the maximum microwave performance. Inductance due to bonding wires can cause unwanted feedback, performance degradation, resonances and possibly oscillations. To reduce the inductance effect, several bond wires can be used in parallel on each bond pad.

The CGY2112UH/C1 can be used in differential or single ended topology. In the case of single ended configuration, the unused output pad is connected to a 50Ω load via a 100 nF DC blocking capacitor.

Recommended Components :

C1, C2, C3, C4 :	100 nF 0402 sub-mount capacitors	
C1, C2, C3, C4 :	100 nF chip Murata :	GMA085F51A104ZD01T (size : 0.8 x 0.8 x 0.5 mm)
C1, C2, C3, C4 :	100 nF chip Presidio :	VL3030Y5V104Z16VH5 (size : 0.8 x 0.8 x 0.56 mm) or VL4080X7R104M16VH5 (size : 1.016 x 2.032 x 0.635 mm)
C5, C6 :	100 nF 0402 sub-mount capacitors	

Power Supply Sequence :

The following power supply sequence is recommended (V_{PH} : Photodiode bias, V_{DD} : TIA bias)

a) Always turn on the photodiode bias V_{PH} first or simultaneously with V_{DD}. Since the photodiode is direct coupled to the TIA input, powering V_{DD} first can damage the photodiode through forward bias and excess current.
b) Apply the input optical signal.

It is important to apply the DC voltage from ground, then increases them to their desired values.

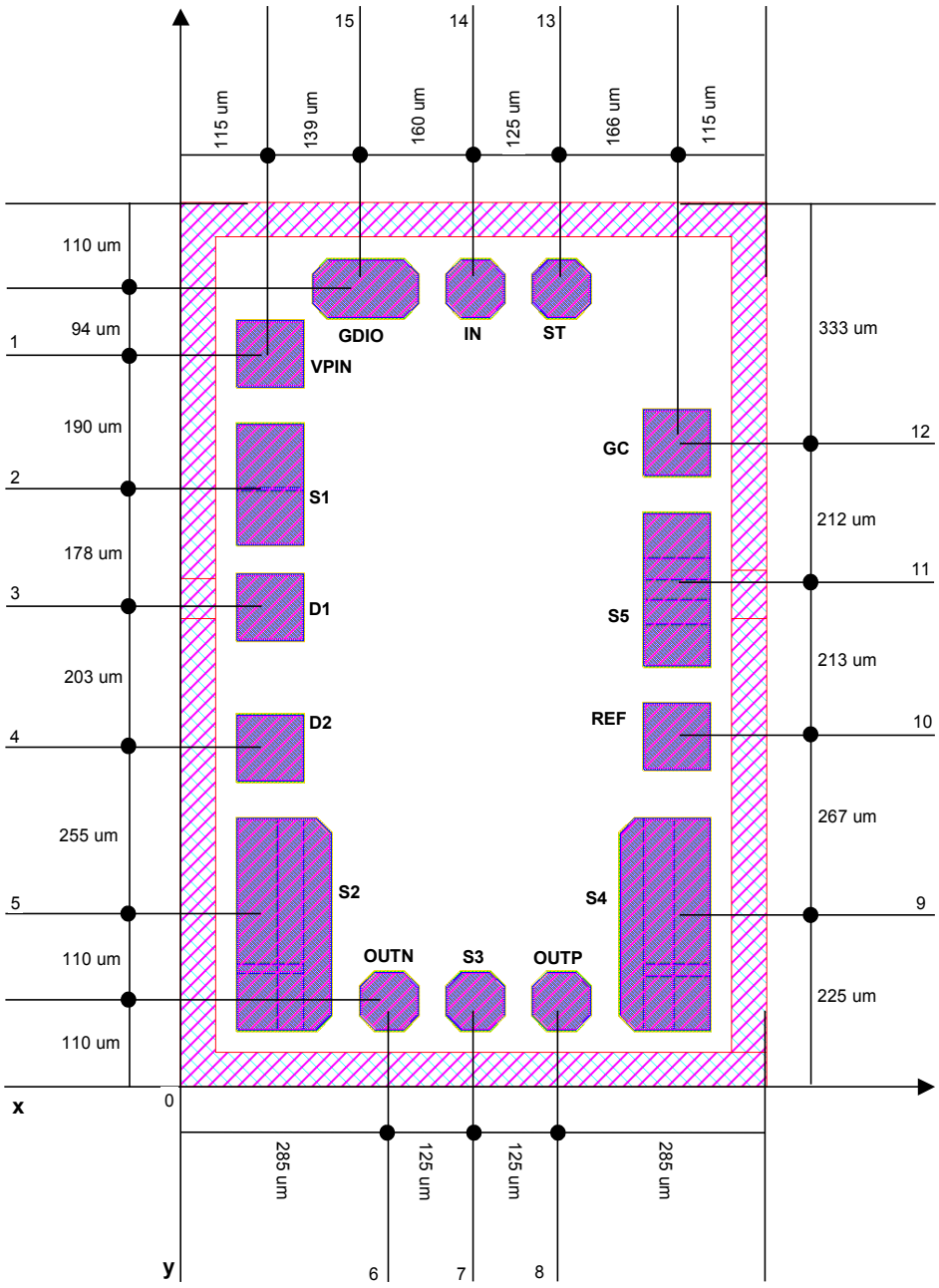
Handling Precautions :

a) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
b) Require all handling personal to wear a conductive bracelet or wrist-strap connected to the ground.
c) Ground all test equipment and all soldering iron tops.
d) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

Caution : This device is a high performance RF component and can be damaged by inappropriate handling. Standard ESD precautions should be followed. OMMIC document "OM-CI-MV/ 001/ PG" contains more information on the precautions to take.

MECHANICAL INFORMATION

Chip size = 1250 x 820 µm (± 15 µm)
Chip Thickness = 200 µm



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PAD POSITION

PAD NAME	PAD NUMBER	COORDINATES		DESCRIPTION
		Y	X	
VPIN	1	1046	115	Photodiode DC supply voltage pad (optional use : see figure 6)
S1	2	856	115	Bond to ground
D1	3	678	115	First stage DC supply voltage, must be decoupled to ground using external capacitor(s)
D2	4	475	115	Second stage DC supply voltage, must be decoupled to ground using external capacitor(s)
S2	5	220	115	Bond to ground
OUTN	6	110	285	RF inverted output
S3	7	110	410	Do not bond
OUTP	8	110	535	RF non-inverted output
S4	9	225	705	Bond to ground
REF	10	492	705	Reference input voltage, must be decoupled to ground using an external capacitor (see figure 5 or figure 6)
S5	11	705	705	Bond to ground
GC	12	917	705	Gain control pad, must be decoupled to ground using an external capacitor (see figure 5 or figure 6)
ST	13	1140	539	Do not bond
IN	14	1140	414	RF input. To be connected to a photodiode anode
GDIO	15	1140	254	To be connected to a photodiode cathode (optional use : see figure 6)

All x and y coordinates (in µm) represent the position of the center of the pad with respect to the lower left corner of the chip layout
See Mechanical Information for more details.

Bonding Pad	Dimensions (µm)
VPIN, D1, D2, GC, REF	100 x 100
IN, ST, OUTP, OUTN, S3	88 x 88
GDIO	157 x 88
S1	179 x 100
S2, S4	310 x 100
S5	225 x 100

PACKAGE

Type	Description	Terminals	Pitch (mm)	Die size (mm)
UH	Bare Die	-	-	1.25 x 0.82 mm ±15 um Die Thickness : 200 µm

DEFINITIONS

Limiting values definition
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Applications that are described herein for any of these products are for illustrative purposes only. OMMIC makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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ORDERING INFORMATION

Generic type	Package type	Version	Sort type	Description
CGY2112	UH	C1	-	10.7 Gb/s Linear TransImpedance Amplifier

RoHS Compliant

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