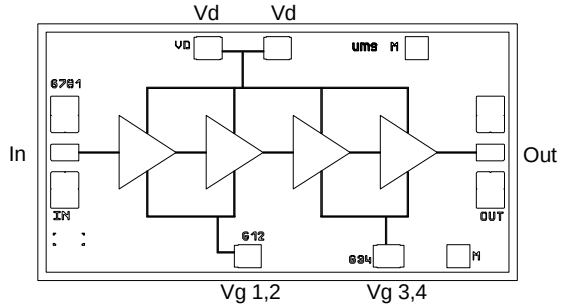
36-40GHz Low Noise Very High Gain Amplifier

GaAs Monolithic Microwave IC

Description

The CHA2095a is a four-stage monolithic low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems.

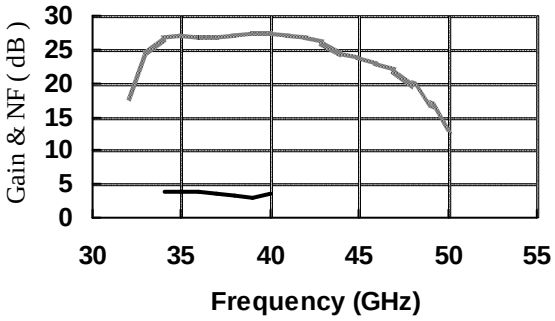
The circuit is manufactured with a pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances
- 3.5dB Noise Figure
- 26dB gain
- ±1.0dB gain flatness
- Low DC power consumption, 90mA @ 3.5V
- Chip size: 2.07 X 1.11 X 0.10 mm

Typical on wafer measurements



Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36		40	GHz
G	Small signal gain	22	26		dB
P1dB	Output power at 1dB gain compression	8	10		dBm
NF	Noise figure		3.5	4.0	dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics

Tamb = +25°C, Vd= 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	36		40	GHz
G	Small signal gain (1)	22	26		dB
ΔG	Small signal gain flatness (1)		±1.0		dB
ΔGsb	Gain ripple over 40MHz (within -30 ; +75°C)			0.5	dBpp
Is	Reverse isolation (1)	35	40		dB
P1dB	Output power at 1dB gain compression	8	10		dBm
VSWRin	Input VSWR (1)		2.5:1	3.0:1	
VSWRout	Output VSWR (1)		2.5:1	3.0:1	
NF	Noise figure (2)		3.5	4.0	dB
Vdc	DC Voltage Vd Vg	 -2	3.5	4 +0.4	V V
Id	Bias current (2)		90	140	mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

(2) 90 mA is the typical bias current used for on wafer measurements, with adjusting Vg1, 2 voltage for optimum noise figure and Vg3,4 adjusting for maximum gain.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Vg	Gate bias voltage	-2.0 to +0.4	V
Id	Drain bias current	200	mA
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

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Typical Scattering Parameters *(On wafer Sij measurements)*

Bias Conditions: Vd= 3.5 Volt, Vg1, 2 = -0.5V, Vg3, 4 = -0.3V, Id = 90 mA.

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
2	-4.08	-69.3	-72.96	56.9	-33.56	147.7	-1.13	-47.0
4	-5.88	-96.9	-66.24	-10.3	-27.97	81.3	-2.97	-80.6
6	-5.85	-115.9	-64.15	-39.7	-25.45	18.8	-4.33	-103.3
8	-5.39	-131.8	-60.47	-85.0	-25.28	-35.2	-5.19	-119.2
10	-4.86	-145.7	-58.55	-120.4	-26.33	-78.4	-5.62	-131.5
12	-4.42	-158.3	-56.57	-140.8	-28.30	-111.9	-5.76	-141.3
14	-4.08	-170.2	-54.57	-164.6	-30.70	-135.8	-5.71	-150.4
16	-3.86	177.7	-51.14	165.0	-32.77	-149.9	-5.49	-158.9
18	-3.75	165.3	-50.79	138.4	-33.89	-156.4	-5.28	-167.9
20	-3.74	152.0	-50.87	107.8	-36.01	-165.6	-4.99	-177.6
21	-3.79	145.3	-50.09	105.4	-36.43	-171.9	-4.92	177.3
22	-3.86	137.4	-51.20	85.4	-38.94	-167.0	-4.85	171.4
23	-4.07	129.4	-50.03	84.9	-46.43	-171.8	-4.85	166.3
24	-4.25	120.4	-48.55	76.9	-51.42	-4.6	-4.76	159.4
25	-4.62	110.0	-48.26	52.0	-33.66	-13.4	-4.84	152.4
26	-5.10	98.1	-49.21	33.2	-25.59	-17.0	-4.99	144.9
27	-5.86	83.9	-51.02	11.8	-19.53	-20.6	-5.14	136.4
28	-6.96	66.3	-53.65	3.4	-13.18	-27.7	-5.49	126.2
29	-8.56	43.0	-55.77	2.9	-6.22	-37.3	-5.97	114.7
30	-10.85	9.2	-57.30	-12.5	1.29	-52.8	-6.73	99.1
31	-13.21	-44.9	-56.20	32.7	9.14	-76.6	-7.93	78.0
32	-12.39	-121.0	-49.77	-1.8	17.49	-114.9	-9.65	41.0
33	-11.54	161.0	-49.70	-31.8	24.39	-175.8	-11.68	-29.6
34	-17.21	82.0	-51.44	-35.1	26.82	115.0	-10.76	-104.3
35	-20.36	-35.5	-47.38	-81.5	27.07	61.7	-8.74	-142.6
36	-13.92	-105.9	-46.89	-126.8	26.81	17.6	-7.39	-171.4
37	-10.14	-139.8	-47.95	-139.2	26.72	-19.2	-7.28	167.6
38	-8.35	-170.4	-46.59	164.0	27.05	-55.3	-7.82	151.2
39	-8.59	157.4	-45.05	177.2	27.29	-91.5	-9.01	141.8
40	-10.56	122.6	-44.36	142.8	27.30	-129.0	-10.33	136.3
41	-16.13	80.3	-42.19	111.1	25.35	-164.2	-11.12	138.9
42	-22.46	-18.9	-41.27	88.1	25.09	157.8	-10.65	139.4
43	-15.92	-81.9	-40.37	70.8	24.61	128.8	-10.47	130.8
44	-12.13	-107.0	-39.92	43.0	23.99	98.5	-11.70	122.6
45	-9.91	-119.3	-40.59	19.9	23.49	68.1	-13.82	118.6
46	-8.25	-123.9	-37.38	-1.2	22.86	34.0	-16.93	129.0
47	-6.10	-125.8	-37.23	-30.8	21.97	-3.5	-15.21	174.9
48	-3.79	-139.9	-34.59	-85.7	19.73	-41.4	-10.25	172.2
49	-1.93	-154.8	-44.23	-109.4	16.66	-76.2	-7.41	152.0
50	-1.26	-167.8	-44.58	-75.7	13.11	-105.0	-6.75	136.3
51	-0.92	179.8	-41.46	-68.6	9.27	-129.2	-6.70	123.0
52	-0.73	170.5	-44.38	-120.1	5.69	-148.8	-6.99	112.4
53	-0.64	162.0	-65.24	64.9	2.23	-166.3	-7.31	103.1
54	-0.66	154.0	-51.59	-46.4	-1.42	176.6	-7.72	95.1
55	-0.63	147.5	-52.88	-54.0	-4.88	162.4	-8.06	87.4

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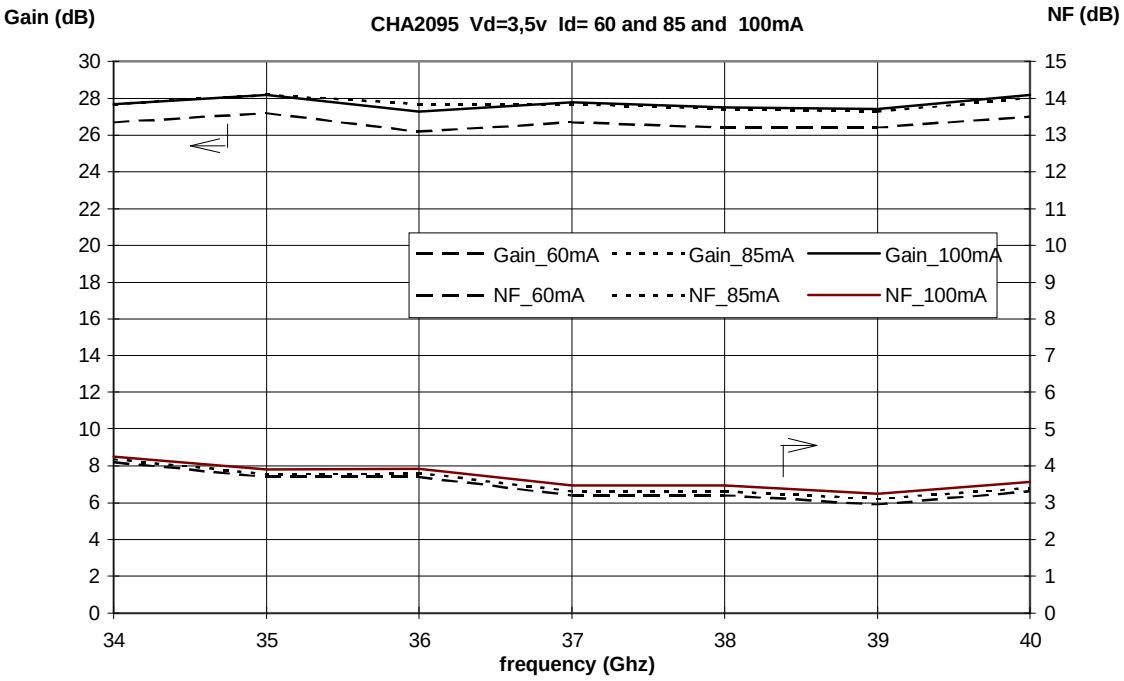
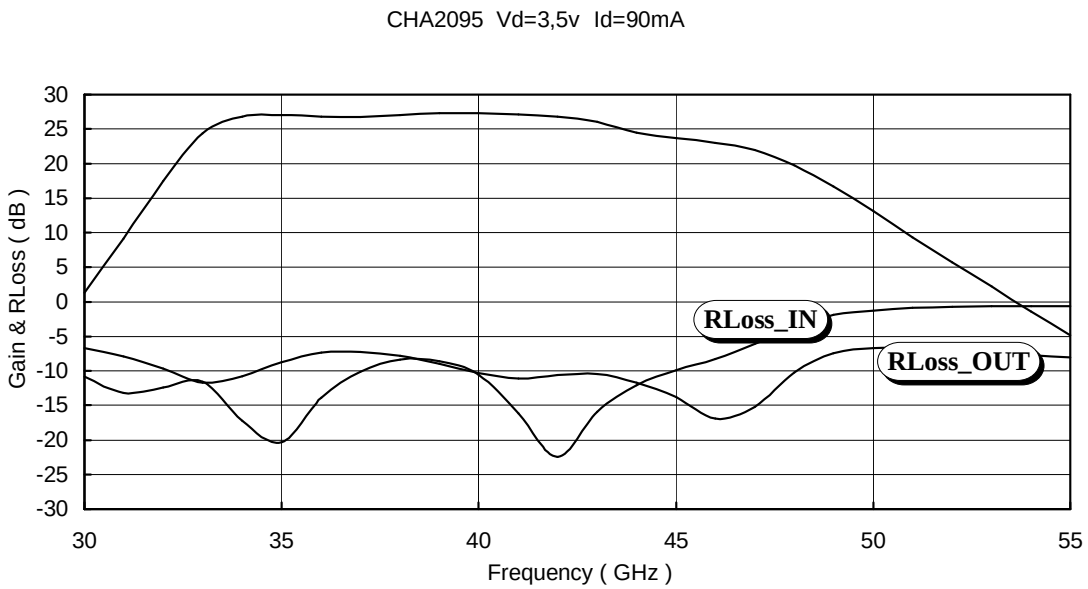
Typical on Wafer Measurements

Tamb = +25°C

Noise figure versus drain current 60, 85, 100mA



Wide band on wafer Sij parameter measurements



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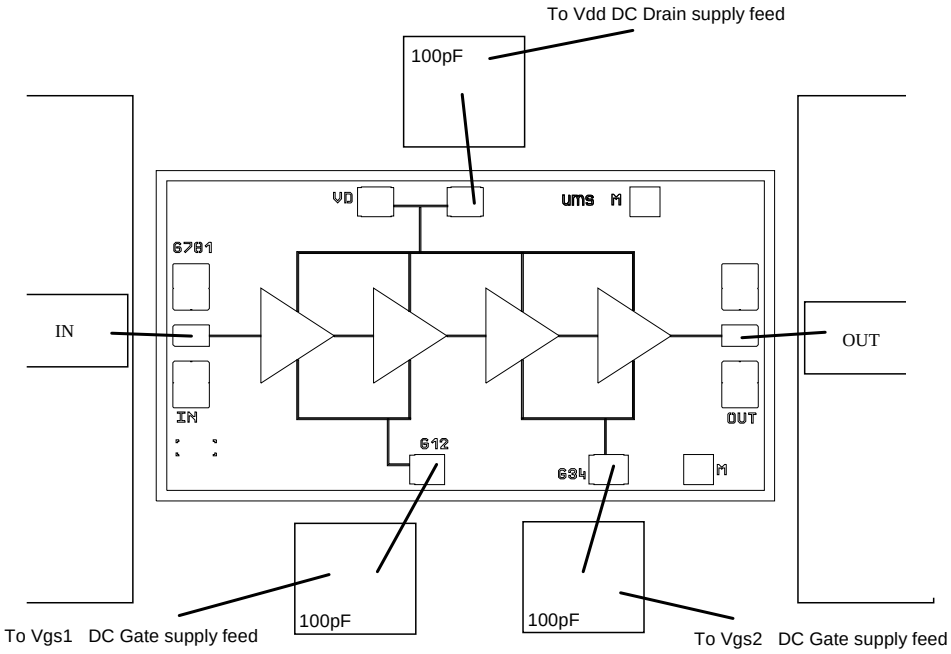
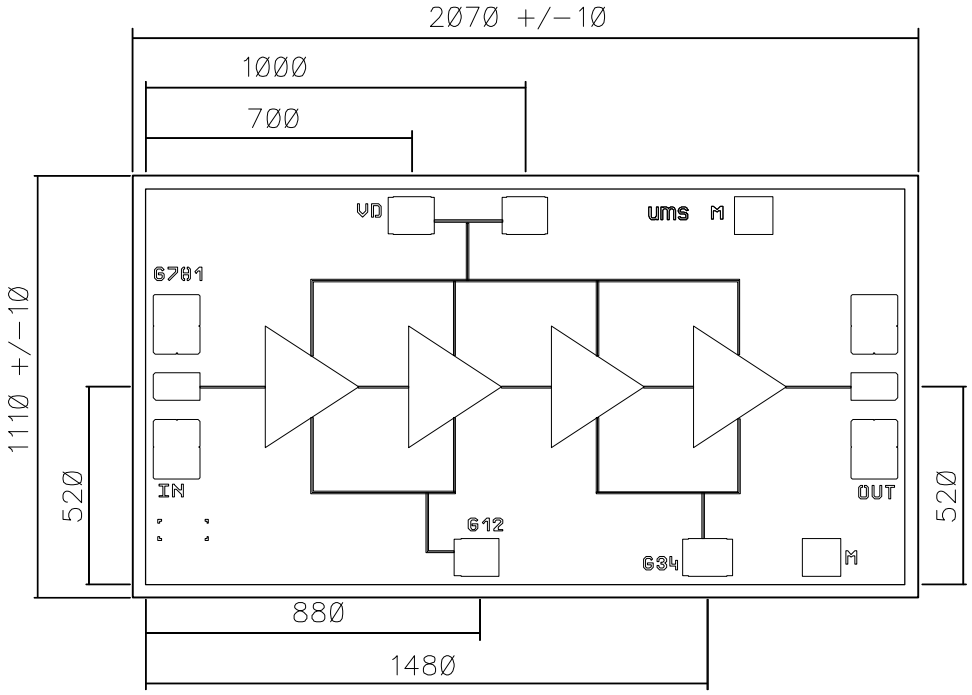
Chip Assembly and Mechanical Data



Note: Supply feed should be capacitively bypassed.



Bonding pad positions.
(Chip thickness: 100µm. All dimensions are in micrometers)

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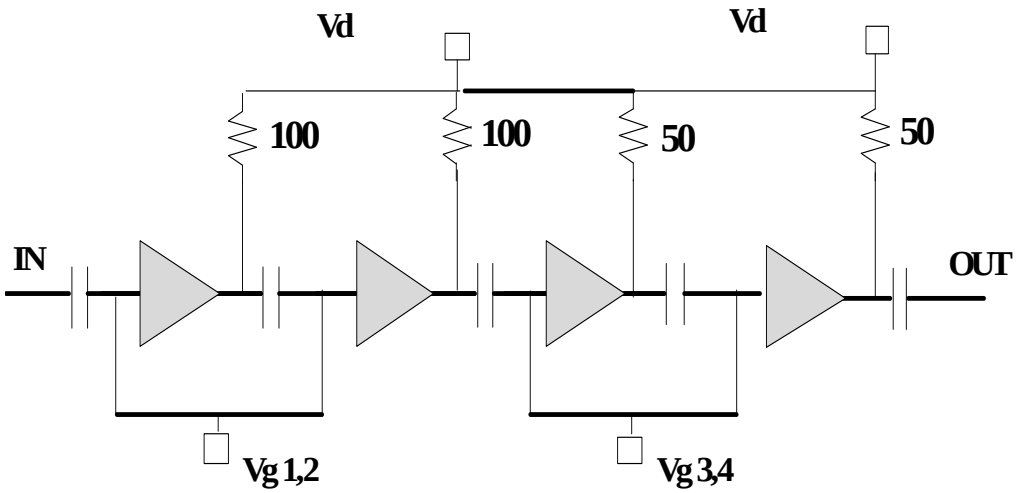
Typical Bias Tuning for Low Noise Operation

The circuit schematic is given below:



For low noise operation, a separate access to the gate voltages of the two first stages (Vg1, 2), and of the two last stage (Vg3,4) is provided. Nominal bias is obtained for a typical current of 60 mA for the output stages and 30 mA for the two first stages (90 mA for the amplifier).
The first step to bias the amplifier is to tune Vg1, 2 = -1V, and Vg3, 4 to drive 60 mA for the full amplifier. Then Vg1,2 is increased to obtain 90 mA of current through the amplifier. A fine tuning of the noise figure may be obtained by modifying the Vg1, 2 bias voltage, but keeping the previous value for Vg3, 4.
It is possible to reduce the total DC current by biasing Vg3, 4 to a more negative value. The consequences will be a reduction of gain and of the output power capabilities of the amplifier.
Vd could be adjust in such a way that the Vds (Drain to Source voltage of the internal transistor) is kept below 3.5V, knowing that all the transistors have the same size, and with the given resistors.

Ordering Information

Chip form : CHA2095a99F/00

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