

## FEATURES

- ζ 24/25 dBm P1dB/PSAT
- ζ Full 60 GHz ISM-band coverage
- ζ 32 dBm OIP3
- ζ 19 dB gain

## TYPICAL APPLICATIONS

- ζ Point-to-point communication
- ζ Instrumentation
- ζ Fiber over radio
- ζ WiGig incl. new 802.11a/y frequencies

## DESCRIPTION

gAPZ0039 is a Power Amplifier (PA) in the 60 GHz ISM frequency band suitable for WiGig V-band point-to-point communication. The PA's output stage has four parallel HEMTs to increase output power. The PA has high gain, high linearity, low input/output return loss and flat gain response, as well as out of band rejection.

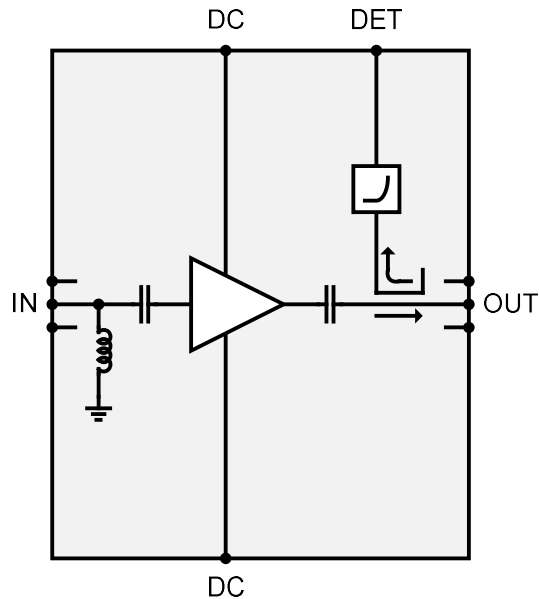


Figure 1. Block diagram of the PA.

## ELECTRICAL PERFORMANCE

Table 1. Electrical performance  $T_A=25^{\circ}\text{C}$ 

Parameter	Min	Typ	Max	Unit
Frequency	55 (52)		71 (72)	GHz
Gain	16	19	21	dB
Gain control	<-15		0	dB
P1dB	23	24	26	dBm
PSAT	24	25	26	dBm
OIP3	30	32	34	dBm
PAE			20	%
Input return loss	8			dB
Output return loss	12			dB
Power consumption		1700		mW

## MEASURED PERFORMANCE

The chip has been measured on-wafer using CW and 2-tone input test signals. The PA uses typical bias settings if not specified differently.

Table 2. Test conditions

Parameter	Setting
RF input power	-10 dBm/tone
RF input frequency	61 GHz
Frequency separation	10 MHz
Temperature	25°C

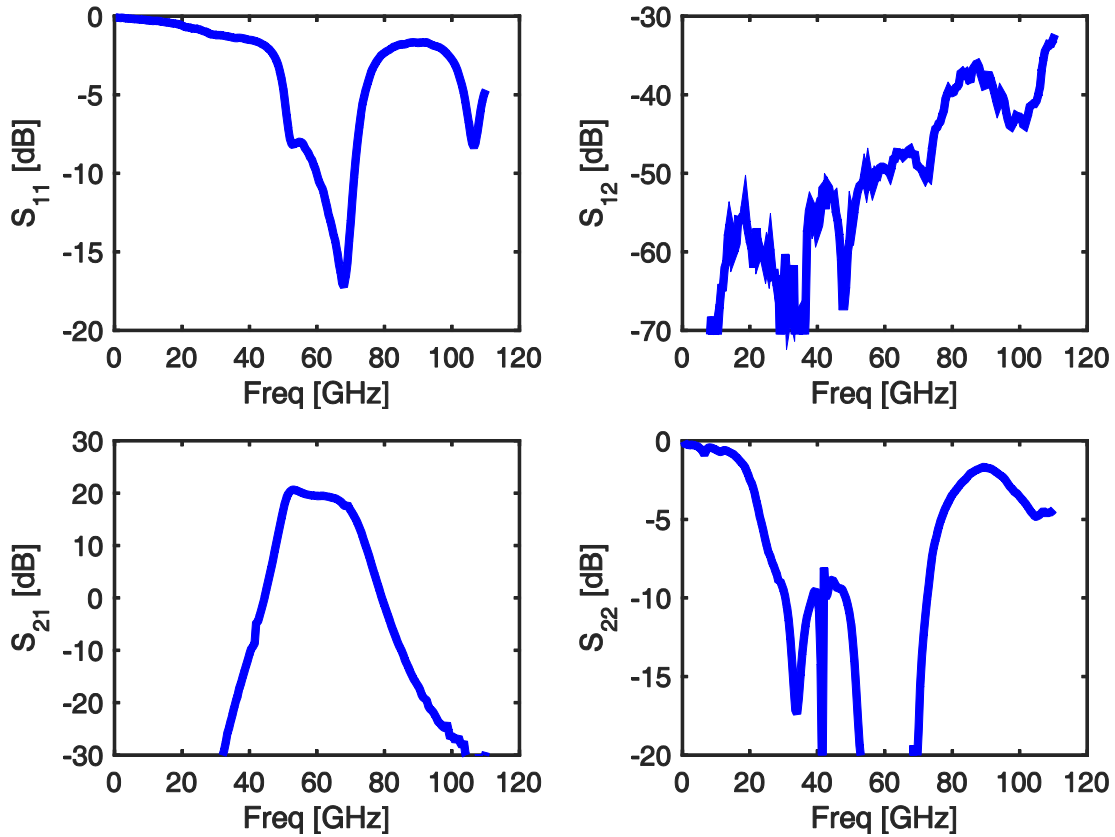
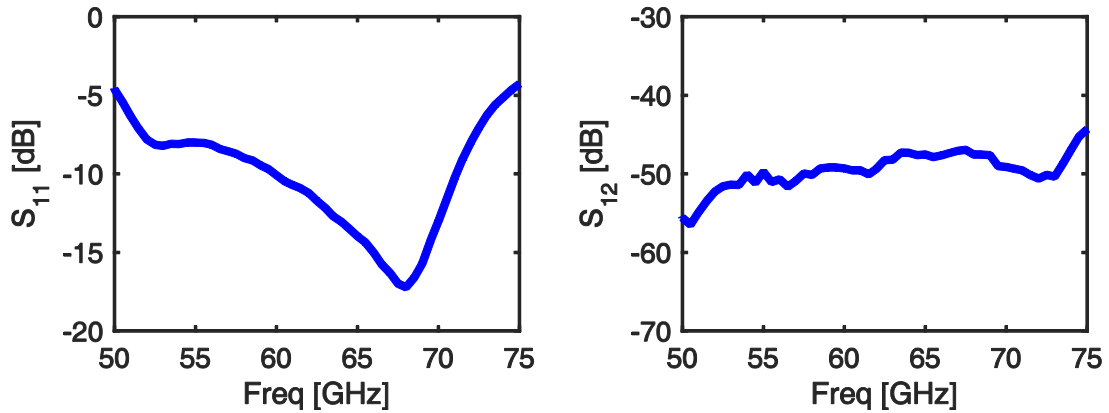


Figure 2. Small signal response from 0-120 GHz at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.



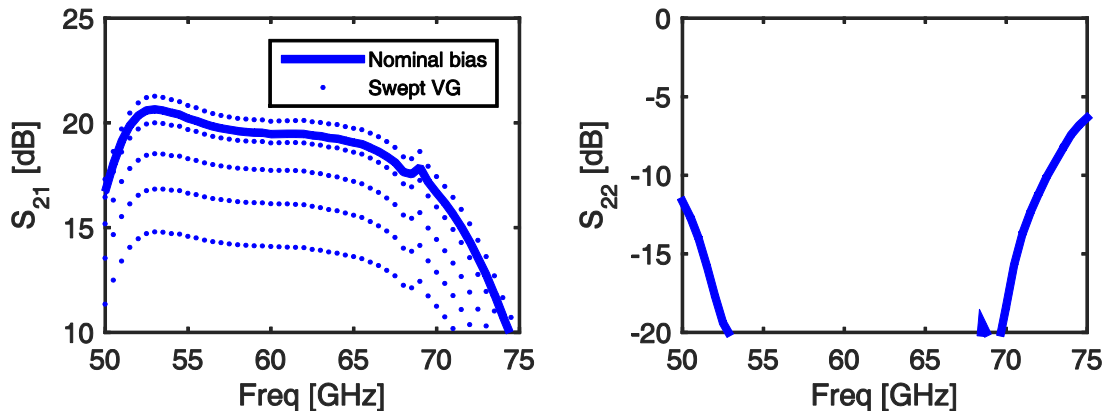


Figure 3. Small signal response within the V-band at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain, (solid) nominal bias and (dashed) VG1 = VG2 from -0.7 V to -0.3 V in 0.1 step VD nominal. Note: VG = -0.7 V not minimum for gain.. (Lower right): Output matching.

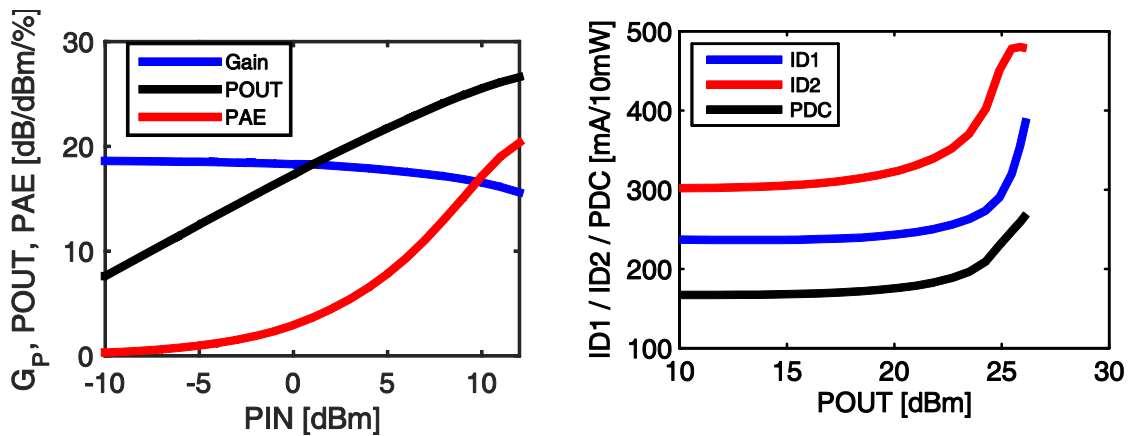
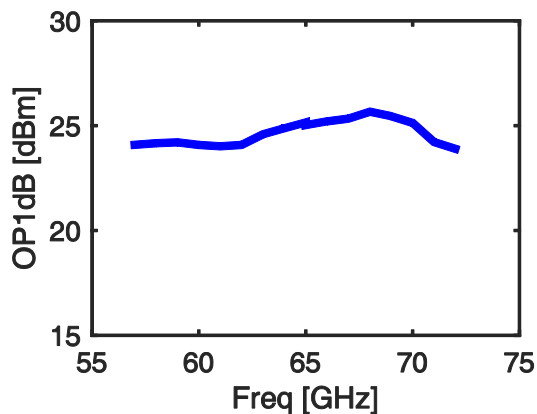


Figure 4. (Left): Output power, PAE and gain vs input power at 60 GHz. (Right): Power dissipation and drain currents ID1 and ID2 vs output power at 60 GHz.



TO BE ADDED

Figure 5. (Left): OP1db vs frequency. (Right): OIP3 vs frequency.

## RECOMMENDED OPERATING CONDITIONS

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 3-5 to obtain the specified drain currents. The drain currents are stated with no input signal.

Table 3. Electrical settings on connector P1

Connector P1	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
VOUT_DET	1	0		2	Output
VREF_DET	2	0	0.2		Output
VG_DET	3	-1.0	-0.8 <sup>[1]</sup>	-0.6	Input
VD2 <sup>[2],[3]</sup>	4	3.2	3.3 / 300	3.4	Input
GND	5	0	0	0	Ground
VG2 <sup>[2]</sup>	6	-0.7	-0.5	-0.3	Input
VG1 <sup>[2]</sup>	7	-0.7	-0.5	-0.3	Input
VD1 <sup>[2],[3]</sup>	8	3.2	3.3 / 225	3.4	Input
NC	9				NC

Table 4. Electrical settings on connector P2

Connector P2	Pad No.	Interface	I/O
GND	1		Ground
RF_OUT	2	Z <sub>0</sub> = 50 Ohm, AC coupled	Output
GND	3		Ground

<sup>[1]</sup> Maximum sensitivity is achieved at threshold voltage.

<sup>[2]</sup> VG1, VG2, VD1 and VD2 are physically connected across the chip via P1 and P3. Both connectors must be biased for maximum performance.

<sup>[3]</sup> Total current for connectors P1 and P3.

Table 5. Electrical settings on connector P3

Connector P3	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
NC	1				NC
VD1 <sup>[2,3]</sup>	2	3.2	3.3 / 225	3.4	Input
VG1 <sup>[2]</sup>	3	-0.7	-0.5	-0.2	Input
VG2 <sup>[2]</sup>	4	-0.7	-0.5	-0.2	Input
GND	5	0	0	0	Ground
VD2 <sup>[2,3]</sup>	6	3.2	3.3 / 300	3.4	Input
NC	7				NC
NC	8				NC
NC	9				NC

Table 6. Electrical settings on connector P4

Connector P4	Pad No.	Interface	I/O
GND	1		Ground
RF_IN	2	Z <sub>0</sub> = 50 Ohm, AC coupled	Input
GND	3		Ground

## ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute maximum ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
ID1	480 mA
ID2	720 mA
RF input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

## OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. The substrate thickness is 50  $\mu\text{m}$  (GaAs).

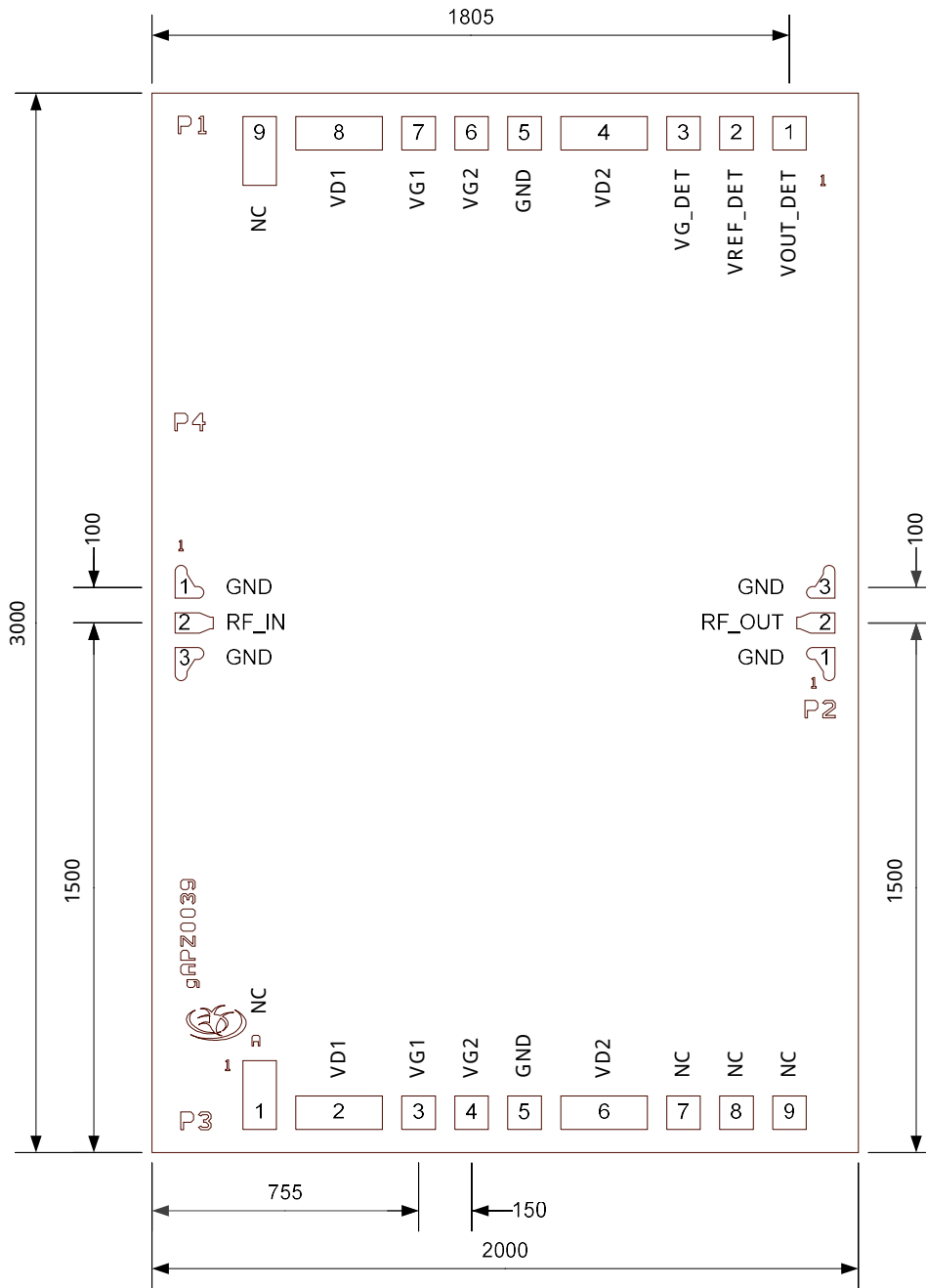


Figure 6. Outline drawing of the MMIC. Dimensions are in  $\mu\text{m}$ .