36-40GHz Very Low Noise Amplifier

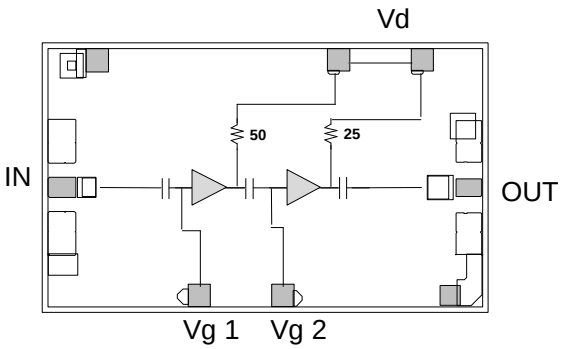
GaAs Monolithic Microwave IC

Description

The CHA2391 is a two-stage wide band monolithic low noise amplifier.

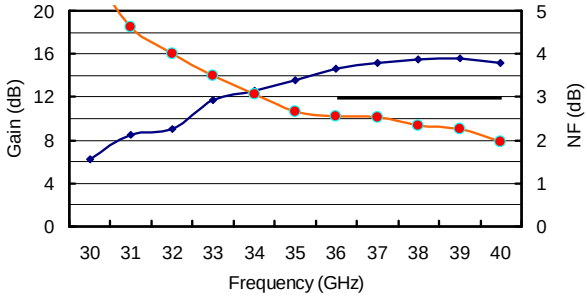
The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in chip form.



Main Features

- Broad band performance 36-40GHz
- 2.5dB noise figure, 36-40GHz
- 15dB gain, ± 0.5dB gain flatness
- Low DC power consumption, 50mA
- 20dBm 3rd order intercept point
- Chip size: 1.67 x 1.03 x 0.1mm



On wafer typical measurements

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36		40	GHz
NF	Noise figure, 36-40GHz		2.5	3	dB
G	Gain	12	15		dB
P1dB	Output power at 1dB gain compression		9		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Tamb = +25℃, Bias Conditions:Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36		40	Ghz
G	Gain (1)	12	15		dB
ΔG	Gain flatness (1)		± 0.5	± 1.0	dB
NF	Noise figure (1)		2.5	3	dB
VSWRin	Input VSWR (1)			3.0:1	
VSWRout	Ouput VSWR (1)			3.0:1	
IP3	3rd order intercept point		20		dBm
P1dB	Output power at 1dB gain compression		12		dBm
Vd	DC Voltage Vd Vg	 -2	4 -0.25	4.5 +0.4	V
Id	Drain bias current (2)		45		mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.When the chip is attached with typical 0.15nH input and output bonding wires, the indicated parameters should be improved.

(2) 45 mA is the typical bias current used for on wafer measurements, with Vg1= Vg2. For optimum noise figure, the bias current could be reduced down to 30 mA, adjusting the Vg1,2 voltage.

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5.0	V
Vg	Gate bias voltage	-2.0 to +0.4	V
Vdg	Maximum drain to gate voltage (Vd-Vg)	+5.0	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Pin	Maximum continuous input power	+1	dBm
Top	Operating temperature range	-40 to +85	℃
Tsg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Duration < 1s.

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Typical Results

Chip Typical Response (On wafer Sij)

Tamb = +25°C
Bias conditions: Vd = +4V, Id=45mA

Freq GHz	MS11 dB	PS11 °	MS12 dB	PS12 °	MS21 dB	PS21 °	MS22 dB	PS22 °
10	-6,21	154,25	-62,67	-132,87	-22,58	67,85	-2,93	-143,42
12	-6,33	141,75	-57,99	-156,02	-16,83	50,10	-3,89	-164,87
14	-6,29	127,36	-55,17	173,41	-12,52	23,11	-4,95	178,26
16	-6,08	114,92	-55,88	168,49	-9,73	-5,37	-5,86	161,51
18	-5,84	101,82	-53,92	135,46	-7,54	-31,47	-7,18	144,01
20	-5,54	86,62	-51,45	138,48	-6,13	-55,85	-8,65	131,69
21	-5,43	78,44	-50,53	139,32	-5,41	-67,16	-9,65	127,30
22	-5,30	68,96	-49,42	132,07	-4,82	-77,06	-10,46	125,73
23	-5,29	58,88	-49,04	122,68	-4,06	-85,86	-11,18	124,83
24	-5,35	47,97	-49,34	123,59	-3,25	-94,05	-11,33	125,87
25	-5,54	35,38	-47,96	126,63	-2,19	-101,60	-11,19	124,77
26	-5,87	21,00	-46,55	123,65	-0,88	-110,55	-11,01	125,49
27	-6,47	3,87	-44,77	125,28	0,38	-119,43	-10,17	122,17
28	-7,39	-16,23	-43,13	124,81	1,88	-128,85	-9,43	117,25
29	-8,77	-41,92	-40,03	123,61	3,63	-138,80	-9,11	109,58
30	-10,69	-77,04	-37,67	115,28	5,50	-151,53	-8,70	103,41
31	-12,44	-127,88	-35,70	105,15	7,35	-166,04	-8,15	94,50
32	-12,19	170,79	-33,04	93,43	9,18	176,87	-7,69	83,88
33	-10,65	120,05	-31,11	75,77	10,75	158,36	-7,59	70,55
34	-9,85	82,96	-29,60	58,30	12,14	138,69	-7,80	56,02
35	-9,98	54,87	-28,64	42,10	13,37	117,54	-8,57	40,66
36	**-10,94**	**33,47**	**-27,69**	**26,41**	**14,27**	**95,66**	**-9,80**	**25,19**
37	**-12,52**	**20,51**	**-26,89**	**9,83**	**14,95**	**73,24**	**-11,70**	**9,54**
38	**-13,72**	**17,24**	**-26,15**	**-5,87**	**15,28**	**51,13**	**-14,31**	**-4,52**
39	**-13,22**	**18,64**	**-25,53**	**-22,03**	**15,46**	**29,79**	**-17,89**	**-18,79**
40	**-11,65**	**9,29**	**-25,06**	**-38,88**	**15,53**	**8,33**	**-23,80**	**-30,52**
41	-10,30	-3,86	-24,91	-56,23	15,40	-12,86	-51,61	-16,72
42	-8,90	-20,55	-24,74	-72,65	15,17	-32,98	-26,28	118,15
43	-7,51	-38,62	-24,62	-88,50	14,89	-52,97	-20,52	111,87
44	-6,22	-59,90	-24,63	-105,66	14,54	-73,10	-17,09	101,92
45	-5,17	-81,47	-24,78	-122,84	14,05	-93,80	-14,60	89,21
46	-4,24	-102,42	-25,30	-139,10	13,39	-113,54	-12,92	73,66
47	-3,18	-122,95	-25,65	-155,88	12,59	-133,30	-11,93	59,95
48	-2,51	-143,29	-26,29	-173,89	11,55	-152,49	-11,14	47,16
49	-2,04	-161,80	-27,21	170,58	10,40	-170,65	-10,65	35,08
50	-1,62	-178,03	-27,82	157,24	9,39	172,00	-9,69	20,78

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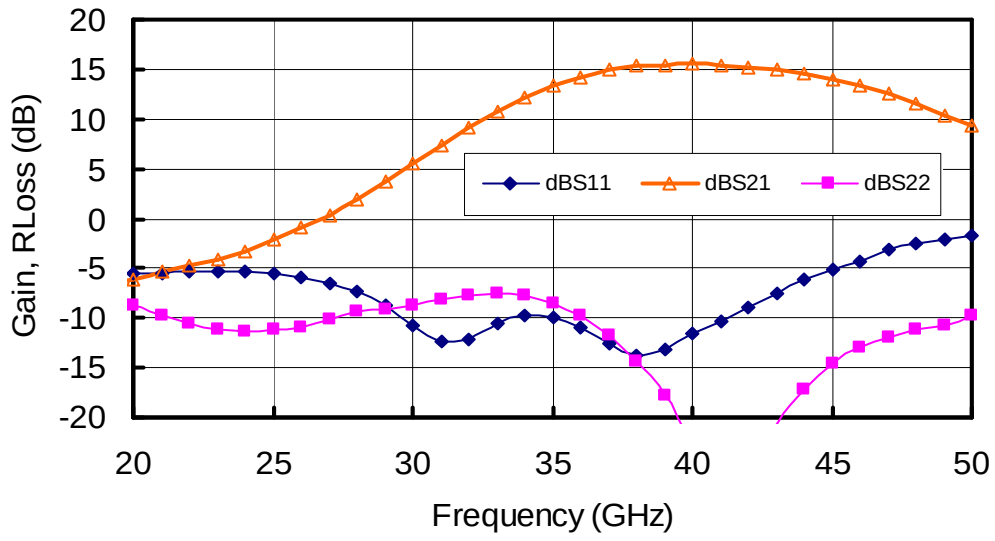
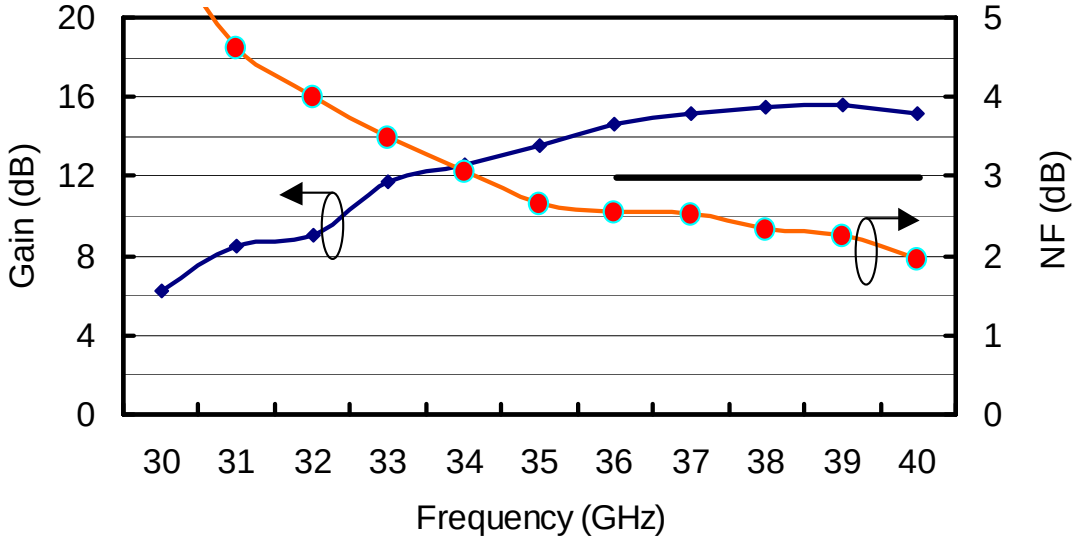
Typical Results

Chip Typical Response (On wafer Sij)

Tamb = +25℃
Vd = +4V Id=45mA



Typical Gain and Matching measurements on wafer



Typical Gain and Noise Figure measurements on wafer

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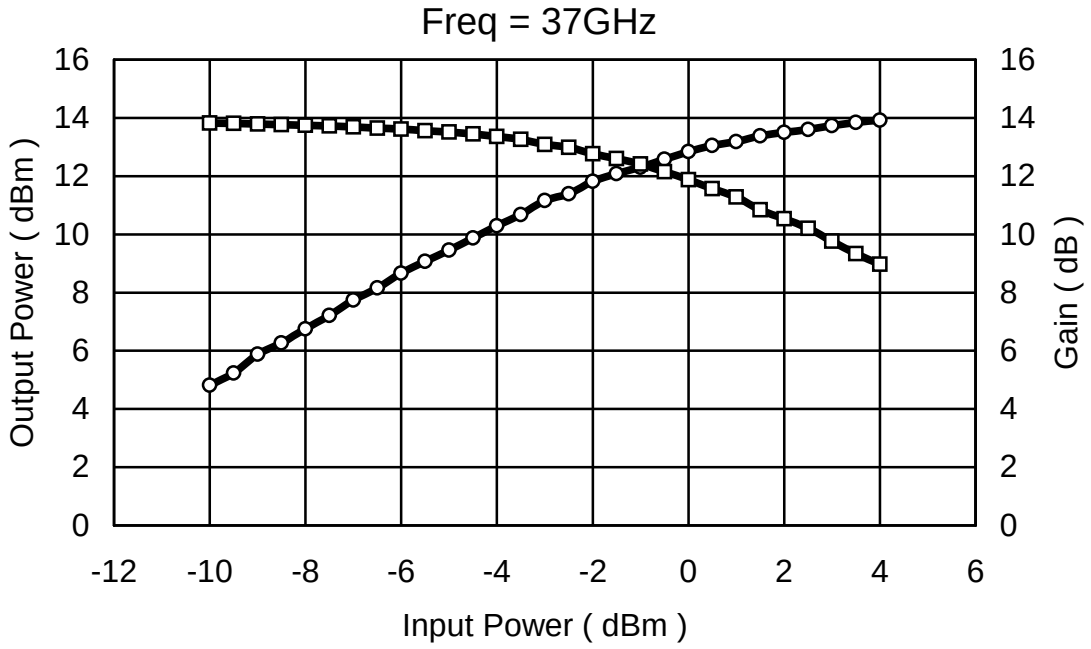
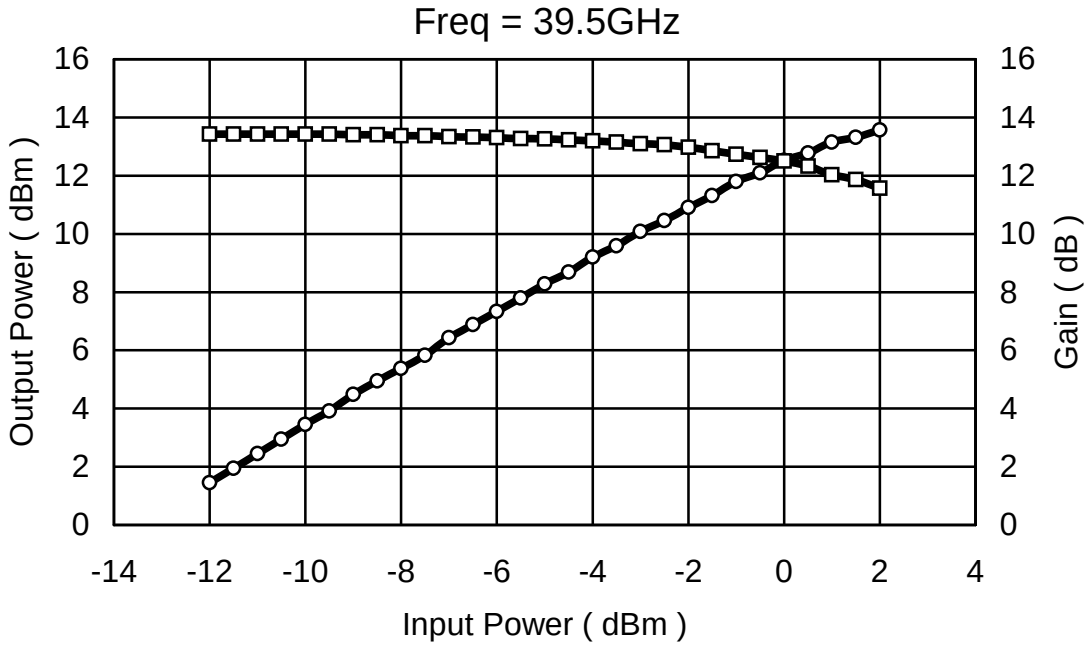
Typical Results

Tamb = +25°C
Vd = 4V ; Id = 45mA





Typical Output Power and Gain measurements in test jig
(included losses of the jig)

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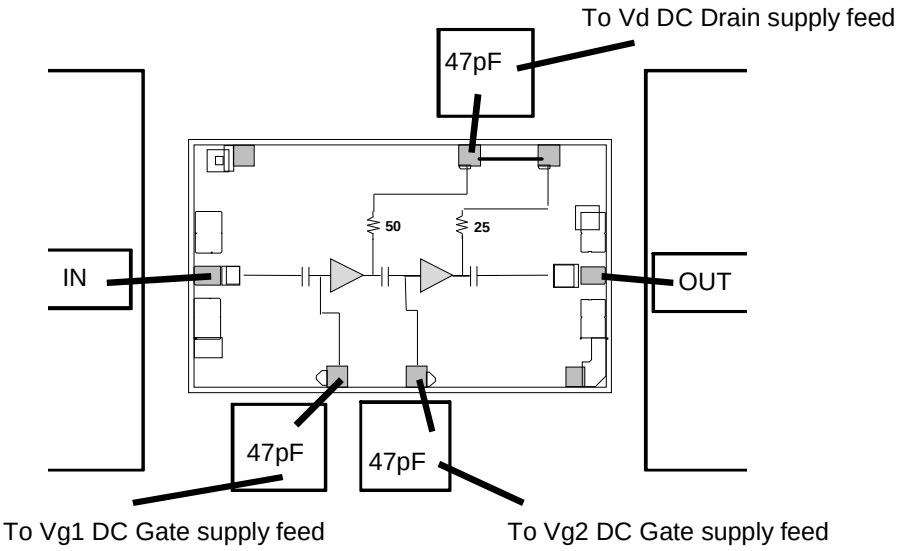
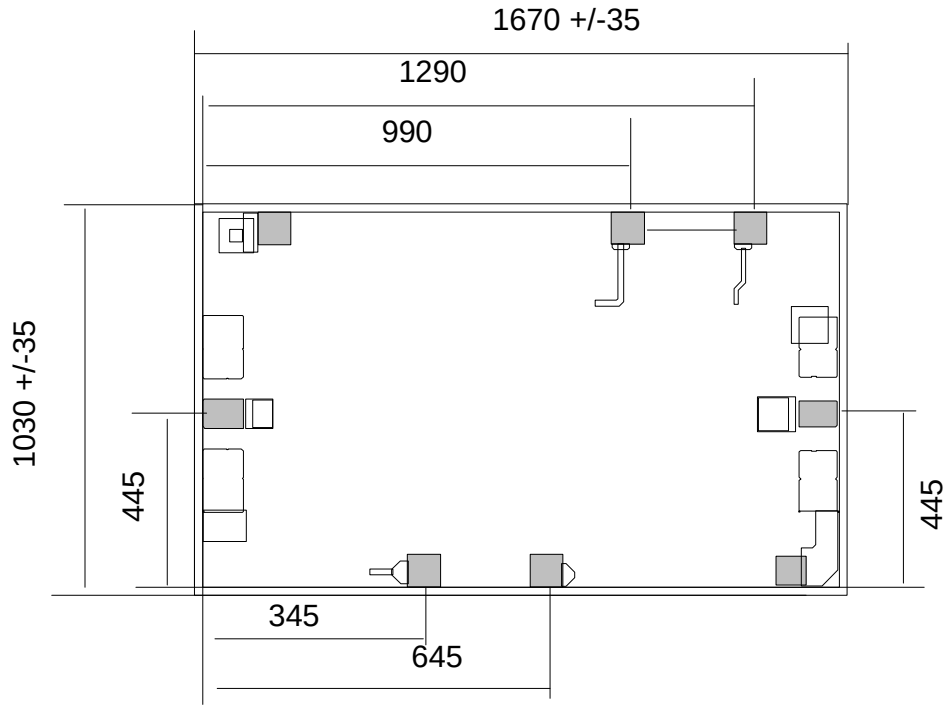
Typical Chip Assembly



Note: Supply feed should be capacitively bypassed.

Mechanical data



Bonding pad positions.
(Chip thickness: 100µm. All dimensions are in micrometers)

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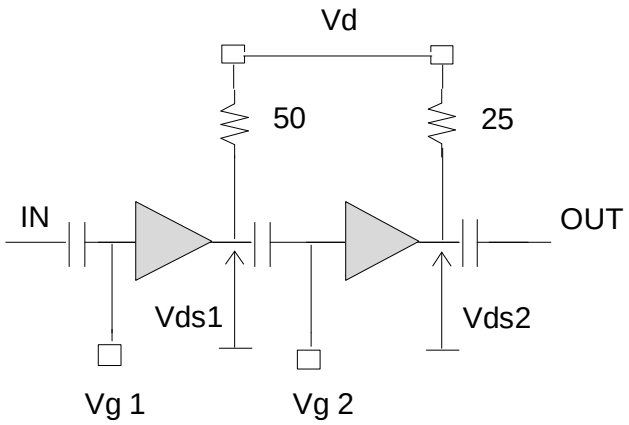
Chip Biasing

This chip is a two stage amplifier, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



Not exceed Vds = 3.5Volt (internal Drain to Source voltage).

We propose two standard biasing:

Low Noise and low consumption: Vd = 3.5V and Id = 30mA.

Low Noise and high output power: Vd = 4.0V and Id = 45mA. (A separate access to the gate voltages of the first and the output stage is provided. Nominal bias is obtained for a typical current of 30mA for the output stage and 15 mA for the first stage. The first step to bias the amplifier is to tune the Vg1 = -1V and Vg2 to drive 30mA for the full amplifier. Then Vg1 is reduced to obtain 45 mA of current through the amplifier.

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Ordering Information

Chip form : CHA2391-99F/00

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