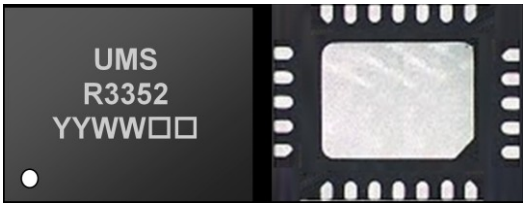
# 12-16GHz Integrated Down Converter

## GaAs Monolithic Microwave IC in SMD leadless package

## Description

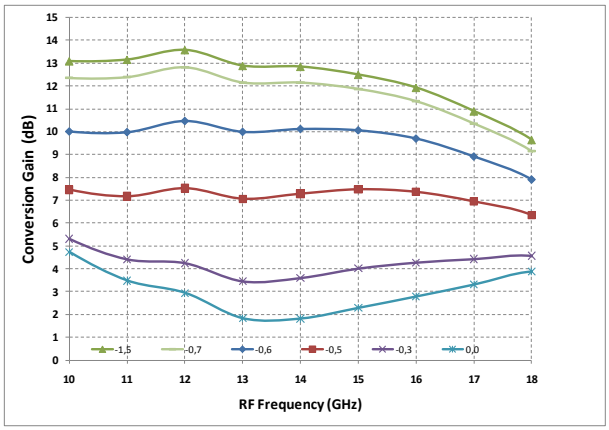
The CHR3352-QEG is a multifunction monolithic circuit, which integrates a balanced cold FET mixer, a LO buffer and a RF LNA including gain control.
It is designed for a wide range of applications, typically ISM and commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.




## Main Features

- Broadband RF performance 12-16GHz
- 13dB conversion gain
- 2dBm Input IP3
- 9dB Gain Control
- 15dBc Image Rejection
- 24LQFN4x5 – MSL1
- ESD protected

Gain versus attenuation




## Main Characteristics

Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{RF}$ | RF Frequency range | 12 | | 16 | GHz |
| $F_{LO}$ | LO Frequency range | 8.5 | | 19.5 | GHz |
| $F_{IF}$ | IF Frequency range | DC | | 3.5 | GHz |
| $G_c$ | Conversion gain | | 13 | | dBm |



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Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FRF | RF frequency range | 12 | | 16 | GHz |
| FLO | LO frequency range | 8.5 | | 19.5 | GHz |
| FIF | IF frequency range | DC | | 3.5 | GHz |
| $C_G$ | Conversion gain@ min. attenuation (1) | | 12 | | dB |
| $\Delta G$ | Gain control range | | 9 | | dB |
| NF | Noise Figure@ min. attenuation, IF>0.1GHz | | 2.7 | | dB |
| Im_rej | Image rejection (1) | | 15 | | dBc |
| PLO | LO Input power | | 0 | | dBm |
| IIP3 | Input IP3@ at Gc max. | | 2 | | dBm |
| LO RL | LO Return Loss | | -12 | | dB |
| RF RL | RF Return Loss | | -12 | | dB |
| VD, VDL | DC drain voltage | | 4.0 | | V |
| IDL | LNA current | | 120 | | mA |
| ID | LO Buffer current | | 130 | | mA |
| VG2, 3 | LNA DC gate voltage | | -0.5 | | V |
| B | LO Buffer DC gate voltage | | -3 | | V |
| IB | LO Buffer DC gate current | | -7 | | mA |
| GC | Gain control DC voltage | -1.5 | | 0 | V |

(1) An external combiner 90° is required on I / Q
These values are representative of on-board measurements.
Note: Id is not affected by GC.

Electrostatic discharge sensitive device, observe handling precautions!



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## Absolute Maximum Ratings (1)

Tamb.= +25°C

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| VD, VDL | Maximum drain bias voltage | 4.5 | V |
| Id_total | Maximum drain bias current | 420 | mA |
| VGL | LNA DC gate voltage | -2.0 to +0.4 | V |
| B | Buffer, Mixer DC gate voltage | -4 | V |
| GC | Gain control voltage | -2.5 to + 0.8 | V |
| P_RF | Maximum peak input power overdrive | 10 | dBm |
| P_LO | Maximum LO input power | 5 | dBm |
| Tch | Maximum channel temperature | 175 | °C |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

(1) Operation of this device above anyone of these parameters may cause permanent damage.

## Typical Bias Conditions

Tamb.= +25°C

| Symbol | Pad N° | Parameter | Values | Unit |
|---|---|---|---|---|
| VDL, VD | 10, 11 | DC drain voltages | 4 | V |
| IDL | 10 | LNA current controlled with VG2, 3 | 120 | mA |
| VG2, 3 | 8, 9 | LNA DC gate voltage | -0.5 | V |
| B | 12 | Buffer DC gate voltage | -3 | V |
| GC | 7 | Gain control DC voltage | -1.5 to 0 | V |



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## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

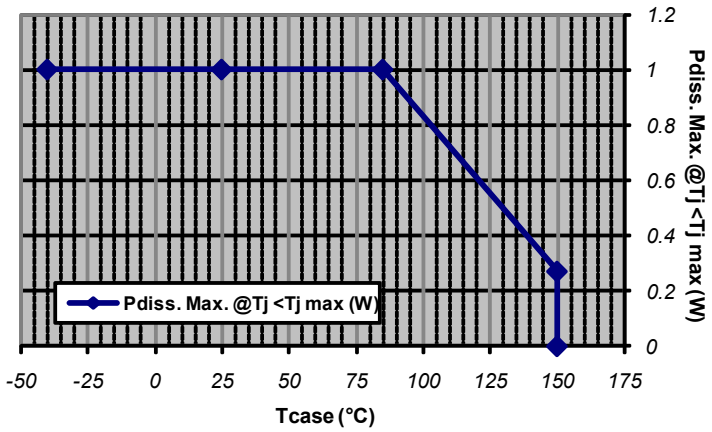
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

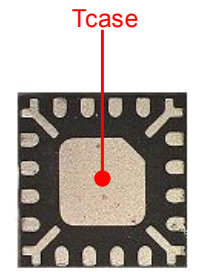
| DEVICE THERMAL SPECIFICATION : CHR3352-QEG | | | |
|---|---|---|---|
| Recommended max. junction temperature (Tj max) | : | 174 | °C |
| Junction temperature absolute maximum rating | : | 175 | °C |
| Max. continuous dissipated power (Pdiss. Max.) | : | 1.0 | W |
| => Pdiss. Max. derating above Tcase(1)= 85 °C | : | 11 | mW/°C |
| Junction-Case thermal resistance (Rth J-C)(2) | : | <89 | °C/W |
| Minimum Tcase operating temperature(3) | : | -40 | °C |
| Maximum Tcase operating temperature(3) | : | 85 | °C |
| Minimum storage temperature | : | -55 | °C |
| Maximum storage temperature | : | 150 | °C |

*(1) Derating at junction temperature constant = Tj max.*

*(2) Rth J-C is calculated for a worst case considering the* ***hottest junction*** *of the MMIC and all the devices biased.*

*(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).*




Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.0



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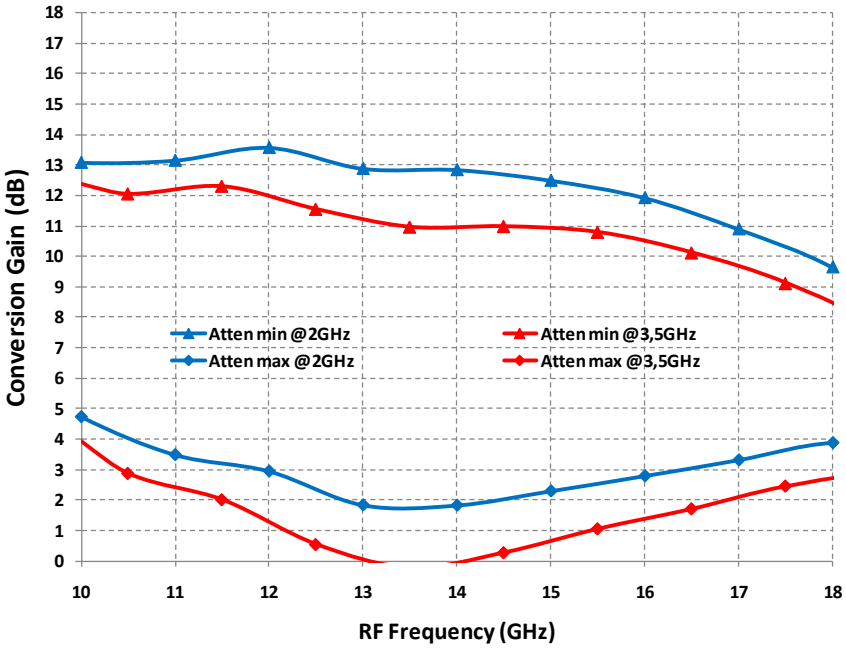
## Typical Measured Performances [1]

Tamb = +25°C, VD=VDL= 4V, VG2=VG3= -0.5V, VGM = -0.7V, P_LO = 0dBm
Board losses de-embedded (result given on package access planes)

**Conversion Gain versus RF & IF Frequencies**
RF = LO+ IF, GC = -1.5V & 0V




[1] If no specific mention, the following values are representative of onboard measurements (on connector access planes) as defined on the drawing at paragraph Evaluation mother board. The board losses are estimated from 0.8 to 1.2dB in the frequency range.



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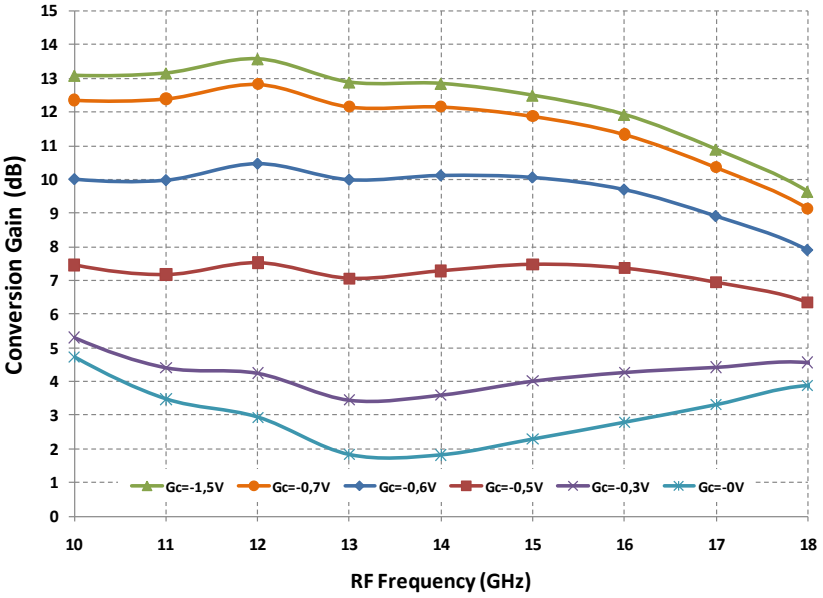
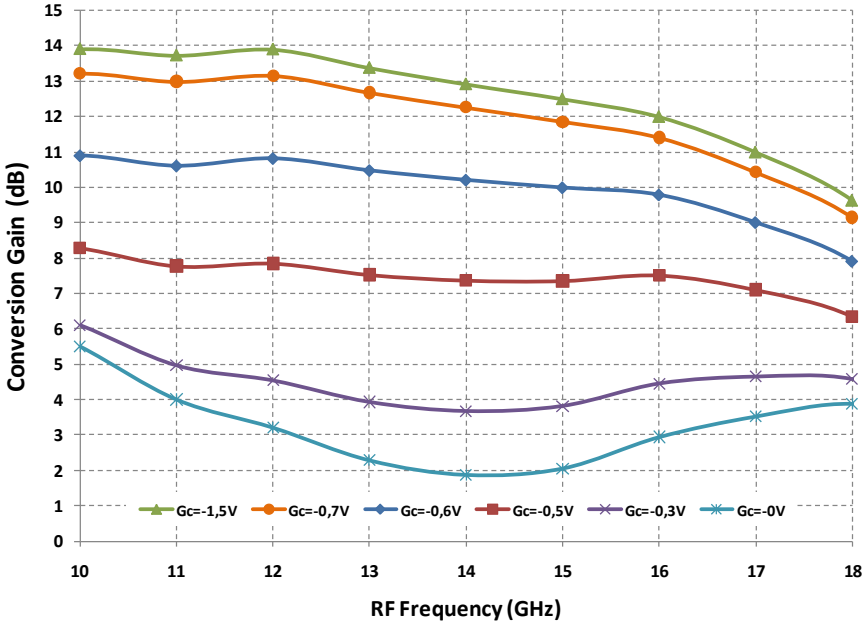
Board losses de-embedded (result given on package access planes)

**Conversion Gain in Supradyne Mode versus RF Frequency & GC**
RF = LO+ IF, IF = 2GHz




**Conversion Gain in infradyne Mode versus RF Frequency & GC**
RF = LO- IF, IF = 2GHz



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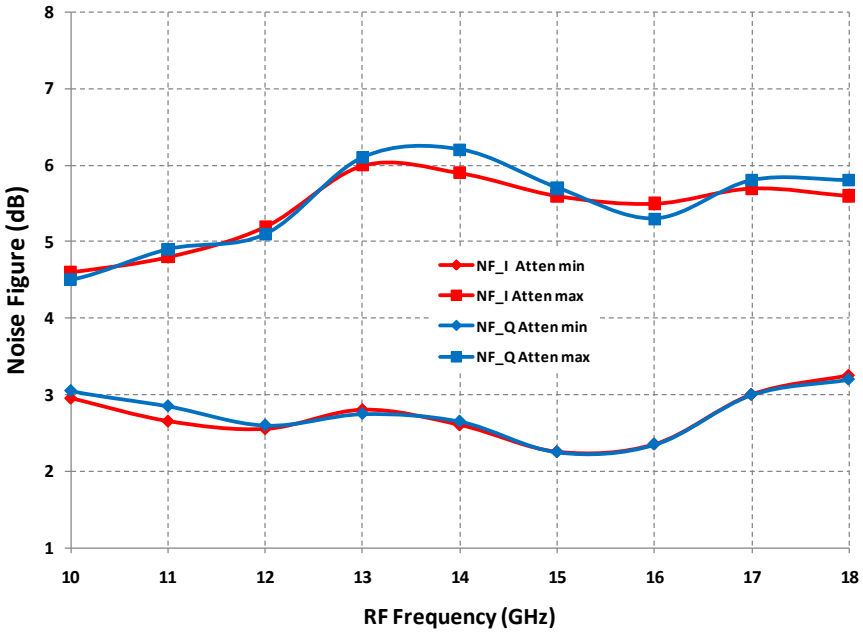
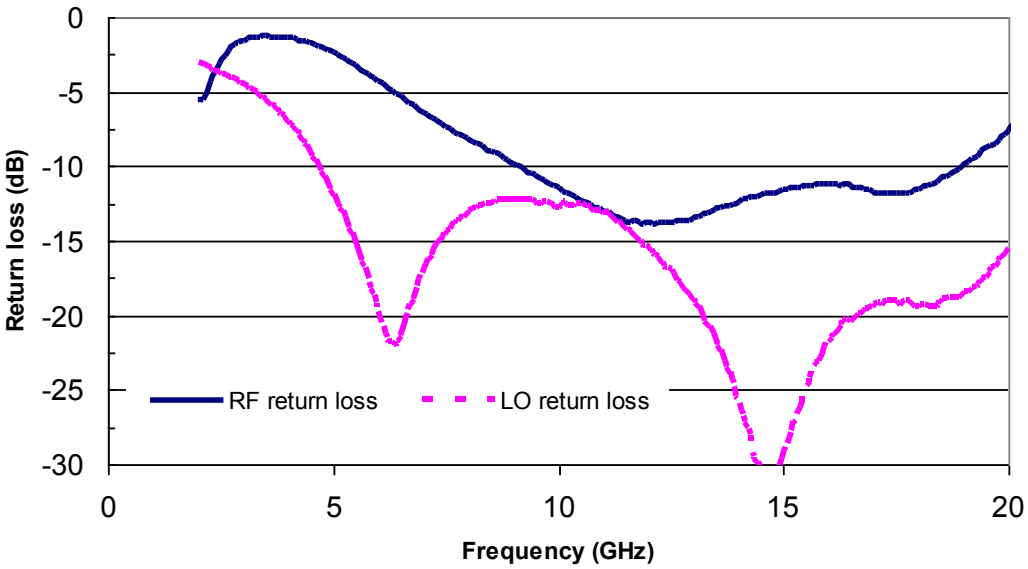
## Typical Measured Performances

Tamb = +25°C, VD=VDL= 4V, VG2=VG3= -0.5V, VGM = -0.7V, P_LO = 0dBm
Board losses de-embedded (result given on package access planes)

**Noise Figure versus Frequency**
RF = LO+/- IF, IF = 2GHz, GC = -1.5 & 0V




**Return loss versus Frequency**
GC = -1.5V



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Tamb = +25°C, VD=VDL= 4V, VG2=VG3= -0.5V, VGM = -0.7V, P_LO = 0dBm
Board losses de-embedded (result given on package access planes)

**Image Rejection versus frequency**
RF = LO+/- IF, IF = 2GHz, GC = -1.5V

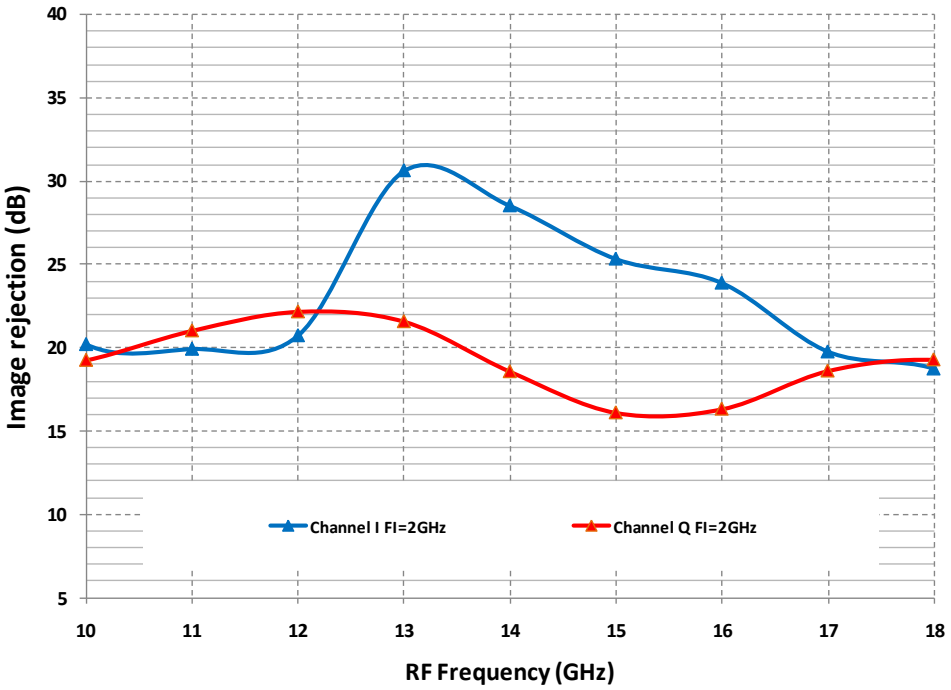
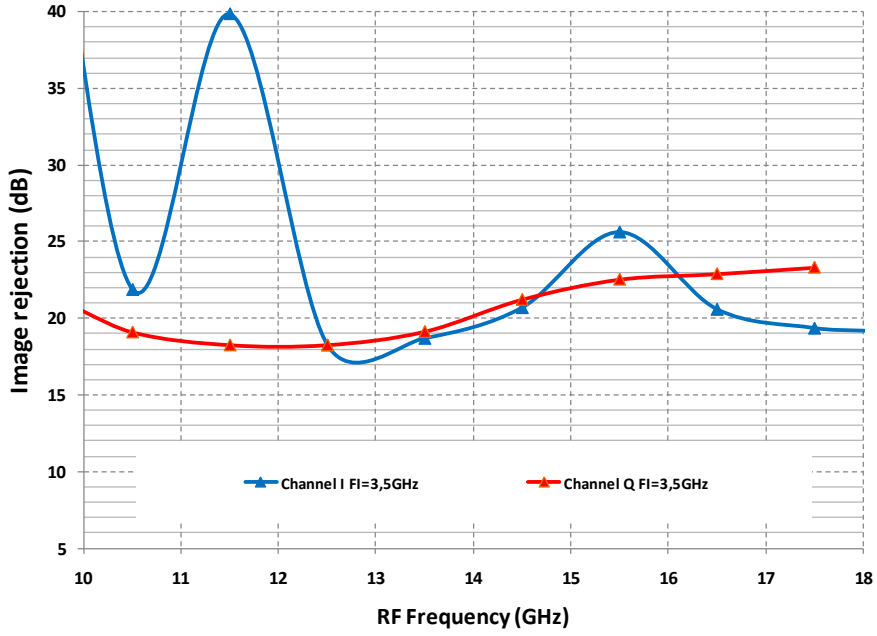



**Image Rejection versus Frequency**
RF = LO+/- IF, IF = 3.5GHz, GC = -1.5V



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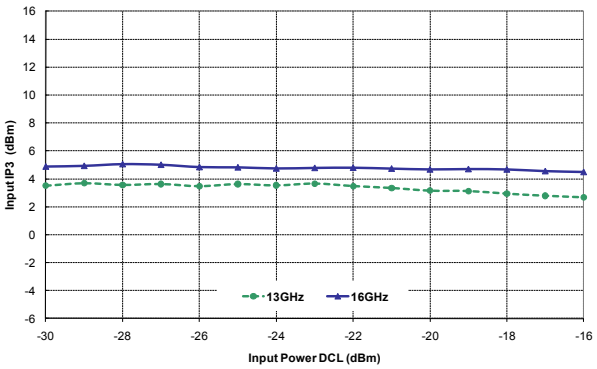
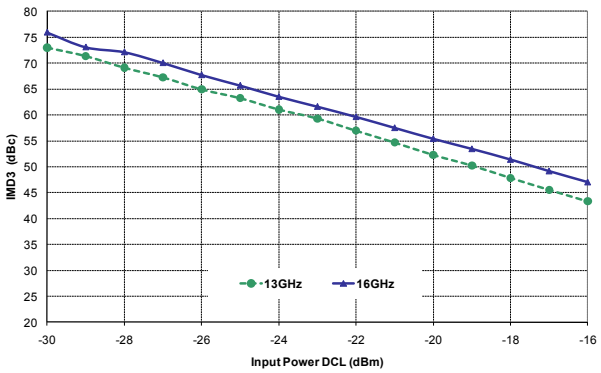
Tamb = +25°C, VD=VDL= 4V, VG2=VG3= -0.5V, VGM = -0.7V, P_LO = 0dBm
Board losses de-embedded (result given on package access planes)

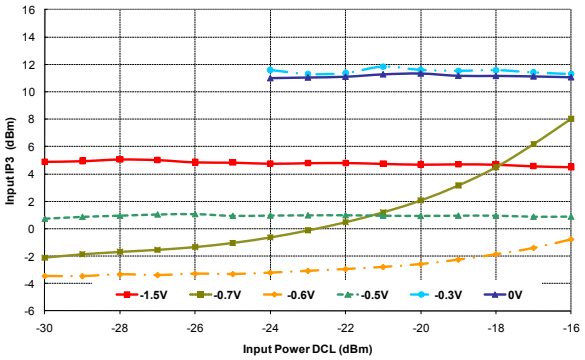
### Input IP3 versus Freq. at GC = -1.5V



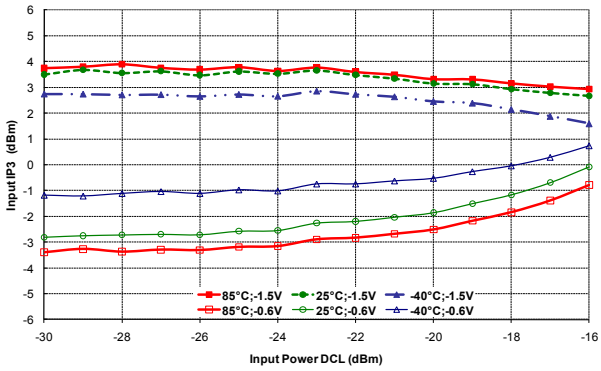

### IMD3 versus Freq. at GC = -1.5V




### Input IP3 versus GC at 16GHz




### Input IP3 vs temperature at 13GHz



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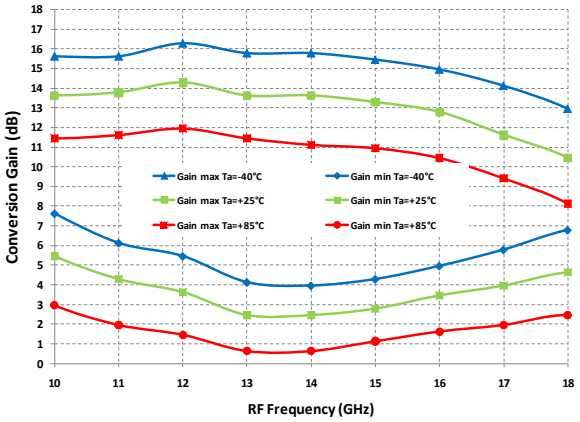
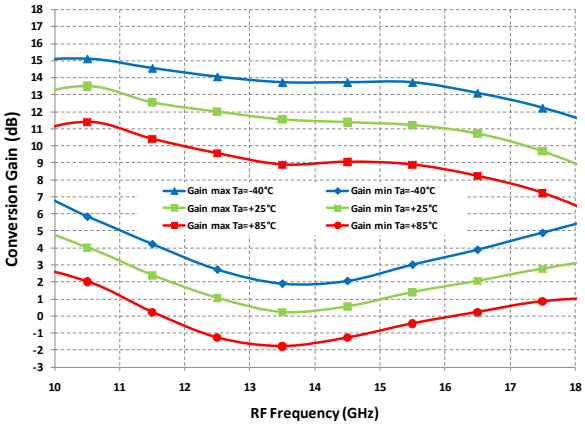
## Typical Measured Performances

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD=VDL= 4V, VG2=VG3= -0.5V, VGM = -0.7V, P_LO = 0dBm
Board losses de-embedded (result given on package access planes)

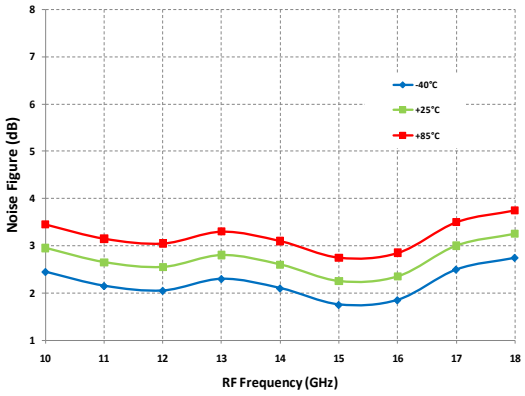
### Conversion Gain vs Temperature
IF = 2GHz, GC = -1.5V & 0V



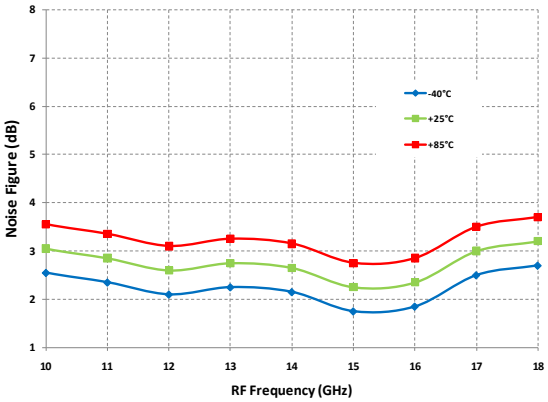

### Conversion Gain vs Temperature
IF = 3.5GHz, GC = -1.5V & 0V




### Noise figure vs Temperature
Supradyne, IF = 2GHz, GC = -1.5V




### Noise figure vs Temperature
Infradyne, IF = 2GHz, GC = -1.5V




### Spurious on IF outputs
P_RF = -20dBm / P_LO = 0dBm @12GHz

| | nLO | | | | |
|---|---|---|---|---|---|
| mRF | 0 | 1 | 2 | 3 | 4 |
| 0 | Xx | 12 | 9 | 22 | >40 |
| 1 | 26 | 24 | >40 | 32 | >40 |
| 2 | 39 | >40 | 37 | >40 | >40 |
| 3 | 33 | >40 | >40 | >40 | >40 |
| 4 | >40 | >40 | >40 | >40 | >40 |

All values in dBc below IF power level (IF = 1GHz).
Data measured without external hybrid coupler.



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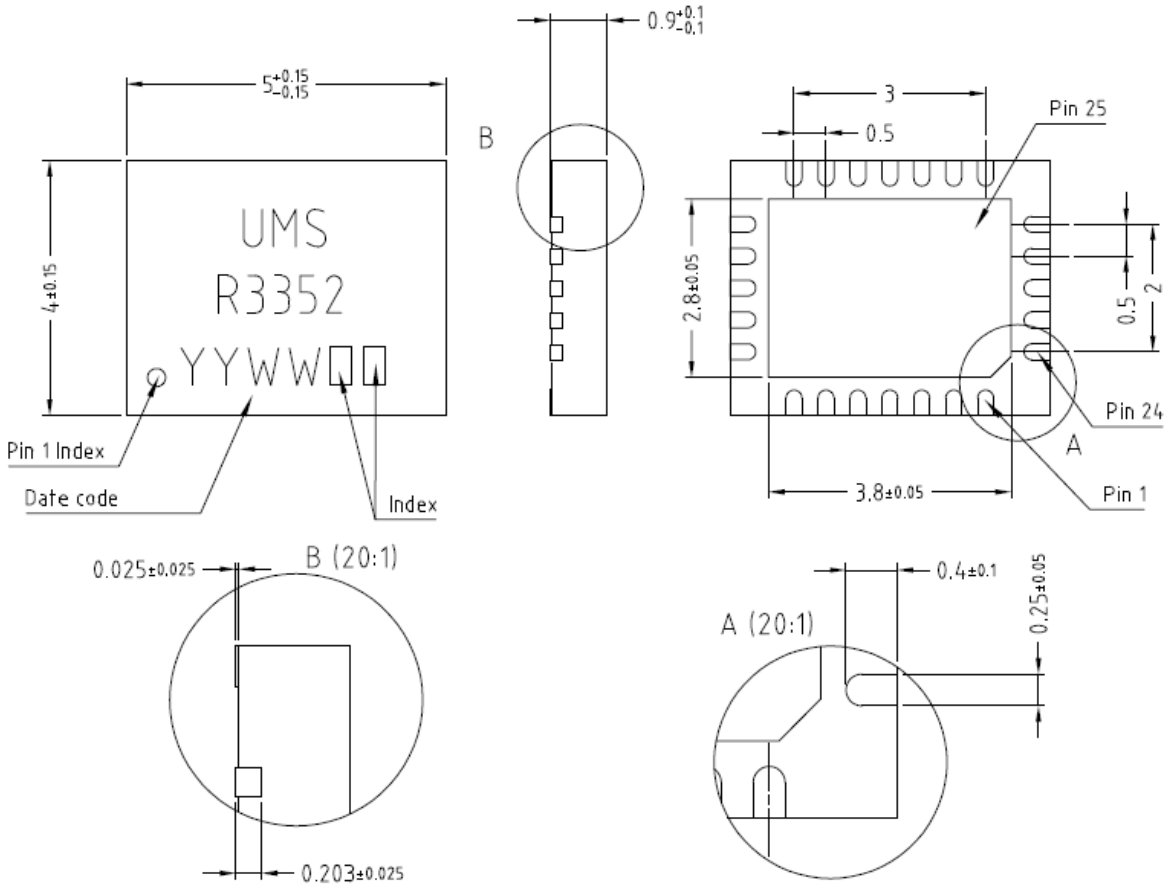
## Package outline (1)




| | | | | |
|---|---|---|---|---|
| Matt tin, Lead Free | (Green) | 1- Nc | 9- VG3 | 17- Nc |
| Units : | mm | 2- Nc | 10- VDL | 18- Nc |
| From the standard : | JEDEC MO-220 | 3- Nc | 11- VD | 19- Nc |
| | (VGGD) | 4- Gnd(2) | 12- B | 20- IF_I |
| 25- GND | | 5- RF in | 13- Nc | 21- Gnd(2) |
| | | 6- Nc | 14- Nc | 22- IF_Q |
| | | 7- GC | 15- LO in | 23- Nc |
| | | 8- VG2 | 16- Gnd(2) | 24- Nc |

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.



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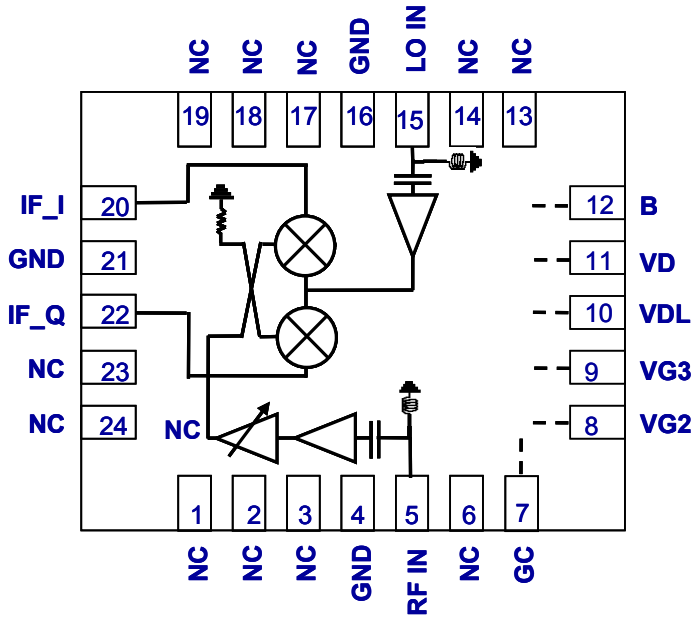
## Note:

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.




ESD protections are also implemented on gate and control accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.



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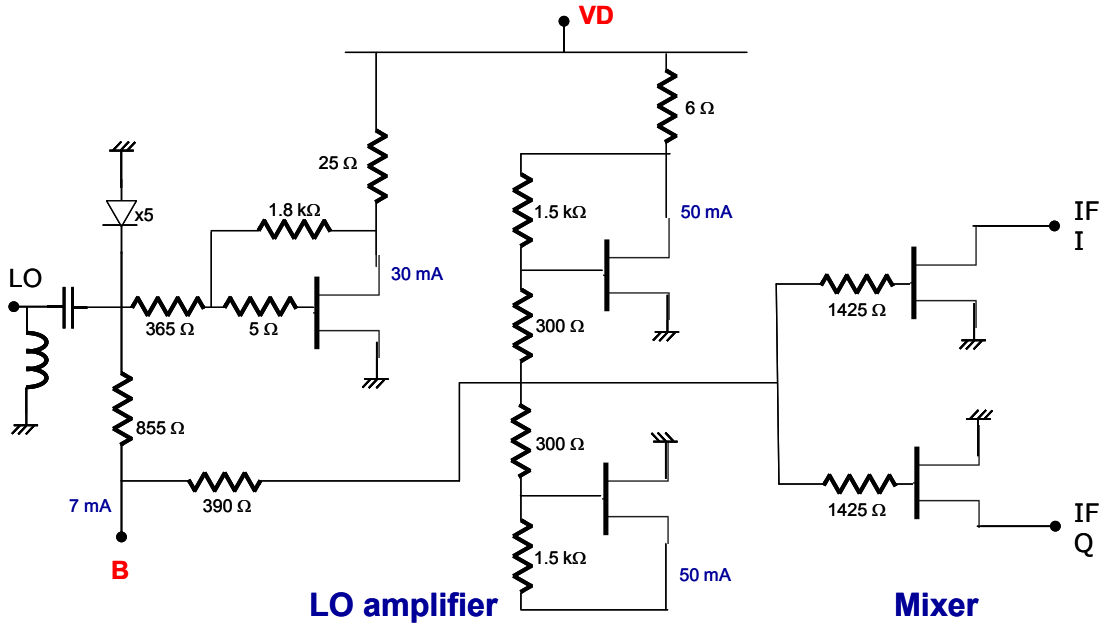
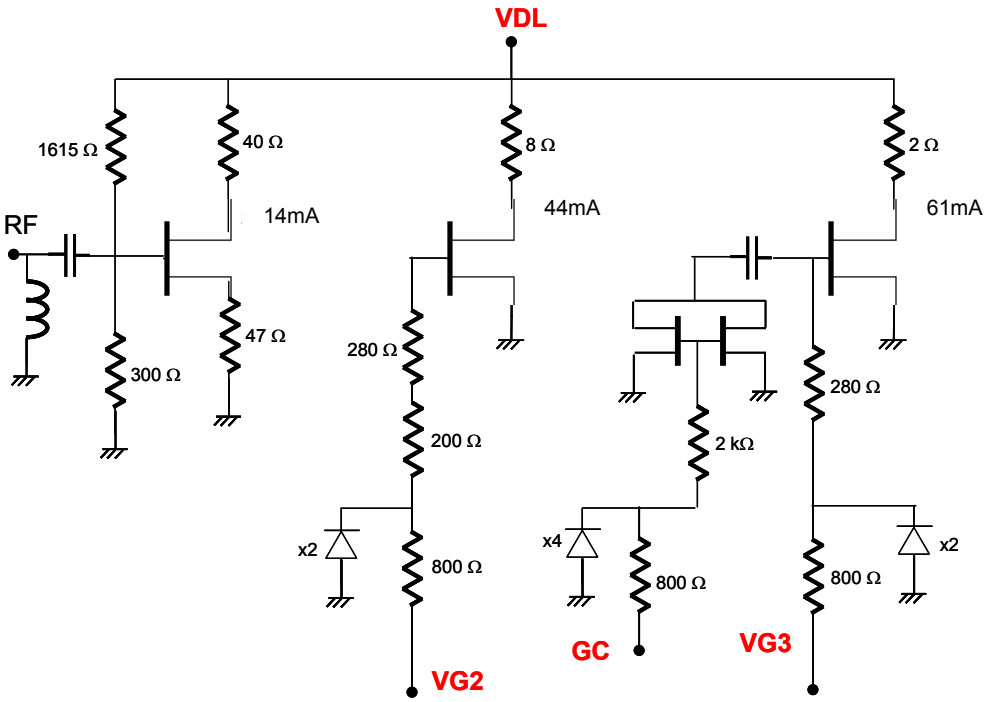
## DC Schematic

**LO Amplifier and Mixer: 4V, 130mA; -3V, 7mA**




**LNA: 4V, 120mA**



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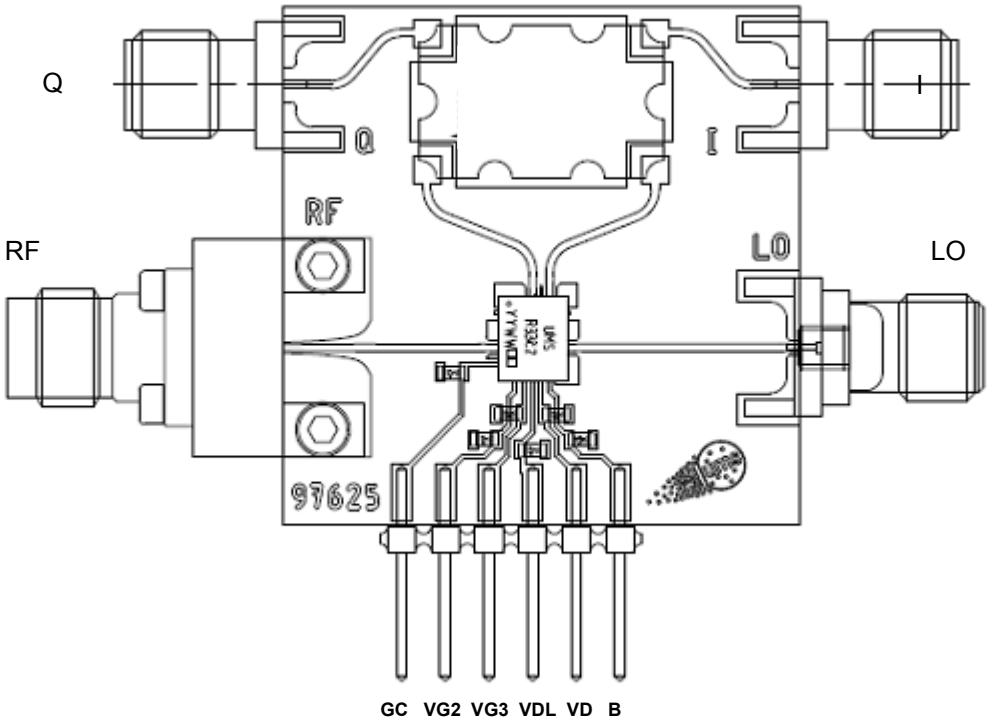
## Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Hybrid coupler 90°; 2- 4GHz



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## Notes



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## Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

## Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

| | | |
|---|---|---|
| QFN 4x5 RoHS compliant package: | CHR3352-QEG/XY | |
| | Stick: XY = 20 | Tape & reel: XY = 21 |





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